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High-Performance and Energy-Efficient CNFET-Based Designs for Ternary Logic Circuits

RAMZI A. JABER[1], (Student Member, IEEE), ABDALLAH KASSEM[2], (SENIOR MEMBER, IEEE), AHMAD M. EL-HAJJ[1], (MEMBER, IEEE), LINA A. NIMRI[3], AND ALI M. HAIDAR[1]

[1]Department of Computer and Electrical Engineering, Beirut Arab University, Debbieh, Lebanon (e-mail: r.jaber@bau.edu.lb; a.elhajj@bau.edu.lb; ari@bau.edu.lb)
[2]Department of Electrical and Computer Engineering, Notre Dame University-Louaize, Lebanon (e-mail: akassem@ndu.edu.lb)
[3]Department of Business Computer, Lebanese University, Beirut, Lebanon (e-mail: lnimri@ul.edu.lb)

Corresponding author: Ramzi A. Jaber (e-mail: r.jaber@bau.edu.lb).

ABSTRACT Recently, the demand for portable electronics and embedded systems has increased. These devices need low-power circuit designs because they depend on batteries as an energy resource. Moreover, Multi-Valued Logic (MVL) circuits provide notable improvements over binary circuits in terms of interconnect complexity, chip area, propagation delay, and energy consumption. Therefore, this paper proposes new ternary circuits aiming to lower the power delay product (PDP) to save battery consumption. The proposed designs include new ternary gates [Standard Ternary Inverter (STI), Ternary NAND ($TNAND$)] and combinational circuits [Ternary Decoder ($TDecoder$), Ternary Half-Adder (THA), and Ternary Multiplier ($TMUL$)] using Carbon Nano-Tube Field Effect Transistors (CNFET). The paper employs the best trade-off between reducing the number of used transistors, utilizing energy-efficient transistor arrangement such as transmission gate and applying the dual supply voltages (Vdd, and Vdd/2). The five proposed designs are compared to the latest fifteen ternary circuits using the HSPICE simulator for different supply voltages, different temperatures, and different frequencies. One hundred eighty simulations are performed to prove the efficiency of the proposed designs. The results show the advantage of the proposed designs in reduction over 43% in terms of transistors' count for the ternary decoder and over 88%, 99%, 98%, 86%, and 78% in energy consumption (PDP) for the STI, $TNAND$, $TDecoder$, THA, and $TMUL$ respectively.

INDEX TERMS Carbon Nano-Tube Field Effect Transistors (CNFET), Ternary Combinational Circuits, Ternary Logic Gates, Multi-Valued Logic (MVL), Power Delay Product.

I. INTRODUCTION

THE limitation in the binary circuit is due to a large number of connections thus requiring a big chip area and a notable increase in energy consumption. Whereas, Multi-Valued Logic (MVL) system has more than two-valued logic to lower interconnections, chip area of up to 70% [1], and energy consumption by more than 50% [2]. Moreover, the authors of [3] has proved mathematically that ternary logic is the most efficient in circuit complexity and cost compared to other bases. Ternary logic systems can represented in two ways: balanced ternary logic (-1, 0, 1) corresponding to (-Vdd, 0, Vdd), and standard (unbalanced) ternary logic (0, 1, 2) corresponding to (0, Vdd/2, Vdd).

For the past decade, MVL has attracted researchers' attention over binary logic. MVL can be implemented in software (algorithm) and circuit design such as logic gates, combinational circuits, memory circuits, programmable logic arrays (PLAs), MV-Quantum Logic, and wireless sensor networks [4]–[10].

Different transistor technologies have been used such as CMOS [11], FinFet [12], and CNFET [13]–[18]. Among the mentioned techniques, CNFET provides the best trade-off in terms of energy efficiency and circuit speed [19].

Therefore, this paper uses CNFET technology in the design of the ternary circuits. The proposed designs will compare to the latest CNFET-based designs in [13]–[18], which are known to provide efficient circuit designs in terms of transistor count, power and PDP. In particular, [13] presents the

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STI, $TNAND$, $TNOR$, $TDecoder$, THA, and $TMUL$ using CNFET. In [14] and [17], a ternary decoder design described in replacing the $TNOR$ with a binary NOR. In [15], [16], [18], improved circuit designs for the STI, $TNAND$, THA, and $TMUL$, are presented.

This paper proposes new designs for the STI, $TNAND$, $TDecoder$, THA, and $TMUL$ by reducing the number of used transistors, utilizing energy-efficient transistor arrangement such as transmission gate and applying the dual supply voltages Vdd (0.9 V), and Vdd/2 (0.45 V) from the same power supply [18].

The new designs provide a considerable gain in terms of system performance which they have the lowest PDP compared to the designs in [13]–[18] as demonstrated in the HSPICE-based simulation results. Therefore, the proposed circuits can be implemented in low-power portable electronics and embedded systems to save battery consumption.

The rest of the paper is organized as follows: Section II provides a background of CNFETs and existing ternary logic gates, while the proposed new ternary logic gates are described in section III, and the proposed combinational circuits in section IV. Simulation results and comparisons are discussed in section V followed by the Conclusion.

II. BACKGROUND

A. CNFET DESIGN

Full details about the Stanford CNFET model found at [20]–[22], but it is worth mentioning that the CNFETs use a semiconducting single-walled CNT as a channel for conduction with high drive current 35 μA when the supply voltage Vdd is equal to 0.9 V. The improvement of intrinsic CNFET over bulk MOSFET device is about 13 times better. The angle of atom arrangement along the tube in a single-walled CNT (SWCNT) is chirality vector which is represented by the integer pair (n, m). This chirality vector determines if the CNT is metallic or semiconducting; if $n = m$ or n–m = $3j$, where j is an integer, then the nanotube is metallic else it is semiconducting. The CNFET diameter can be calculated from the equation in (1):

$$D_{\text{cnt}} = \frac{\sqrt{3} \cdot a_0}{\pi} \sqrt{n^2 + m^2 + nm} \tag{1}$$

Where a_0 = 0.142 nm is the inter-atomic distance between each carbon atom and its neighbor, and the integer pair (n, m) represents the chirality vector. The characteristics of the CNFET model are similar to traditional MOSFETs. Except for the threshold voltage which is calculated by the following equation (2):

$$V_{\text{th}} = \frac{E_g}{2 \cdot e} = \frac{\sqrt{3}}{3} \frac{a \cdot V\pi}{e \cdot Dcnt} \tag{2}$$

Where a = 2.49 Å is the carbon to carbon atom distance, $V\pi$ = 3.033 eV is the carbon bond energy in the tight binding model, e is the electron charge unit, and $Dcnt$ is the CNT diameter.

In general, three chiralities can be used in the ternary logic design. Table 1 shows the relationship between the chirality, diameter, and threshold voltage.

TABLE 1: The relation between the chirality, diameter, and threshold voltage

		Threshold voltage	
Chirality	CNT diameter	N-CNFET	P-CNFET
(19,0)	1.487nm	0.289V	- 0.289V
(13,0)	1.018nm	0.428V	- 0.428V
(10,0)	0.783nm	0.559V	- 0.559V

B. EXISTING TERNARY LOGIC GATES

The basic ternary logic gates are $NOT, AND, OR, NAND$ and NOR. A_i and B_j are the ternary inputs where i and j $\in$ {0, 1, 2}. The ternary equations of the basic ternary logic gates are presented in (3):

$$\begin{aligned} NOT: &\quad \overline{A_i} = 2 - A_i, \\ AND: &\quad A_i \bullet B_j = min\{A_i, B_j\}, \\ OR: &\quad A_i + B_j = max\{A_i, B_j\}, \\ NAND: &\quad \overline{A_i \bullet B_j} = \overline{min\{A_i, B_j\}}, \\ NOR: &\quad \overline{A_i + B_j} = \overline{max\{A_i, B_j\}}, \end{aligned} \tag{3}$$

In [13], the authors present three types of ternary inverters, $TNAND$, and $TNOR$ logic gate using CNFET.

The first inverter is a standard ternary inverter (STI), the second is a negative ternary inverter (NTI), and the third one is a positive ternary inverter (PTI). Table 2 shows the truth table for the three ternary inverters.

Table 3 shows the truth table for Two-inputs $TNAND$ and $TNOR$ logic gates.

III. PROPOSED TERNARY LOGIC GATES

The existing STI and $TNAND$ logic gates designs in [13], [16], and [18] are shown in Fig. A1 and A2 in the appendix.

This section proposes new designs of STI and $TNAND$ logic gates as shown in Fig. 1 and Fig. 2.

Table 4 shows the disadvantage of the existing STI and $TNAND$ in [13], [16], and [18] and the advantage of the proposed ternary logic gates.

A. PROPOSED STANDARD TERNARY INVERTER

Fig. 1 shows the transistor level design of the proposed STI where the chirality, diameter, and threshold voltage (Vth) of the CNFETs used are shown in Table 5.

TABLE 2: The truth table for the three ternary inverters

Ternary Input	STI	NTI	PTI
Logic 0 (0 V)	2	2	2
Logic 1 (0.45 V)	1	0	2
Logic 2 (0.9 V)	0	0	0

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Table 6 shows the detailed operation of the proposed STI circuit of Fig. 1.

When the input A is logic 0, then transistors (T1, and T4) are turned ON and (T2, and T5) are turned OFF. The output A_p is equal to logic 2, then transistor (T3) is turned ON. Therefore, the output $\bar{A}$ is equal to logic 2.

When the input A is logic 1, then transistor (T1) is turned ON, and (T2, T4, and T5) are turned OFF. The output A_p is equal to logic 2, then transistor (T3) is turned ON. Therefore, the output $\bar{A}$ is equal to logic 1.

Finally, when the input A is logic 2, then transistors (T2, and T5) are turned ON and (T1, and T4) are turned OFF. The output A_p is equal to logic 0, then transistor (T3) is turned OFF. Therefore, the output $\bar{A}$ is equal to logic 0.

B. PROPOSED TERNARY NAND

Fig. 2 shows the transistor level design of the proposed two inputs $TNAND$ where the chirality, diameter, and threshold voltage (Vth) of the CNFETs used are shown in Table 7.

Table 8 shows the selected combinations of two ternary inputs A and B to describe the operation of the proposed $TNAND$ logic gate circuit of Fig. 2.

When the inputs (A, B) are (0 V, 0 V), then transistors (T1, T3, T7, and T8) are turned ON and (T2, T4, T9, and T10) are turned OFF. The outputs (A_n, B_n) are equal to (0.9 V, 0.9 V), then transistors (T5, and T6) are turned OFF. Therefore, the output is equal to 0.9 V.

When the inputs (A, B) are (0 V, 0.45 V), then transistors (T1, T4, and T7) are turned ON and (T2, T3, T8, T9, and T10) are turned OFF. The outputs (A_n, B_n) are equal to (0.9 V, 0 V), then transistor (T6) is turned ON and (T5) is turned OFF. Therefore, the output is equal to 0.9 V.

When the inputs (A, B) are (0.45 V, 0.45 V), then transistors (T2, and T4) are turned ON and (T1, T3, T7, T8, T9, and T10) are turned OFF. The outputs (A_n, B_n) are equal to (0 V, 0 V), then transistors (T5, and T6) are turned ON. Therefore, the output is equal to 0.45 V.

Finally, when the inputs (A, B) are (0.45 V, 0.9 V), then transistors (T2, T4, and T10) are turned ON and (T1, T3, T7, T8, and T9) are turned OFF. The outputs (A_n, B_n) are equal to (0 V, 0 V), then transistors (T5, and T6) are turned ON. Therefore, the output is equal to 0.45 V.

TABLE 3: The truth table for Two-inputs $TNAND$ and $TNOR$ logic gates

Input		Output	
A	B	TNAND	TNOR
0	0	2	2
0	1	2	1
0	2	2	0
1	0	2	1
1	1	1	1
1	2	1	0
2	0	2	0
2	1	1	0
2	2	0	0

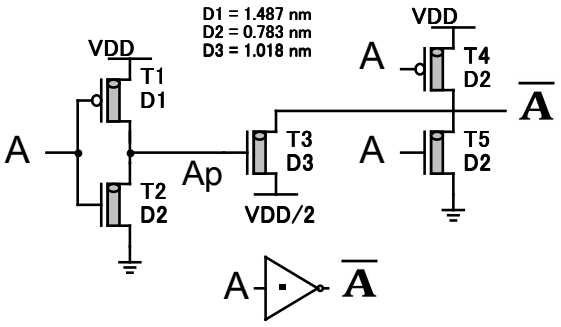

FIGURE 1—Transistor Level of the proposed STI.

IV. PROPOSED COMBINATIONAL CIRCUITS

This section proposes some of the combinational circuits such as $TDecoder$, THA, and $TMUL$.

A. PROPOSED TERNARY DECODER

The ternary decoder converts n trits information inputs to a maximum 3^n unique outputs. It is used in many applications such as the ternary adder, ternary multiplier, ternary memory, and others.

Ternary decoder with one ternary input (X), and three binary outputs (X_0, X_1, X_2) are described mathematically in equation (4) and its truth table is shown in Table 10.

$$X_{k,k\in\{0,1,2\}} = \begin{cases} 2, & if x = k \\ 0, & if x \neq k \end{cases} \tag{4}$$

The existing $TDecoders$ in [13], [14], and [17] are shown in Fig. A3 in the appendix with 16, 10, and 11 transistors respectively.

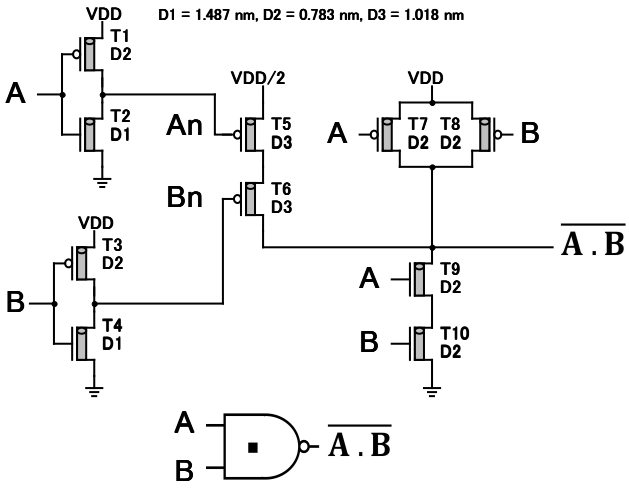

FIGURE 2—Transistor Level of the proposed $TNAND$.

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TABLE 4: The Disadvantage of Existing Logic gates in [13], [16], and [18] and the Advantage of proposed logic gates

Disadvantage	Advantage
Shown in Fig. A1 and A2 in the appendix The existing designs suffer from High power consumption due to:	Shown in Fig. 1 and 2 The proposed designs provide Low power consumption due to:
1- Two transistors that act as resistors in STI (T2, T3) and in $TNAND$ (T5, T6) [13]. 2- Two transistors that act as resistors in STI (T3, T6) and in $TNAND$ (T5, T10) [16]. 3- Two transistors that are always active in STI (T2, T3) and in $TNAND$ (T5, T6) [18].	Eliminating these two transistors by applying dual supply voltages (Vdd and Vdd/2).
4- For STI [13], [18]: Four transistors (T1, T2, T3, T4) in series must be active to get logic 1. 5- For STI [16]: Four transistors (T1, T3, T6, T5) in series must be active to get logic 1.	For the proposed STI: Only one transistor (T3) must be active to get logic 1.
6- For $TNAND$ [13], [18]: Five or Six transistors [(T1 or T2) or both, T5, T6, T7, T8)] in series must be active to get logic 1. 7- For $TNAND$ [16]: Five or Six transistors [(T1 or T2) or both, T5, T10, T8, T9)] in series must be active to get logic 1.	For the proposed $TNAND$: Two transistors (T5, T6) in series must be active to get logic 1.

TABLE 5: The chirality, diameter, and threshold voltage of the CNTs used in the proposed STI

CNFET Type	Chirality	Diameter	Vth
P-CNFET (T4)	(10, 0)	0.783nm	- 0.559V
P-CNFET (T1)	(19, 0)	1.487nm	- 0.289V
N-CNFET (T2,T5)	(10, 0)	0.783nm	0.559V
N-CNFET (T3)	(13, 0)	1.018nm	0.428V

TABLE 6: The detailed operation of STI of Fig. 1

Ternary Input A	**0 (0 V)**	**1 (0.45 V)**	**2 (0.9 V)**
P-CNFET T1	ON	ON	OFF
N-CNFET T2	OFF	OFF	ON
A_p	**2**	**2**	**0**
N-CNFET T3	ON	ON	OFF
P-CNFET T4	ON	OFF	OFF
N-CNFET T5	OFF	OFF	ON
Output $\overline{A}$	**2**	**1**	**0**

This section proposes a new design of $TDecoder$ with 9 transistors through replacing the $TNOR$ and the second NTI with a novel sub-circuit and a binary inverter respectively as represented in Fig. 3.

TABLE 7: The chirality, diameter, and threshold voltage of the CNTs used in the proposed $TNAND$

CNFET Type	Chirality	Diameter	Vth
P-CNFET (T1,T3,T7,T8)	(10, 0)	0.783nm	- 0.559V
P-CNFET (T5, T6)	(13, 0)	1.018nm	- 0.428V
N-CNFET (T9, T10)	(10, 0)	0.783nm	0.559V
N-CNFET (T2, T4)	(19, 0)	1.487nm	0.289V

Fig. 3 shows the transistor level design of the proposed $TDecoder$. It consists of one negative ternary inverter (NTI), one positive ternary inverter (PTI), one binary inverter, and a novel sub-circuit.

Table 9 shows the disadvantage of the existing $TDecoder$ in [13], [14], and [17] and the advantage of the proposed $TDecoder$.

The chirality, diameter, and threshold voltage (Vth) of the CNFETs used are shown in Table 11, and the detailed operation of the proposed circuit described in Table 12.

When the input X is logic 0, then transistors (T1, and T3) are turned ON and (T2, T4, and T7) are turned OFF. The output X_0 and the intermediate Y are equal to logic 2. Then (T5, and T8) are turned OFF and (T6, and T9) are turned ON.

TABLE 8: The detailed operation of $TNAND$ with selected inputs of Fig. 2

Ternary Inputs (A, B)	**(0, 0)**	**(0, 1)**	**(1, 1)**	**(1, 2)**
P-CNFET T1	ON	ON	OFF	OFF
N-CNFET T2	OFF	OFF	ON	ON
A_n	**2**	**2**	**0**	**0**
P-CNFET T3	ON	OFF	OFF	OFF
N-CNFET T4	OFF	ON	ON	ON
B_n	**2**	**0**	**0**	**0**
P-CNFET T5	OFF	OFF	ON	ON
P-CNFET T6	OFF	ON	ON	ON
P-CNFET T7	ON	ON	OFF	OFF
P-CNFET T8	ON	OFF	OFF	OFF
N-CNFET T9	OFF	OFF	OFF	OFF
N-CNFET T10	OFF	OFF	OFF	ON
Output $TNAND$	**2**	**2**	**1**	**1**

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TABLE 9: The Disadvantage of Existing $TDecoder$ in [13], [14], and [17] and the Advantage of proposed $TDecoder$

Disadvantage	Advantage
Shown in in Fig. A3 in the appendix The existing design suffers from High power consumption due to:	Shown in Fig. 3 The proposed design provides Low power consumption due to:
1- The Transistors' count of [13], [14], [17] equal to 16, 10, 11 respectively.	Transistors' count = 9.
2- To get X_1, [13] uses the Ternary NOR (10 transistors). 3- To get X_1, [14], [17] use the Binary NOR (4 transistors).	To get X_1, the design uses the novel sub-circuit (3 transistors) including the Transmission Gate (T7, T8) which provides low power consumption and propagation delay.
4- Six transistors (T11, T12, T13, T14, T15, T16) must be active to get X_1 equals to logic 2 [13]. 5- Two transistors (T9, T10) in series must be active to get logic X_1 equals to logic 2 [14], [17].	Only the Transmission Gate (T7, T8) must be active to get logic X_1 equals to logic 2.

TABLE 10: Ternary Decoder truth Table

Input	Outputs		
X	X_2	X_1	X_0
0	0	0	2
1	0	2	0
2	2	0	0

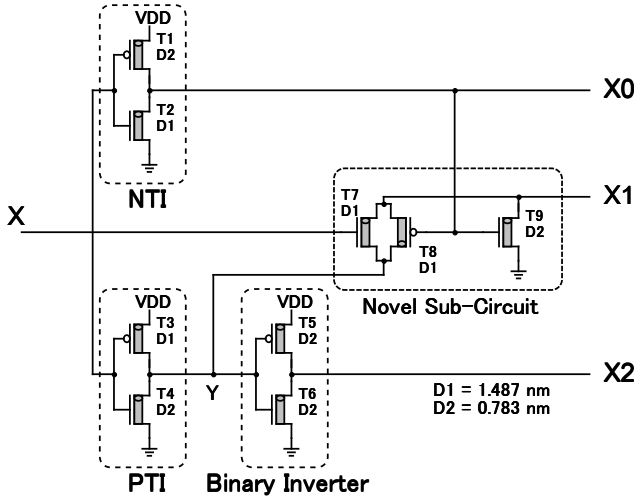

FIGURE 3—Transistor Level of the proposed $TDecoder$ with 9 CNFETs.

TABLE 11: The chirality, diameter, and threshold voltage of the CNTs used in the proposed $TDecoder$

CNFET Type	Chirality	Diameter	Vth
P-CNFET (T1, T5)	(10, 0)	0.783nm	- 0.559V
P-CNFET (T3, T8)	(19, 0)	1.487nm	- 0.289V
N-CNFET (T4, T6, T9)	(10, 0)	0.783nm	0.559V
N-CNFET (T2, T7)	(19, 0)	1.487nm	0.289V

TABLE 12: The detailed operation of the proposed $TDecoder$ of Fig. 3

Ternary Input X	**0 (0 V)**	**1 (0.45 V)**	**2 (0.9 V)**
P-CNFET T1	ON	OFF	OFF
N-CNFET T2	OFF	ON	ON
Output X_0	**2**	**0**	**0**
P-CNFET T3	ON	ON	OFF
N-CNFET T4	OFF	OFF	ON
Intermediate Y	**2**	**2**	**0**
P-CNFET T5	OFF	OFF	ON
N-CNFET T6	ON	ON	OFF
Output X_2	**0**	**0**	**2**
N-CNFET T7	OFF	ON	ON
P-CNFET T8	OFF	ON	ON
N-CNFET T9	ON	OFF	OFF
Output X_1	**0**	**Y=2**	**Y=0**

Therefore, the outputs X_1 and X_2 are equal to logic 0.

When the input X is logic 1, then transistors (T2, T3, and T7) are turned ON and (T1, and T4) are turned OFF. The output X_0 is equal to logic 0, and the intermediate Y is equal to logic 2. Then (T5, and T9) are turned OFF and (T6, and T8) are turned ON. Therefore, the output X_1 is equal to the value of Y which is logic 2 and the output X_2 is equal to logic 0.

Finally, when the input X is logic 2, then transistors (T2, T4, and T7) are turned ON and (T1, and T3) are turned OFF. The output X_0 and the intermediate Y are equal to logic 0. Then (T6, and T9) are turned OFF and (T5, and T8) are turned ON. Therefore, the output X_1 is equal to the value of Y which is logic 0, and the output X_2 is equal to logic 2.

B. PROPOSED TERNARY HALF ADDER

Ternary half adder (THA) is able to add two ternary inputs and provides two outputs: the Sum and the Carry. Table 13

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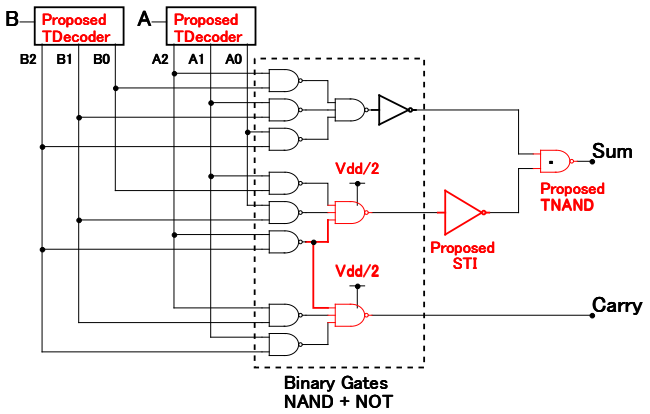

FIGURE 4—Proposed THA with 85 transistors.

shows the Karnaugh map of THA. The equations of sum and carry derived from Table 13 are (5) and (6) as follow:

TABLE 13: Karnaugh Map of THA

Sum

A/B	$B_0(0)$	$B_1(1)$	$B_2(2)$
$A_0(0)$	0	1	2
$A_1(1)$	1	2	0
$A_2(2)$	2	0	1

Carry

A/B	$B_0(0)$	$B_1(1)$	$B_2(2)$
$A_0(0)$	0	0	0
$A_1(1)$	0	0	1
$A_2(2)$	0	1	1

$$\begin{aligned} Sum = 2 \bullet (A_0B_2 + A_1B_1 + A_2B_0) \\ +1 \bullet (A_0B_1 + A_1B_0 + A_2B_2) \end{aligned} \tag{5}$$

$$Carry = 1 \bullet (A_1B_2 + A_2B_1 + A_2B_2) \tag{6}$$

Where A_k and B_k, are the outputs of the $TDecoder$ from inputs A and B respectively.

The existing THA in [13], [15], and [16] are shown in Fig. A4 in the appendix with 136, 112, and 112 transistors respectively.

This section proposes a new design of THA with 85 transistors using De Morgan's Law and dual power supply (Vdd and Vdd/2) to eliminate the encoder level shifter in [13], [15]. Also, it uses the proposed $TDecoder$ of Fig. 3, the proposed STI of Fig. 1 and the proposed $TNAND$ of Fig. 2, and removes one common $NAND$ as illustrate in Fig. 4.

Fig. 4 shows the proposed THA. It consists of two proposed $TDecoders$, eight 2-inputs binary $NAND$, three 3-inputs binary $NAND$, one binary inverter, one proposed $TNAND$, and one proposed STI.

Table 14 shows the total transistors' count of the proposed THA.

TABLE 14: Total transistors' count of the proposed THA

	No. of Devices	No. of Transistors	Subtotal*
Proposed $TDecoder$	2	9	18
Binary 2-$NAND$	8	4	32
Binary 3-$NAND$	3	6	18
Binary Inverter	1	2	2
Proposed STI	1	5	5
Proposed $TNAND$	1	10	10
Total			85

*Subtotal = No. of Devices x No. of Transistors

The operation of the proposed THA: Two ternary inputs A and B fed to the proposed $TDecoder$ and produce outputs as (A_2, A_1, A_0) and (B_2, B_1, B_0). These outputs will drive the eight 2-inputs binary $NAND$, the three 3-inputs binary $NAND$ logic gates, the proposed STI, binary inverter, and the proposed $TNAND$ to get the Sum and the Carry as final outputs.

C. PROPOSED TERNARY MULTIPLIER

Ternary multiplier ($TMUL$) is able to multiply two ternary inputs and provides two outputs: the Product and the Carry. Table 15 shows the Karnaugh map of $TMUL$. The equations of Product and Carry derived from Table 15 are (7) and (8) as follow:

TABLE 15: Karnaugh Map of $TMUL$

Product

A/B	$B_0(0)$	$B_1(1)$	$B_2(2)$
$A_0(0)$	0	0	0
$A_1(1)$	0	1	2
$A_2(2)$	0	2	1

Carry

A/B	$B_0(0)$	$B_1(1)$	$B_2(2)$
$A_0(0)$	0	0	0
$A_1(1)$	0	0	0
$A_2(2)$	0	0	1

$$\begin{aligned} Product = 2 \bullet (A_1B_2 + A_2B_1) \\ +1 \bullet (A_1B_1 + A_2B_2) \end{aligned} \tag{7}$$

$$Carry = 1 \bullet A_2B_2 \tag{8}$$

Where A_k and B_k, are the outputs of the $TDecoder$ from inputs A and B respectively.

The existing $TMUL$ in [13], [15], and [16] are shown in Fig. A5 in the appendix with 100, 86, and 76 transistors respectively.

This section proposes a new design of $TMUL$ with 61 transistors using De Morgan's Law and the dual power supply (Vdd and Vdd/2) to eliminate the encoder level shifter in [13], [15]. Also, it uses the proposed $TDecoder$ of Fig. 3, the

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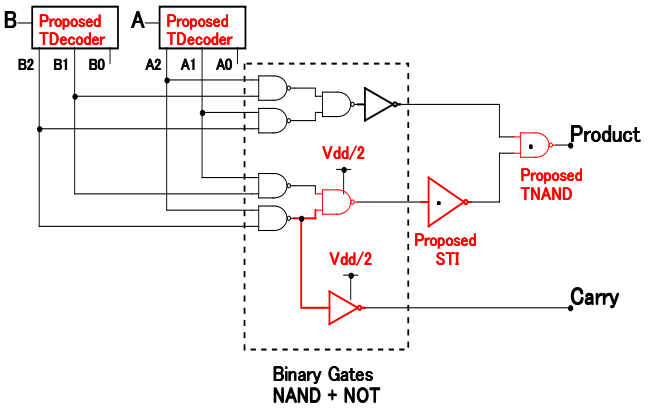

FIGURE 5—Proposed $TMUL$ with 61 transistors.

TABLE 16: Total transistors' count of the proposed $TMUL$

	No. of Devices	No. of Transistors	Subtotal*
Proposed $TDecoder$	2	9	18
Binary $NAND$	6	4	24
Binary Inverter	2	2	4
Proposed STI	1	5	5
Proposed $TNAND$	1	10	10
Total			61

*Subtotal = No. of Devices x No. of Transistors

proposed STI of Fig. 1 and the proposed $NAND$ of Fig. 2, and removes one common $NAND$ as illustrate in Fig. 5.

Fig. 5 shows the proposed $TMUL$. It consists of two proposed $TDecoders$, six binary $NAND$, two binary inverters, one proposed STI, and one proposed $TNAND$.

Table 16 shows the total transistors' count of the proposed $TMUL$.

The operation of the proposed $TMUL$: Two ternary inputs A and B fed to the proposed $TDecoders$ and produce outputs as (A_2, A_1, A_0) and (B_2, B_1, B_0). These outputs will drive the four 2-inputs binary $NAND$, the two 2-inputs binary $NAND$ logic gates, the proposed STI, the two binary inverters, and the proposed $TNAND$ to get the Product and the Carry as final outputs.

V. SIMULATION RESULTS AND COMPARISONS

As mentioned in the Introduction that CNFET provides better energy efficiency compared to CMOS, FinFET, and other transistor technologies [19].

Therefore, the proposed STI, $TNAND$, $TDecoder$, THA, and $TMUL$ are simulated and compared to CNFET-Based ternary circuits in [13]–[18].

All the twenty circuits are extensively simulated and tested using the HSPICE simulator with 32-nm channel length for different power supplies (0.8 V, 0.9 V, 1 V), different temperatures (10°C , 27°C , 70°C), and different frequencies (0.5 GHz, 1 GHz, 2 GHz).

One hundred eighty simulations are performed to study the performance and efficiency of the proposed five circuits in the separate sections below.

TABLE 17: Some of CNFET Model Parameters

	Description	Value
L_{ch}	Physical channel length	32 nm
L_{geff}	The mean free path in the intrinsic CNT	100 nm
L_{ss} (L_{dd})	The length of doped CNT source-side (drain-side) extension region	10 nm
Efi	The Fermi level of the doped S/D tube	0.6 eV
K_{gate}	The dielectric constant of high-k top gate dielectric material (planer gate)	4
T_{ox}	The thickness of the high-k top gate dielectric material (planer gate)	1 nm
C_{sub}	The coupling capacitance between the channel region and the substrate	10 pF/m
C_{csd}	The coupling capacitance between the channel region and the source/drain region	0 pF/m
$Pitch$	The distance between two adjacent CNTs within the same device	20 nm
$Tubes$	The number of tubes in the device	1

Although CNFET-based circuit may suffer performance changes due to device variability, this effect has not been considered in this work.

Table 17 shows some essential parameters of the CNFET model used in all the circuits with brief descriptions.

All input signals have a rise and fall time of 20 ps. The propagation delay of the circuit is measured, for example, for t_1 as shown in Fig. 8, when the input (X) is rising from 0 to 1, and the output (X_0) is falling from 2 to 0. A similar procedure is done to get all possible rising and falling propagation delays for outputs of all studied circuits and find the maximum propagation delay for each circuit.

Then the average power consumption, maximum propagation delay, and maximum power delay product (PDP) are obtained for all circuits.

The performance of the five proposed circuits will be compared to other designs for the Power-Delay Product PDP (energy consumption).

A. TRANSIENT ANALYSIS OF PROPOSED CIRCUITS

Fig. 6 – 10 illustrate the transient analysis of the proposed STI, $TNAND$, $TDecoder$, THA, and $TMUL$ respectively.

B. COMPARISON OF TRANSISTORS' COUNT

The minimization of transistors' count is not the only factor that affects the performance of the proposed circuits, but it is

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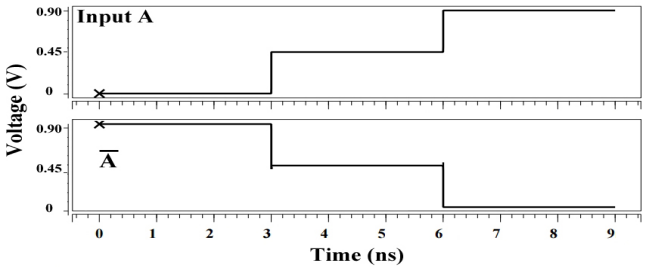

FIGURE 6—Transient analysis of the proposed STI.

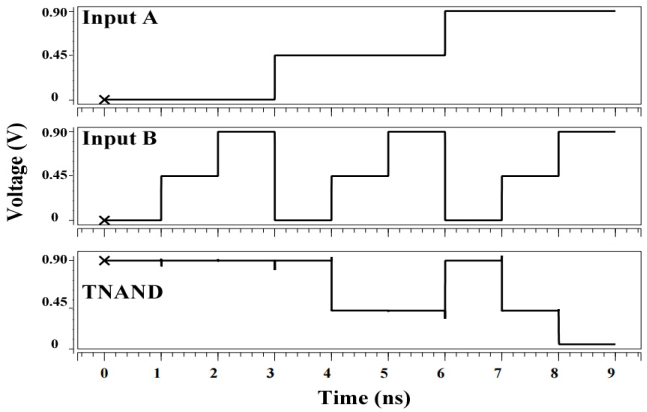

FIGURE 7—Transient analysis of the proposed $TNAND$.

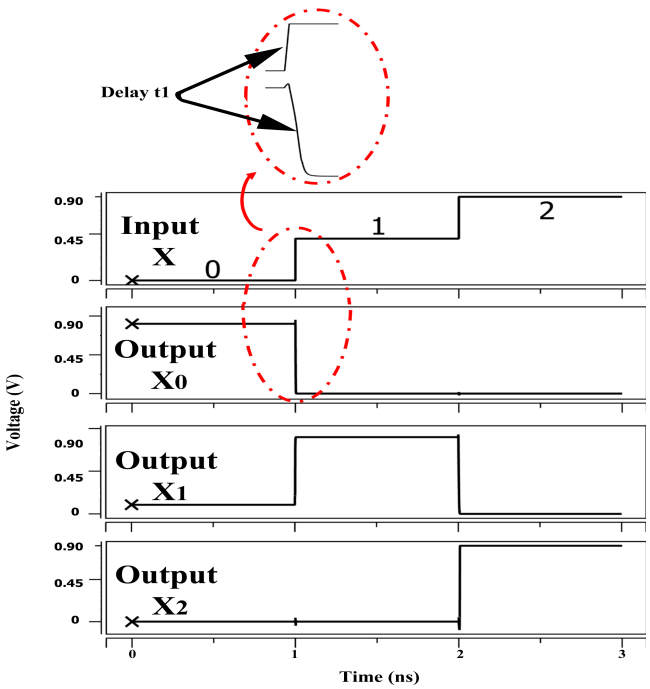

FIGURE 8—Transient analysis of the proposed $TDecoder$.

a good factor. The other factors are described in the following subsections.

Table 18 shows the comparison of transistors' count for STI, $TNAND$, $TDecoder$, THA, and $TMUL$ compared

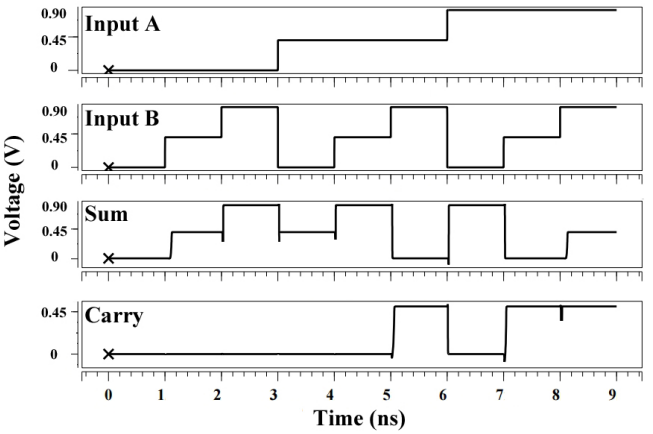

FIGURE 9—Transient analysis of the proposed THA.

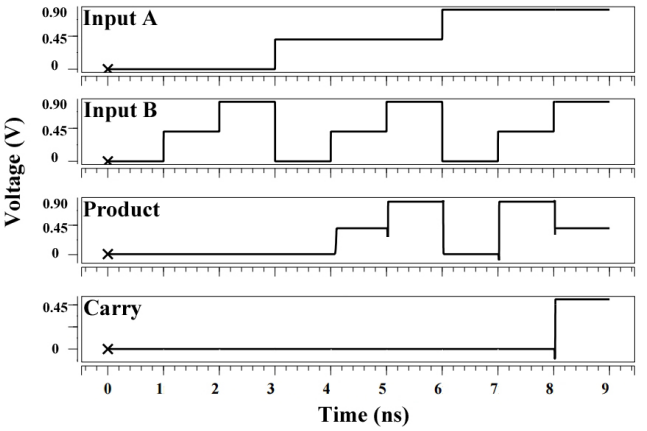

FIGURE 10—Transient analysis of the proposed $TMUL$.

TABLE 18: Comparison of Transistors' Count of All Circuits

	[13]	[16]	[15]	[18]	[17]	[14]	Proposed
STI	6	6	–	6	–	–	**5**
$TNAND$	10	10	–	10	–	–	**10**
$TDecoder$	16	–	–	–	11	10	**9**
THA	136	112	112	–	–	–	**85**
$TMUL$	100	76	86	–	–	–	**61**

to [13]–[18].

This comparison of the proposed circuits demonstrates a notable reduction in transistors' count. For STI, around 16.67% compared to STI in [13], [16], and [18]. For $TNAND$, around 0% compared to $TNAND$ in [13], [16], and [18]. For $TDecoder$, around 43.75%, 10%, and 18.18% compared to $TDecoder$ in [13], [14], and [17] respectively. For THA, around 37.5%, 24.11%, and 24.11% compared to THA in [13], [15], and [16] respectively. For $TMUL$, around 39%, 29.07%, and 19.74% compared to $TMUL$ in [13], [15], and [16] respectively.

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C. COMPARISON OF DIFFERENT STI CIRCUITS

Fig. 11 shows the PDP Comparison of the investigated STI for (a) Different Power Supplies, (b) Different Temperatures, and (c) Different Frequencies.

1) Impact of Different Power Supplies

The effect of different power supplies (0.8 V, 0.9 V, 1 V) on the performance metrics of all proposed circuits is studied.

Simulation is done at 1 GHz operating frequency and room temperature at 27°C as illustrated in Fig. 11 (a).

The comparison of the proposed STI demonstrates a notable reduction in PDP as shown in Fig. 11 (a). For Vdd=0.8 V, around 28.33%, 88.68%, and 80.37% compared to [13], [16], and [18] respectively. For Vdd=0.9 V, around 61.22%, 83.95%, and 86.38% compared to [13], [16], and [18] respectively. For Vdd=1 V, around 30.42%, 68.98%, and 74.05% compared to [13], [16], and [18] respectively.

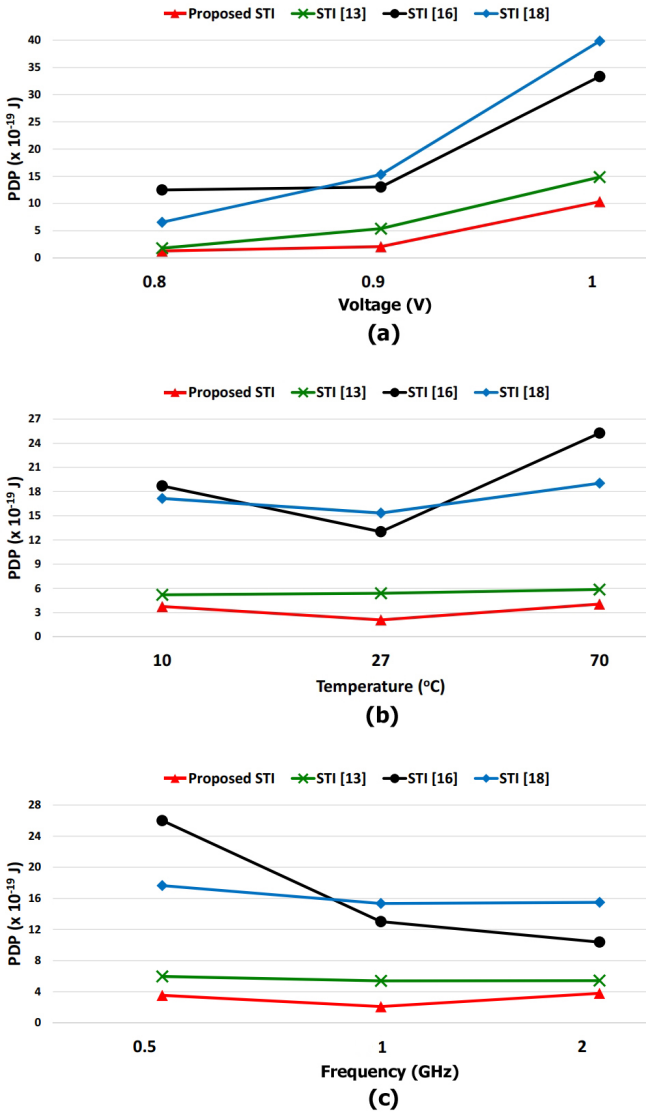

FIGURE 11—PDP Comparison of the investigated STI for: (a) Different Power Supplies, (b) Different Temperatures, and (c) Different Frequencies.

2) Impact of Different Temperatures

Temperature noise is one of the most critical issues which negatively affect the performance of the circuit.

The effect of different temperatures (10°C, 27°C, 70°C) on the performance metrics of all proposed circuits is studied. Simulation is done at 1 GHz operating frequency, and power supply Vdd equals 0.9 V as illustrated in Fig. 11 (b).

The comparison of the proposed STI demonstrates a notable reduction in PDP as shown in Fig. 11 (b). For Temperature=10°C, around 27.88%, 79.95%, and 78.15% compared to [13], [16], and [18] respectively. For Temperature=27°C, around 61.22%, 83.95%, and 86.38% compared to [13], [16], and [18] respectively. For Temperature=70°C, around 30.89%, 83.96%, and 78.73% compared to [13], [16], and [18] respectively.

3) Impact of Different Frequencies

Electronic circuits behave very differently at high frequencies because due to a change in the behavior of passive components (resistors, inductors, and capacitors) and parasitic effects on active components, PCB tracks and grounding patterns at high frequencies.

Recently, High-frequency operation is a demand for electronic devices.

The effect of different frequencies (0.5 GHz, 1 GHz, 2 GHz) on the performance metrics of all proposed circuits is studied. Simulation is done at power supply Vdd equals 0.9 V, and temperature equals 27°C as illustrated in Fig. 11 (c).

The comparison of the proposed STI demonstrates a notable reduction in PDP as shown in Fig. 11 (c). For frequency=0.5 GHz, around 40.60%, 86.38%, and 79.93% compared to [13], [16], and [18] respectively. For frequency=1 GHz, around 61.22%, 83.95%, and 86.38% compared to [13], [16], and [18] respectively. For frequency=2 GHz, around 30.20%, 63.45%, and 75.52% compared to [13], [16], and [18] respectively.

D. COMPARISON OF DIFFERENT TNAND CIRCUITS

Fig. 12 shows the PDP Comparison of the investigated $TNAND$ for (a) Different Power Supplies, (b) Different Temperatures, and (c) Different Frequencies.

1) Impact of Different Power Supplies

Simulation is done at 1 GHz operating frequency and room temperature at 27°C as illustrated in Fig. 12 (a).

The comparison of the proposed $TNAND$ demonstrates a notable reduction in PDP as shown in Fig. 12 (a). For Vdd=0.8 V, around 32.53%, 99.64%, and 90.07% compared to [13], [16], and [18] respectively. For Vdd=0.9 V, around 69.22%, 93.73%, and 94.35% compared to [13], [16], and [18] respectively. For Vdd=1 V, around 44.6%, 79.27%, and 98.3% compared to [13], [16], and [18] respectively.

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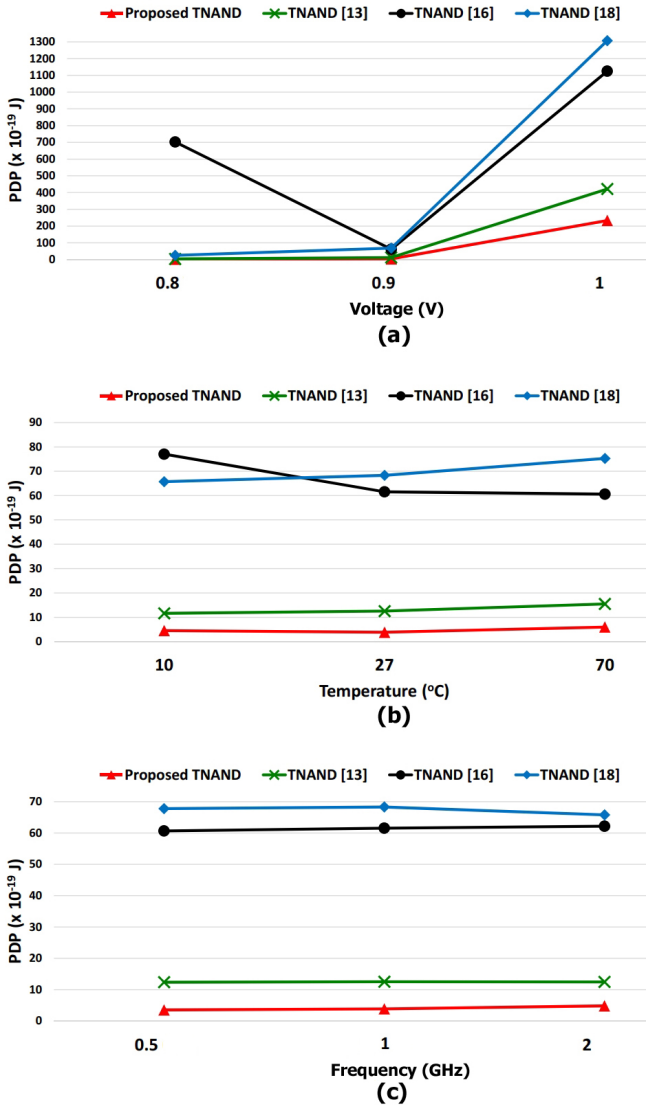

FIGURE 12—PDP Comparison of the investigated $TNAND$ for: (a) Different Power Supplies, (b) Different Temperatures, and (c) Different Frequencies.

2) Impact of Different Temperatures

The effect of different temperatures (10°C, 27°C, 70°C) on the performance metrics of all proposed circuits is studied.

Simulation is done at 1 GHz operating frequency, and power supply Vdd equals 0.9 V as illustrated in Fig. 12 (b).

The comparison of the proposed $TNAND$ demonstrates a notable reduction in PDP as shown in Fig. 12 (b). For Temperature=10°C, around 60.88%, 94.09%, and 93.08% compared to [13], [16], and [18] respectively. For Temperature=27°C, around 69.22%, 93.73%, and 94.35% compared to [13], [16], and [18] respectively. For Temperature=70°C, around 61.34%, 90.13%, and 92.06% compared to [13], [16], and [18] respectively.

3) Impact of Different Frequencies

The effect of different frequencies (0.5 GHz, 1 GHz, 2 GHz) on the performance metrics of all proposed circuits is studied.

Simulation is done at power supply Vdd equals 0.9 V, and temperature equals 27°C as illustrated in Fig. 12 (c).

The comparison of the proposed $TNAND$ demonstrates a notable reduction in PDP as shown in Fig. 12 (c). For frequency=0.5 GHz, around 71.46%, 94.18%, and 94.79% compared to [13], [16], and [18] respectively. For frequency=1 GHz, around 69.22%, 93.73%, and 94.35% compared to [13], [16], and [18] respectively. For frequency=2 GHz, around 61.27%, 92.23%, and 92.66% compared to [13], [16], and [18] respectively.

E. COMPARISON OF DIFFERENT TDECODER CIRCUITS

1) Impact of Different Power Supplies

Table 19 shows the comparison to the existing Ternary Decoder in [13], [14], and [17] in terms of the average power consumption, maximum propagation delay, and maximum energy (PDP) for different supply voltages (0.8 V, 0.9 V, 1 V), same temperature (27°C), and same frequency (1 GHz). The boldface values are the best values among others.

The comparison of the proposed Ternary Decoder demonstrates a notable reduction in PDP as shown in Table 19. For Vdd=0.8 V, around 54.01%, 23.64%, and 98.85% compared to [13], [14], and [17] respectively. For Vdd=0.9 V, around 47.91%, 19.8%, and 98.86% compared to [13], [14], and [17] respectively. For Vdd=1 V, around 60.7%, 48.17%, and 97.74% compared to [13], [14], and [17] respectively.

2) Impact of Different Temperatures

Table 20 shows the comparison to the existing Ternary Decoder in [13], [14], and [17] in terms of the average power consumption, maximum propagation delay, and maximum energy (PDP) for different temperatures (10°C, 27°C, 70°C), same supply voltage Vdd (0.9 V), and same frequency (1 GHz).

The comparison of the proposed Ternary Decoder demonstrates a notable reduction in PDP as shown in Table 20. For Temperature=10°C, around 46.82%, 24.62%, and 98.27% compared to [13], [14], and [17] respectively. For Temperature=27°C, around 47.91%, 19.8%, and 98.86% compared to [13], [14], and [17] respectively. For Temperature=70°C, around 44.29%, 18%, and 98.5% compared to [13], [14], and [17] respectively.

3) Impact of Different Frequencies

Table 21 shows the comparison to the existing Ternary Decoder in [13], [14], and [17] in terms of the average power consumption, maximum propagation delay, and maximum energy (PDP) for different frequencies (0.5 GHz, 1 GHz, 2 GHz), same temperatures (27°C), and same supply voltage Vdd (0.9 V).

The comparison of the proposed Ternary Decoder demonstrates a notable reduction in PDP as shown in Table 21. For

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TABLE 19: Comparison of Average Power (μw), Maximum Delay (ps), and Maximum PDP (x10^{-19} J) of 4 $TDecoders$ with T=27°C, F=1 GHz, and for different supply voltages

	Vdd=0.8 V			Vdd=0.9 V			Vdd=1 V		
	Power	Delay	PDP	Power	Delay	PDP	Power	Delay	PDP
TDecoder [13]	2.6	10.4	2.74	3.5	8.91	3.11	11.8	8.24	9.72
TDecoder [14]	1.9	8.50	1.65	2.7	7.50	2.02	10.4	7.06	7.37
TDecoder [17]	126	8.67	109.24	185	7.68	142.08	250	7.18	168.73
Proposed TDecoder	**1.9**	**6.59**	**1.26**	**2.6**	**6.26**	**1.62**	**9.1**	**4.18**	**3.82**

TABLE 20: Comparison of Average Power (μw), Maximum Delay (ps), and Maximum PDP (x10^{-19} J) of 4 $TDecoders$ with Vdd=0.9 V, F=1 GHz, and for Different Temperatures

	Temp.=10°C			Temp.=27°C			Temp.=70°C		
	Power	Delay	PDP	Power	Delay	PDP	Power	Delay	PDP
TDecoder [13]	5.1	9.18	4.72	3.5	8.91	3.11	4.4	8.31	3.68
TDecoder [14]	4.3	7.7	3.33	2.7	7.50	2.02	3.5	7.05	2.50
TDecoder [17]	184	7.89	145.17	185	7.68	142.08	189	7.20	136.72
Proposed TDecoder	**4**	**6.4**	**2.51**	**2.6**	**6.26**	**1.62**	**3.5**	**5.85**	**2.05**

TABLE 21: Comparison of Average Power (μw), Maximum Delay (ps), and Maximum PDP (x10^{-19} J) of 4 $TDecoders$ with T=27°C, Vdd=0.9 V, and for different frequencies

	f= 2 GHz			f= 1 GHz			f= 0.5 GHz		
	Power	Delay	PDP	Power	Delay	PDP	Power	Delay	PDP
TDecoder [13]	6.0	8.93	5.17	3.5	8.91	3.11	2.3	8.91	2.11
TDecoder [14]	4.1	7.54	3.12	2.7	7.50	2.02	2.0	7.5	1.46
TDecoder [17]	185	7.7	142.24	185	7.68	142.08	184	7.68	142.08
Proposed TDecoder	**4**	**6.25**	**2.44**	**2.6**	**6.26**	**1.62**	**1.8**	**6.26**	**1.17**

frequency=2 GHz, around 52.8%, 21.79%, and 98.28% compared to [13], [14], and [17] respectively. For frequency=1 GHz, around 47.91%, 19.8%, and 98.86% compared to [13], [14], and [17] respectively. For frequency=0.5 GHz, around 44.55%, 19.86%, and 99.18% compared to [13], [14], and [17] respectively.

F. COMPARISON OF DIFFERENT THA CIRCUITS

Fig. 13 shows the PDP Comparison of the investigated THA for (a) Different Power Supplies, (b) Different Temperatures, and (c) Different Frequencies.

1) Impact of Different Power Supplies

Simulation is done at 1 GHz operating frequency and room temperature at 27°C as illustrated in Fig. 13 (a).

The comparison of the proposed THA demonstrates a notable reduction in PDP as shown in Fig. 13 (a). For Vdd=0.8 V, around 86.16%, 72.53%, and 64.55% compared to [13], [15], and [16] respectively. For Vdd=0.9 V, around 73.43%, 61.24%, and 49.97% compared to [13], [15], and [16] respectively. For Vdd=1 V, around 76.75%, 72.82%, and 62.85% compared to [13], [15], and [16] respectively.

2) Impact of Different Temperatures

The effect of different temperatures (10°C, 27°C, 70°C) on the performance metrics of all proposed circuits is studied.

Simulation is done at 1 GHz operating frequency, and power supply Vdd equals 0.9 V as illustrated in Fig. 13 (b).

The comparison of the proposed THA demonstrates a notable reduction in PDP as shown in Fig. 13 (b). For Temperature=10°C, around 68.97%, 58.08%, and 42.78% compared to [13], [15], and [16] respectively. For Temperature=27°C, around 73.43%, 61.24%, and 49.97% compared to [13], [15], and [16] respectively. For Temperature=70°C, around 69.58%, 59.51%, and 46.28% compared to [13], [15], and [16] respectively.

3) Impact of Different Frequencies

The effect of different frequencies (0.5 GHz, 1 GHz, 2 GHz) on the performance metrics of all proposed circuits is studied.

Simulation is done at power supply Vdd equals 0.9 V, and temperature equals 27°C as illustrated in Fig. 13 (c).

The comparison of the proposed THA demonstrates a notable reduction in PDP as shown in Fig. 13 (c). For frequency=0.5 GHz, around 74.4%, 66.04%, and 55.94% compared to [13], [15], and [16] respectively. For frequency=1 GHz, around 73.43%, 61.24%, and 49.97% compared to [13], [15], and [16] respectively. For frequency=2 GHz, around 72.01%, 60.22%, and 48.4% compared to [13], [15], and [16] respectively.

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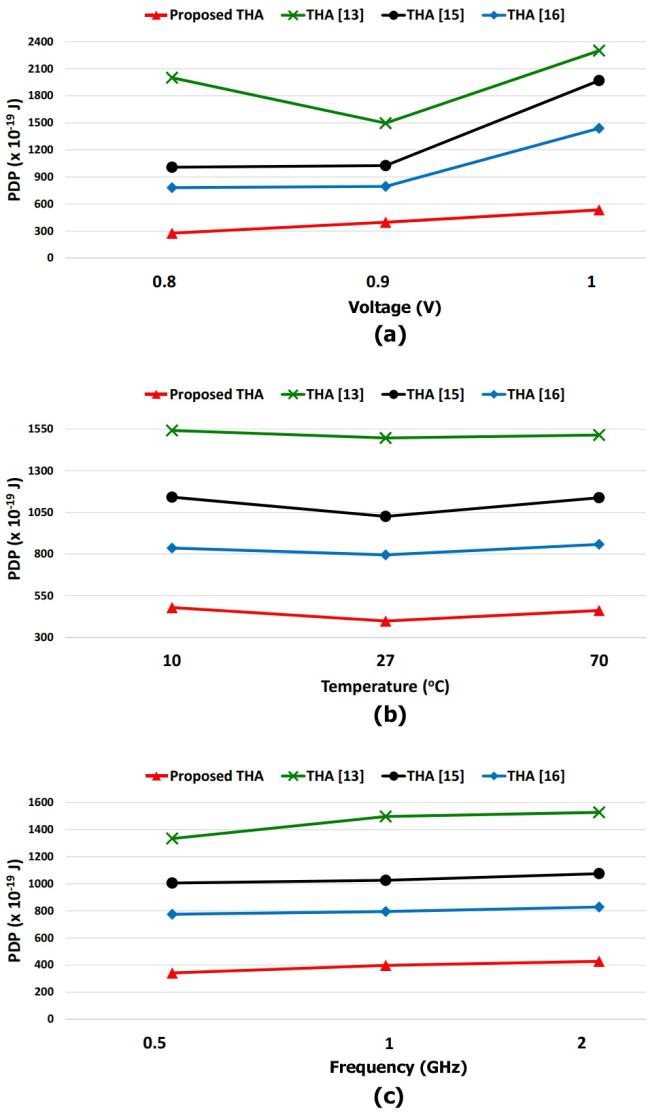

FIGURE 13—PDP Comparison of the investigated THA for: (a) Different Power Supplies, (b) Different Temperatures, and (c) Different Frequencies.

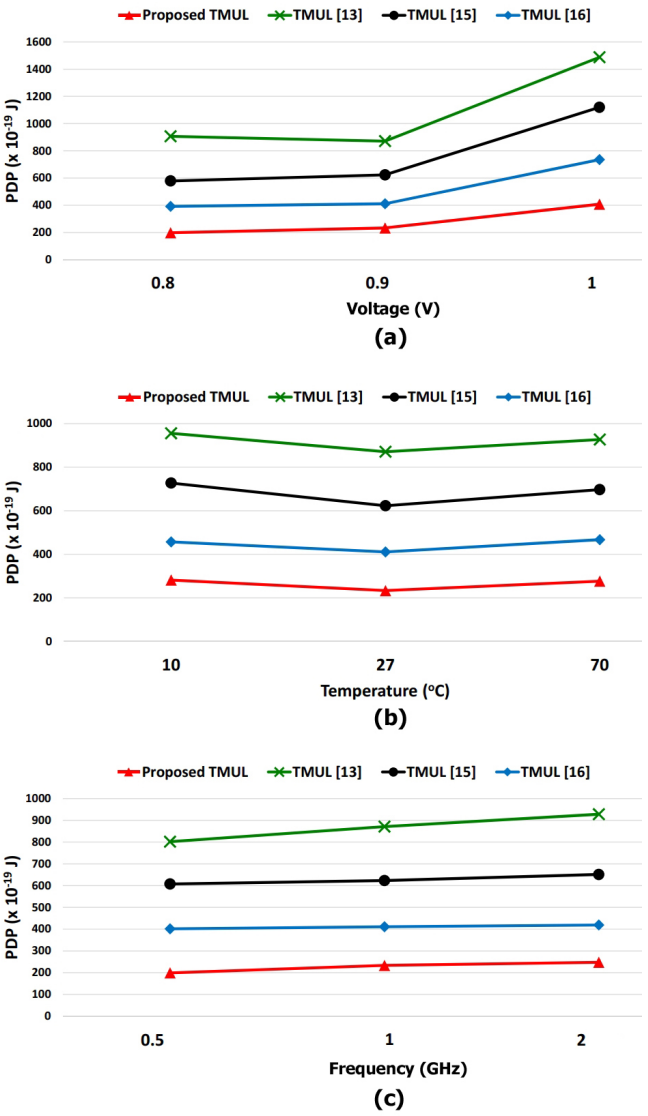

FIGURE 14—PDP Comparison of the investigated $TMUL$ for: (a) Different Power Supplies, (b) Different Temperatures, and (c) Different Frequencies.

G. COMPARISON OF DIFFERENT TMUL CIRCUITS

Fig. 14 shows the PDP Comparison of the investigated $TMUL$ for (a) Different Power Supplies, (b) Different Temperatures, and (c) Different Frequencies.

1) Impact of Different Power Supplies

Simulation is done at 1 GHz operating frequency and room temperature at 27°C as illustrated in Fig. 14 (a).

The comparison of the proposed $TMUL$ demonstrates a notable reduction in PDP as shown in Fig. 14 (a). For Vdd=0.8 V, around 78.16%, 65.77%, and 49.49% compared to [13], [15], and [16] respectively. For Vdd=0.9 V, around 73.19%, 62.52%, and 43.19% compared to [13], [15], and [16] respectively. For Vdd=1 V, around 72.58%, 63.58%, and 44.55% compared to [13], [15], and [16] respectively.

2) Impact of Different Temperatures

The effect of different temperatures (10°C, 27°C, 70°C) on the performance metrics of all proposed circuits is studied.

Simulation is done at 1 GHz operating frequency, and power supply Vdd equals 0.9 V as illustrated in Fig. 14 (b).

The comparison of the proposed $TMUL$ demonstrates a notable reduction in PDP as shown in Fig. 14 (b). For Temperature=10°C, around 70.51%, 61.25%, and 38.36% compared to [13], [15], and [16] respectively. For Temperature=27°C, around 73.19%, 62.52%, and 43.19% compared to [13], [15], and [16] respectively. For Temperature=70°C, around 70.17%, 60.32%, and 40.82% compared to [13], [15], and [16] respectively.

3) Impact of Different Frequencies

The effect of different frequencies (0.5 GHz, 1 GHz, 2 GHz) on the performance metrics of all proposed circuits is studied.

Simulation is done at power supply Vdd equals 0.9 V, and temperature equals 27°C as illustrated in Fig. 14 (c).

The comparison of the proposed $TMUL$ demonstrates a notable reduction in PDP as shown in Fig. 14 (c). For frequency=0.5 GHz, around 75.15%, 67.2%, and 50.38% compared to [13], [15], and [16] respectively. For frequency=1 GHz, around 73.19%, 62.52%, and 43.19% compared to [13], [15], and [16] respectively. For frequency=2 GHz, around 73.31%, 61.97%, and 40.91% compared to [13], [15], and [16] respectively.

The **advantage** of all proposed circuits is that they have the lowest PDP among all investigated circuits for different supply voltages, temperatures, and frequencies. Therefore, they are more suitable for low-power portable electronics and embedded systems to save battery consumption.

VI. CONCLUSION

This paper proposed new designs for the Standard Ternary Inverter, Ternary NAND, Ternary Decoder, Ternary Half Adder, and Ternary Multiplier that aim to keep high-performance levels and energy efficiency.

The design process tried to optimize several circuit techniques such as reducing the number of used transistors, utilizing energy-efficient transistor arrangements, and applying the dual supply voltages (Vdd and Vdd/2).

The proposed ternary circuits are compared to the latest fifteen ternary circuits, simulated and tested using HSPICE simulator under various operating conditions with different supply voltages, different temperatures, and different frequencies.

One hundred eighty simulations are performed to prove the efficiency of the proposed designs. The results prove the merits of the approach in terms of reduced energy consumption (PDP) compared to other existing designs.

Therefore, the proposed circuits can be implemented in low-power portable electronics and embedded systems to save battery consumption.

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APPENDIX. INVESTIGATED CIRCUITS FROM THE LITERATURE.

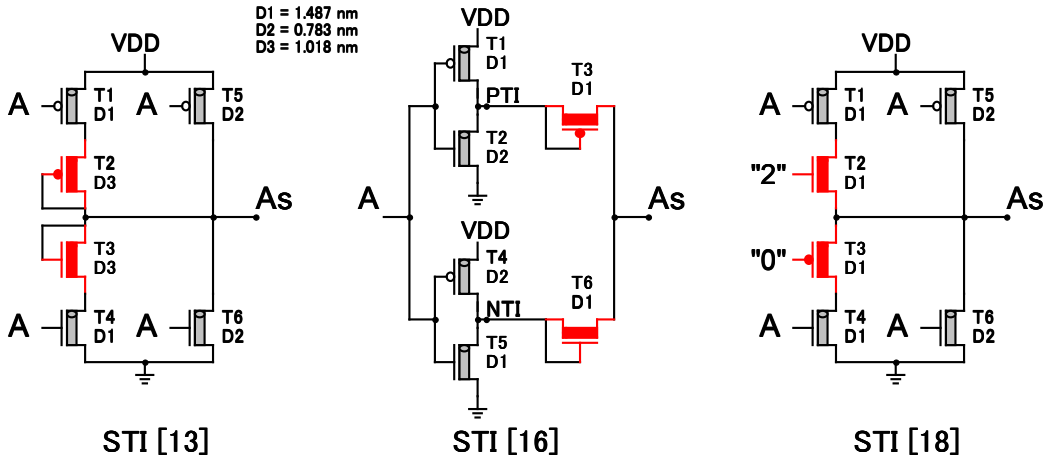


FIGURE A1—Existing STI in (a) [13], (b) [16], and (c) [18].

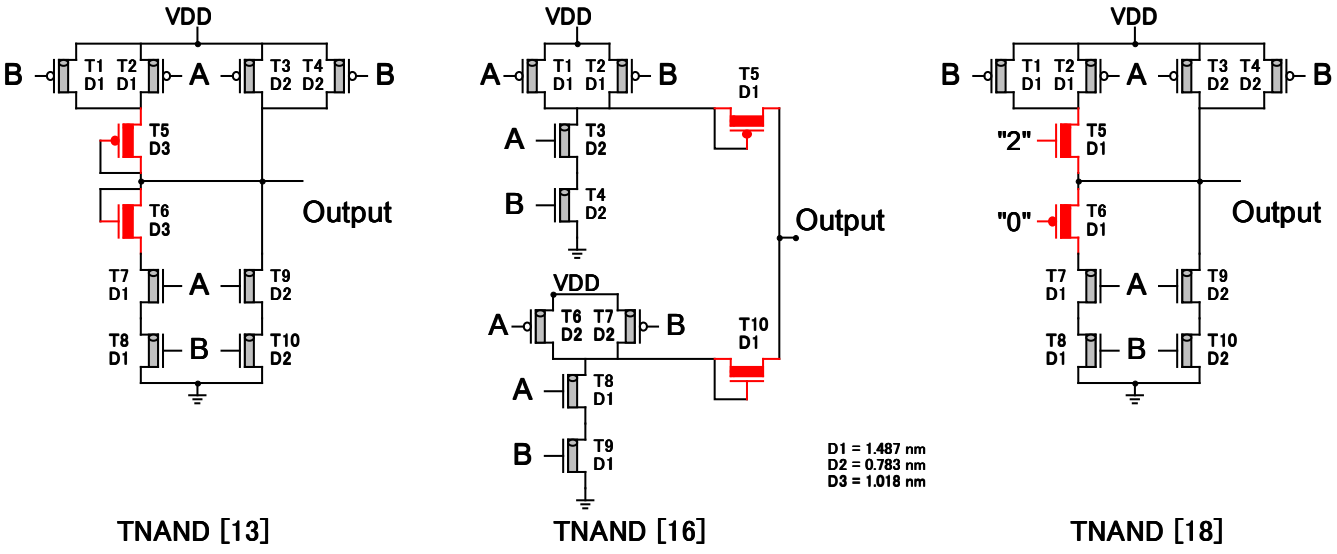
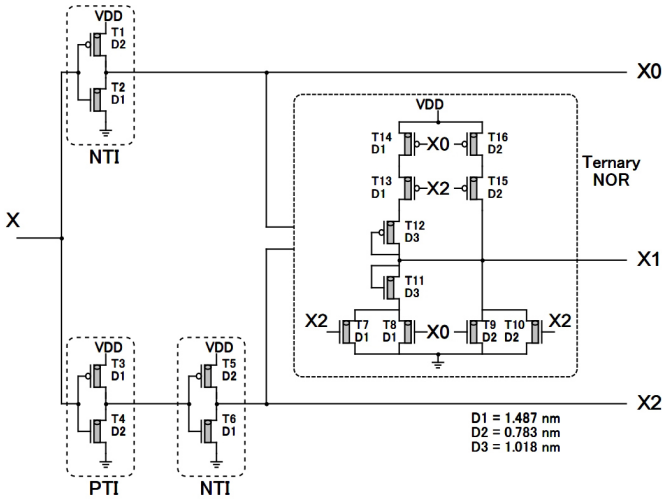
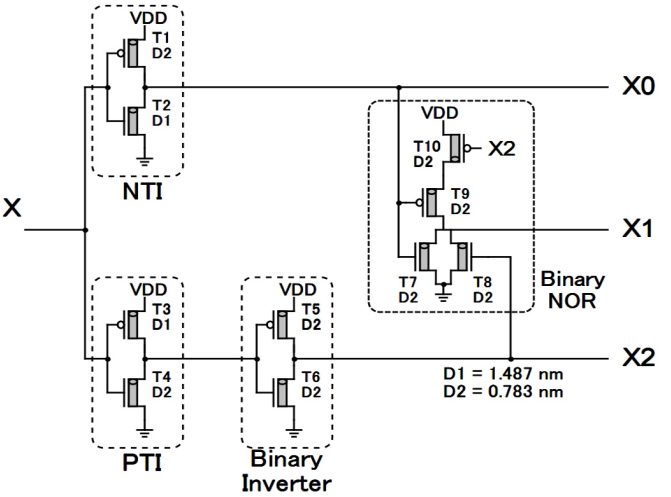


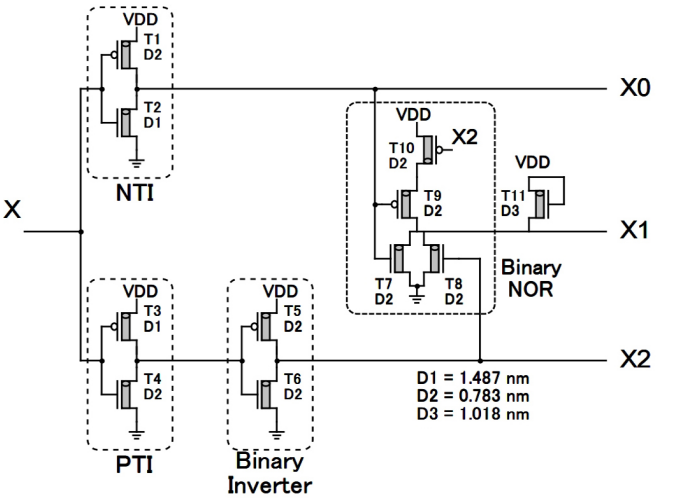
FIGURE A2—Existing $TNAND$ in (a) [13], (b) [16], and (c) [18].



(a) TDECODER [13] with 16 Transistors



(b) TDECODER [14] with 10 Transistors



(c) TDECODER [17] with 11 Transistors

FIGURE A3—Existing $TDecoder$ in (a) [13], (b) [14], and (c) [17].

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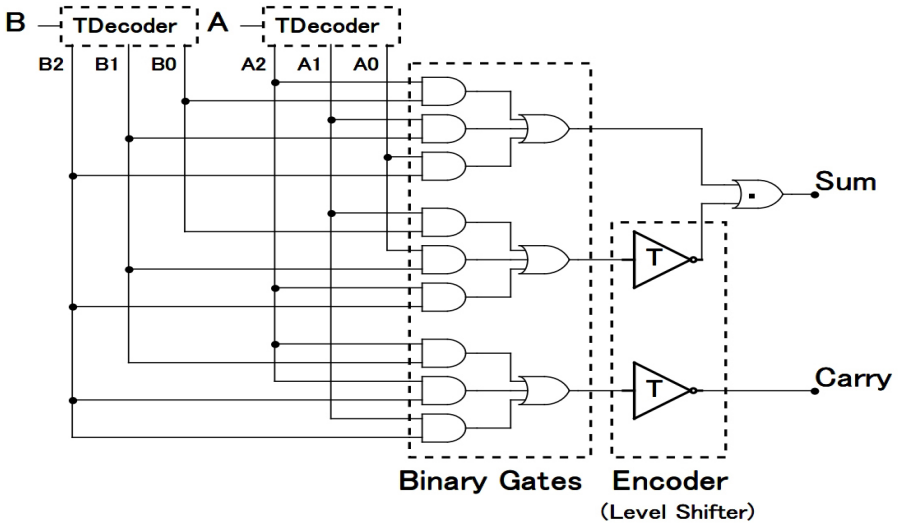
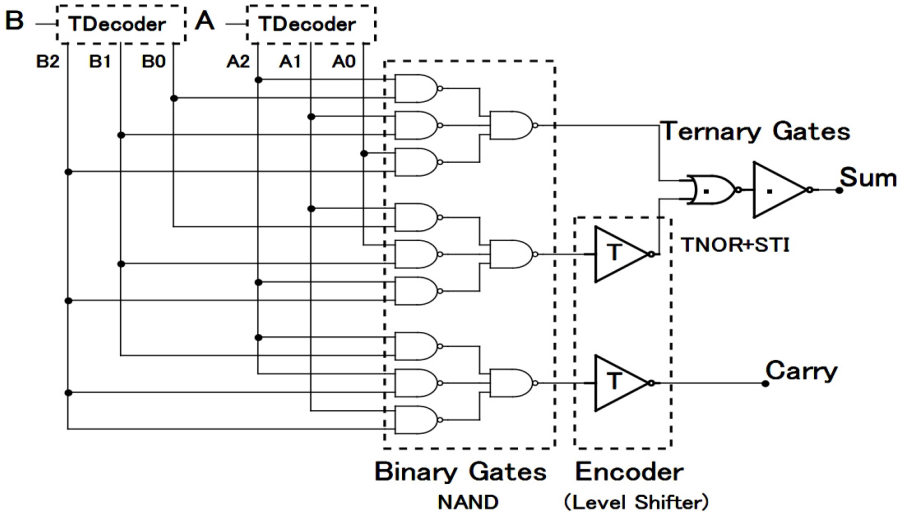
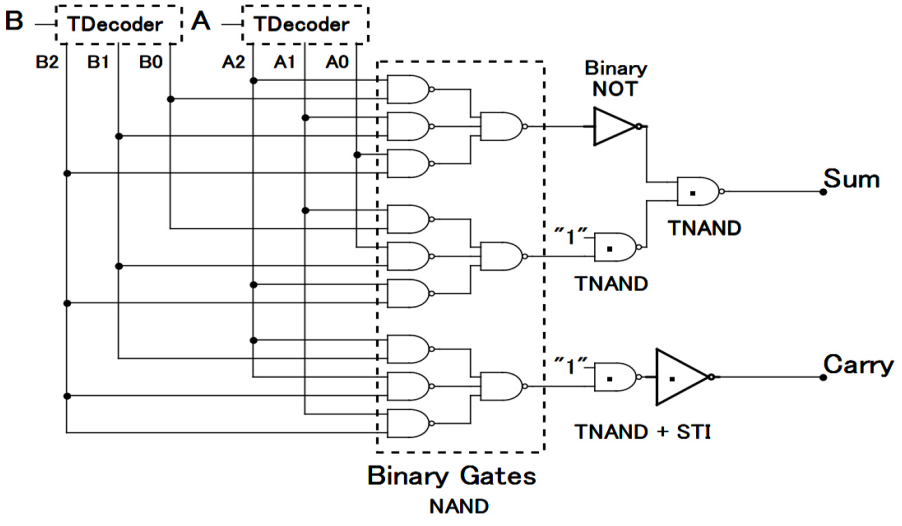


(a) THA [13] with 136 transistors



(b) THA [15] with 112 transistors



(c) THA [16] with 112 transistors

FIGURE A4—Existing THA in (a) [13], (b) [15], and (c) [16].

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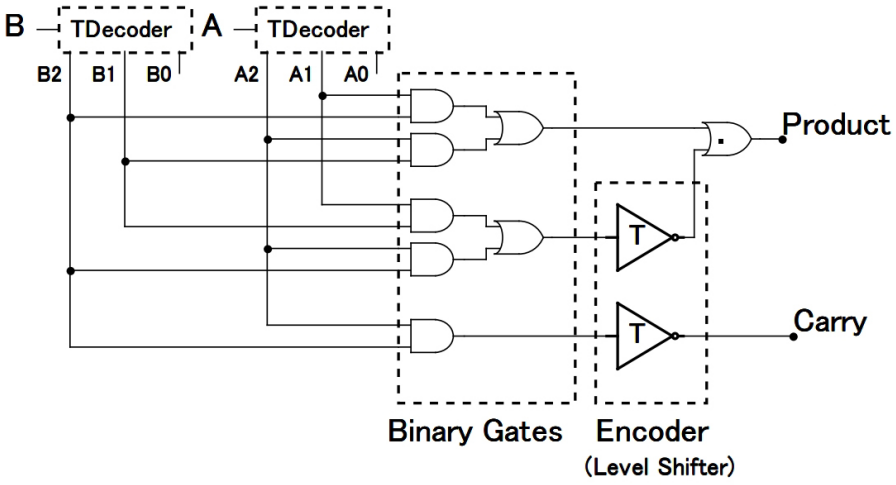
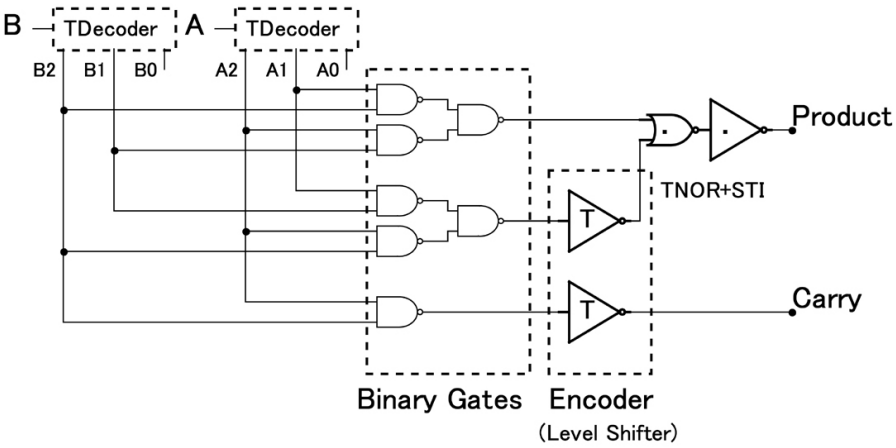
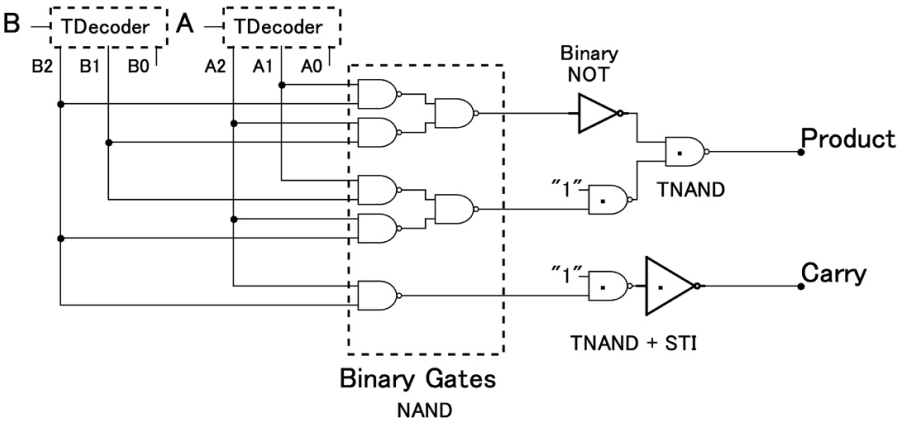


(a) TMUL [13] With 100 Transistors



(b) TMUL [15] With 86 Transistors



(c) TMUL [16] With 76 Transistors

FIGURE A5—Existing $TMUL$ in (a) [13], (b) [15], and (c) [16].

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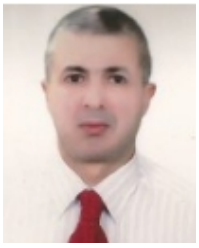
RAMZI A. JABER (S' 19) received the B.E. (Hons.) degree in Computer & Electrical Engineering and the Master's degree in Computer Engineering & Informatics from the Beirut Arab University, B.A.U in 2001 and 2010 respectively. He is currently working toward the Ph.D. degree in Computer & Electrical Engineering at B.A.U. From 2002 to 2006, he taught at different High Schools at Lebanon. From 2006 to 2010, he taught as Lab Instructors in the Faculty of Computer Sciences at Lebanese University. From 2006 to 2019, he taught as Lab Instructors and Lecturer in the Computer & Electrical Engineering department at Beirut Arab University (BAU). His current research interests include high-performance and energy-efficient digital circuit design, as well as high-speed low-power Very Large-Scale Integrated (VLSI) circuit design and Multiple-Valued Logic (MVL). He is a CCNA (Cisco Certified Network Associate) Instructor since 2011.



ABDALLAH KASSEM (S'98–M'02–SM'11) received his B.S. in Microelectronics from the University of Quebec in Montreal in 1992, his M.Sc. and Ph.D. in microelectronics from Ecole Polytechnique de Montreal in 1996 and 2004 respectively. From 1996 to 2000, he taught some courses and laboratories, as an instructor, in his field at AUB, LAU in Lebanon. Dr. Kassem joined Notre Dame University in Lebanon as an assistant professor in the Electrical and Computer Engineering department. He was promoted to the rank of associate professor in 2011. Dr. Kassem published approximately 60 papers in reviewed journals and conference proceedings in Lebanon and around the world. He is an Associate Editor in IEEE ACCESS, a Guest Editor Elsevier, AEU - International Journal of Electronics and Communications. Dr. Kassem was a member of the organizing committee of many international conferences sponsored or technically co-sponsored by IEEE (DINWC 2018, EBECEGC 2018, ICM, ICABME, MECBME, ACTEA, ICDIPC 2016, EECEA 2016, DICTAP 2015, TAEECE 2015, ICABME 2015, ICeND2014, MELECON). Dr. Kassem was invited as a keynote speaker in some conferences and workshops. His research interests include microelectronics design and testing, VLSI, semiconductor device modeling and simulation, microprocessors, engineering education/management, ultrasonic applications, healthcare applications, biomedical system design, smart medical devices e-Health, and m-Health.

AHMAD M. EL-HAJJ (S'05–M'16) is an Assistant Professor in the communications and electronics program and the coordinator of the biomedical engineering program at Beirut Arab University. He received his B.E, M.E and Ph.D. degrees in electrical and computer engineering from the American University of Beirut in 2007, 2009 and 2014, respectively. His research interests include wireless network optimization, radio network planning, game theory, neuro-engineering, biomimetics, and bioinformatics. Dr. El-Hajj also serves as a member of the executive committee of the IEEE-Lebanon section and the local chapter of the IEEE Communications Society (IEEE ComSoc).

LINA A. EL-NIMRI received her Diploma in Computer Engineering from Leningrad Electrotechnical Institute (LETI) in 1983. From 1983 till 1989 she worked as an analyst, programmer and system administrator in several companies where she developed business applications and applications for production and analysis purposes. Later, in 1994, she obtained her Ph.D. in technical sciences "Computers, Complexes and Systems" from Saint-Petersburg Electrotechnical University (ETU). While conducting her Ph.D. research, she was also working at the university's computer laboratory where she designed and programmed a parametric system for the simulation of processes and their interactions. She has taught in the following universities: "Beirut Arab University" BAU, "Institute Supérieur des Sciences Appliquées et Économiques" (ISAE-Cnam Liban), "Islamic University of Lebanon" IUL, and since 1999 she has been, and continues to be, an associate professor at the "Lebanese University". Her scientific interests and teaching experiences are focused on the following areas: Simulation, Logic Design, Operating Systems, Compilation theory, Database theory, Programming Languages, System Analysis and Design, Web development, Web services, Multimedia, Big Data, and Information retrieval. Besides teaching, she has advised and supervised many students in their graduation projects and master's theses.

ALI MASSOUD HAIDAR received his B.S in Electrical Engineering (Electronics & Telecommunications) from Beirut Arab University in 1986, his M.E degree in Computer and Information Engineering from Faculty of Engineering, University of the Ryukyus, Japan in 1992 and his Ph.D. in Computer Engineering from Department of Computer and Information Engineering, Faculty of Engineering, Saitama University, Japan in 1995. He joined Hiroshima City University in April 1995 as an Assistant Professor. Then, he joined Beirut Arab University in October 1997, where he is currently a Professor in the Department of Electrical and Computer Engineering. His scientific interests are; Logic Theory and its Applications, Neural Networks, Petri Nets, Cloud Computing, Digital Communication, and Smart Grids. He published approximately 100 papers in reviewed journals and conference proceedings. He has supervised around 25 graduate students (Master and Ph.D.).