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A Study of Ternary Fuzzy Processor Using Neural Networks

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Abstract—

A novel ternary fuzzy processor using the logic oriented neural networks is proposed, and the simulation results are illustrated to show how a ternary fuzzy inference engine can be realized by taking into consideration of advantages of neural networks. The principle to construct a ternary processor using the neural networks is described in detail and the simulation results for a novel Max circuit which is the essential circuit of the fuzzy inference engine are given. The features of the proposed processor are capability of high speed operation, and very simple construction with less number of elements to perform a function of fuzzy processor.

I. Introduction

Multiple-valued logic circuits have been watched with keen interests because they have a possibility to achieve a high circuit density and to perform a high performance operation with reduction of interconnection problems[1]. In this paper, a ternary fuzzy processor taking into consideration of these advantages of multiple-valued logic circuits is proposed. Although the fuzzy processors have been constructed with the common LSI[2], the ternary fuzzy processor proposed here is built with the Logic Oriented (LOGO) neural networks[3]. One of the features of the LOGO neural networks is a capability of high performance operation with simple construction of less number of elements. Therefore, we propose a novel ternary neural network to develop a ternary fuzzy processor. The principles of the ternary LOGO neural networks as well as the ternary fuzzy processor are described in detail. In digital fuzzy processor, there exist four main circuits including inference engine. The inference engine among these circuits is the key function to process the input data, which is performed by combination of the Max and Min circuits. In this paper we describe a 3-trit ternary Max circuits by using LOGO neural networks which are implemented with the current-mode MOSFET[5]. In order to verify the function of Max circuit simulations have been made by SPICE program. The results of simulations show that the Max function can be realized with a satisfactory performance of reduction of numbers of transistors and wiring.

II. Ternary LOGO neural networks

The expression of ternary number considered here is represented as

$$(t_n 3^n + t_{n-1} 3^{n-1} + \cdots + t_1 3^1 + t_0)$$

where $t_n \in \{1, 0, \bar{1}\}$, and $\{1, 0, \bar{1}\}$ is the set of 3-valued logic system which is called as the signed ternary logic. LOGO neural networks are fundamentally simple feed-forward processors as same as common neural networks, and are composed of processing elements of neuron and weighted connections between neurons. Their characteristics are defined as follows:

(1) The threshold values of neuron are integers.
(2) The input and output values of neuron are integers.
(3) The values of multiplication coefficient of "weight" are integers.

In order to realize the ternary fuzzy processor proposed here, two types of neurons in LOGO neural networks are used. One of them is "one-threshold type" and the other "two-thresholds type." Fig. 1(a) shows the symbol of one-threshold type neuron, while Fig. 1(b) indicates the input/output characteristics of the neuron. In the figure, x_i is the input signal, w_i is the weight value between neurons, θ is the threshold value and y is the output signal, respectively. Similarly, Fig. 2(a) and (b) show the symbol and the input/output characteristics of two-thresholds type neuron. The behaviors of these neurons are represented by following expressions.

(1) for one-threshold type neuron

$$y = \begin{cases} 0 & Z \le \theta \\ 1 & Z > \theta \end{cases} \tag{1}$$

(2) for two-thresholds type neuron

$$y = \begin{cases} -1 & Z < -\theta \\ 0 & -\theta \le Z \le \theta \\ 1 & Z > \theta \end{cases} \tag{2}$$

where $Z = \sum_{i=1}^{n} w_i x_i$.

The ternary logic operation for the neural networks can be performed by using "two-threshold type neuron".

III. Fuzzy inference engine

Fuzzy processor consists of four main circuits shown in Fig. 3. Fig. 4 shows a schematic diagram of the inference process by using membership functions, where two rules for the inference are considered. These two rules for inference are represented by following formula,

$$\begin{array}{l} \text{if } [x \text{ is } A_1] \text{ and } [y \text{ is } B_1] \text{ then } [z \text{ is } C_1] \\ \text{if } [x \text{ is } A_2] \text{ and } [y \text{ is } B_2] \text{ then } [z \text{ is } C_2] \end{array} \tag{3}$$

where A_1, B_1, A_2 and B_2 are the assumption for fuzzy inference, and C_1 and C_2 are the conclusion. In actual

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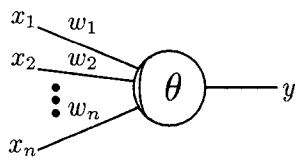
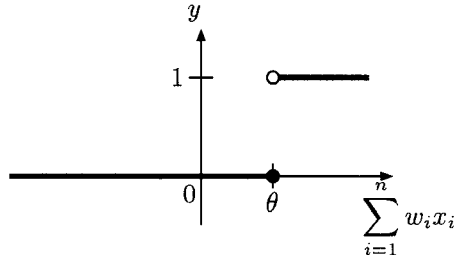
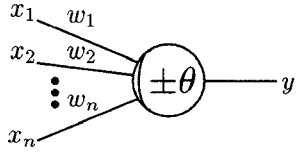


(a) One threshold type neuron.

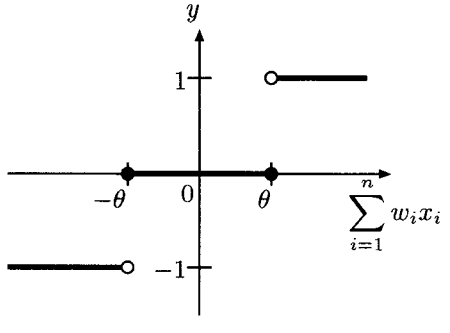


(b) Input/output characteristics.

Fig. 1. The symbol of one-threshold type neuron and its input/output characteristics.



(a) Two thresholds type neuron.



(b) Input/output characteristics.

Fig. 2. The symbol of two-thresholds type neuron and its input/output characteristics.

process of the inference engine, the fuzzy premise of A' is obtained instead of A. A fitness between A and A' is defined by using the so-called membership function. In this study, a membership function is expressed as a set of 27 singletons shown in Fig. 5. Each singleton is expressed as 3-trit data from (000) to (111). For example, the singleton

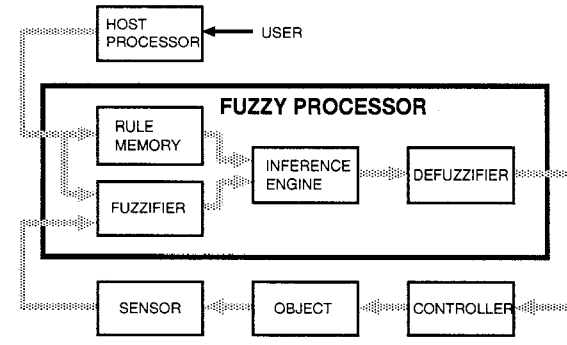


Fig. 3. Fuzzy processor and inference flow.

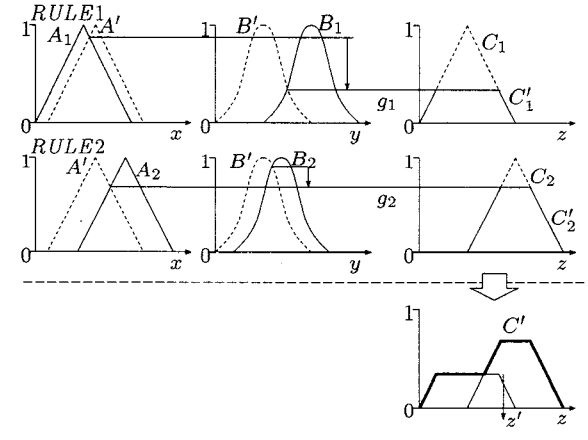


Fig. 4. Schematic diagram of the fuzzy inference process by using membership functions.

S_{15} is represented as the value $(11\bar{1})$.

In order to develop a fuzzy inference engine, it is required to construct Max circuits as well as Min circuits. Fig. 6 shows the block diagram of a fuzzy inference engine with 20 rules. The intersection circuit in the figure plays a role to perform the logical product of two membership functions. It consists of 27 Max circuits. The climax circuit selects

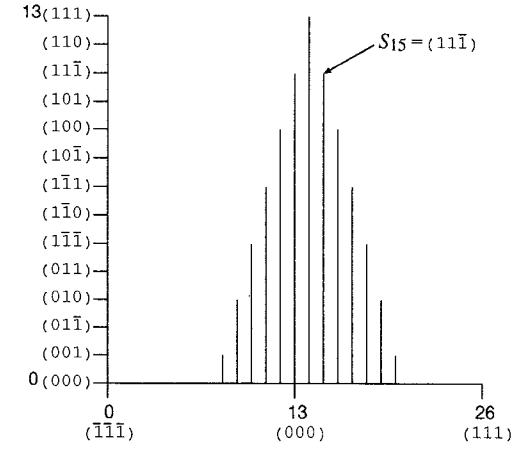


Fig. 5. A membership function as a set of singletons.

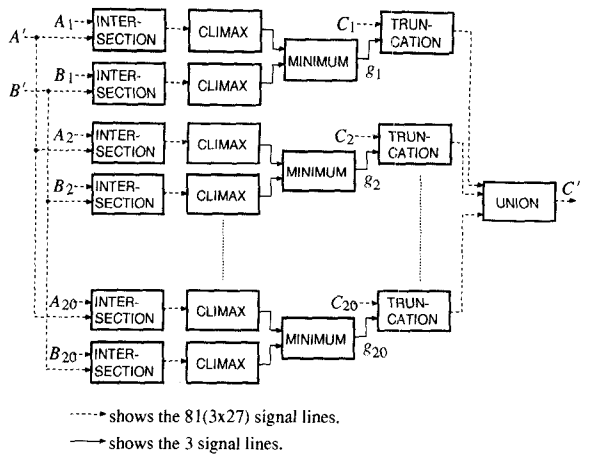


Fig. 6. The block diagram to realize the fuzzy inference engine with 20 rules.

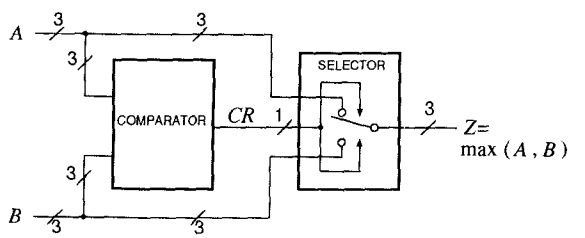


Fig. 7. The block diagram of Max circuit where $A = (a_2 a_1 a_0)$, $B = (b_2 b_1 b_0)$

the top grade of a membership function. This circuit also consists of 27 Max circuits. The truncation circuit executes a truncation of a membership function. It consists of 27 Min circuits. The union circuit performs the logical sum of membership functions. It consists of a set of similar circuits to the climax circuits, with total 513 Max circuits.

Fig. 7 shows a block diagram of Max circuit, which consists of a comparator and a data-selector. The comparator compares two 3-trit ternary input data (A and B) and produces a 1-trit CR output signal corresponding to the relation between inputs as shown in Table I. This function of comparator can be constructed by LOGO neural networks as shown in Fig. 8. The symbol of "o" in the figure shows that the value of weight is -1. The data-selector circuit produces either data of A or B corresponding to the condition that CR is $\bar{1}$, 0 or 1. Fig. 9 shows a 1-trit data-selector circuit using LOGO neural networks. Thus, a Max circuit can be constructed as shown in Fig. 10. In the similar way, Min circuit can be easily constructed by using LOGO neural networks as shown in Fig. 11.

In order to construct the Max circuit, we have developed a LOGO neural networks by using MOSFET. After designing the Max circuit as shown in Fig. 10 using current mode MOSFETs which are based on the 0.5μm design rules, we have investigated by SPICE program how the Max circuit can be performed.

Fig. 12 shows one example of simulation results. It is

TABLE I

RELATIONS BETWEEN INPUT SIGNAL AND OUTPUT SIGNAL OF CR

condition for inputs	CR
$A < B$	$\bar{1}$
$A = B$	0
$A > B$	1

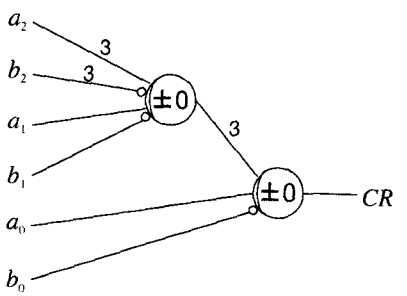


Fig. 8. Comparator circuit by using LOGO neural networks.

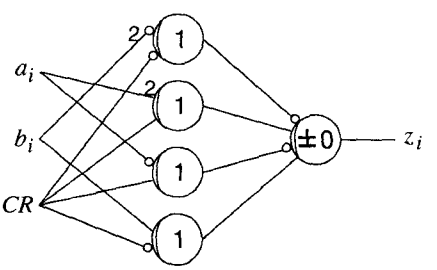


Fig. 9. 1-trit data-selector circuit by using LOGO neural networks.

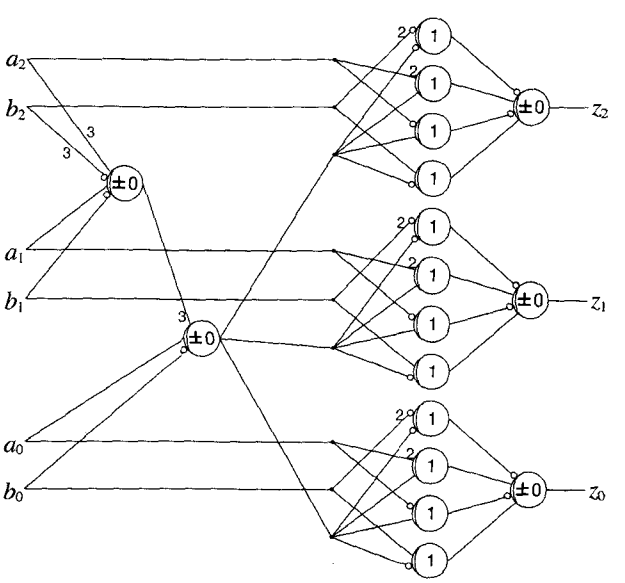


Fig. 10. Max circuit by using LOGO neural networks.

clear from these results that the reliable operation of Max circuit are obtained. The delay time of the operation is

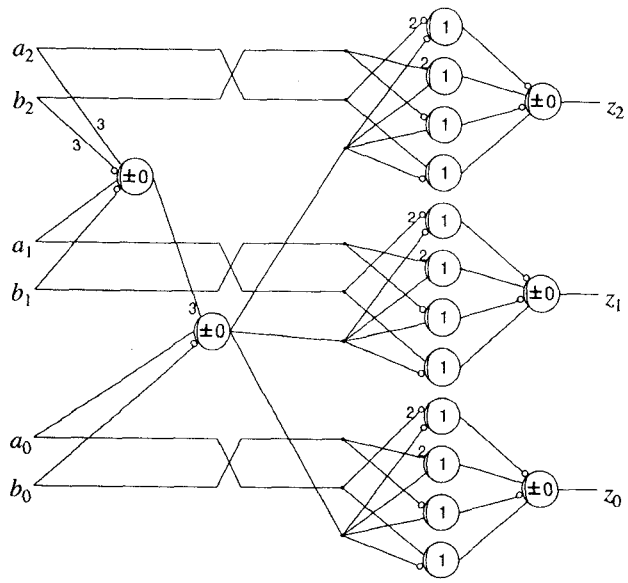


Fig. 11. Min circuit by using LOGO neural networks.

8.6ns. Furthermore we have made simulation for a fuzzy inference engine which has 3233 Max/Min circuits for two input data and twenty rules. The simulation results show that the ternary fuzzy inference engine can reduce the total number of wiring to 63% and does the total number of transistors to 89%, comparing the binary logic fuzzy inference engine.

IV. Conclusion

A novel ternary fuzzy inference engine by using LOGO neural networks has been proposed. The principle of the fuzzy inference engine, especially how the Max circuit can be implemented with LOGO neural networks, has been described. In order to verify the Max circuit which is a key circuit of the inference engine, we have made simulations of Max circuit with satisfaction. Moreover, we have made simulations for fuzzy inference engine with 3233 Max/Min circuit. From these results, it is clear the ternary fuzzy inference engine has a advantage of reduction of numbers of wiring and transistors over the common binary fuzzy inference engine.

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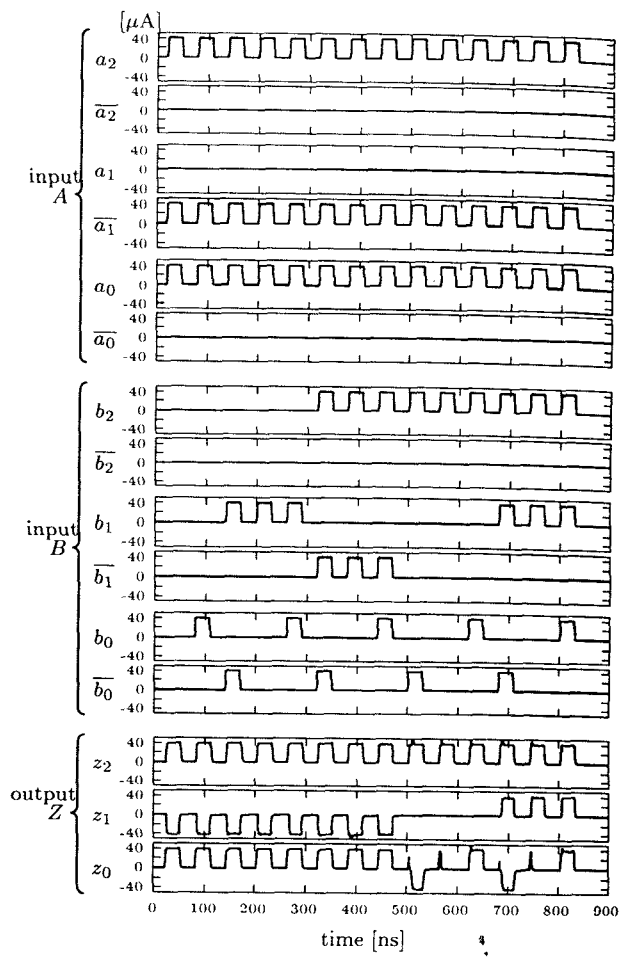

Fig. 12. One example of simulation results of the proposed Max circuit.