PROFESSOR‘S NOTES

10.1 TRANSISTOR CIRCUITS

The transistor is a component that acts as a ’transfer–resistance’, or ’trans–resistance’, and is the why of it being named “transistor”. It is a component which exercises control over a low–conductance output path. In an electronic circuit, the transistor is usually placed in series with other conductive components between an upper voltage supply rail and a lower voltage supply rail, and is then used to control the flow of current through this path. Control is exercised by a third node external to the conductance path, much like the generic form shown by figure 10.1–1(a). This control of current flow can be interpreted as if it were a dependent current source, defined by a bias between two input terminals. For small increments (small–signals), the control is nearly linear, and we can interpret the *small–signal* operation as if Mr. transistor were a *linearly–dependent* current source. Then all of the simplifications of linear network analysis can be applied to give us a reasonable sense of how the transistor can be used to define and drive a linear amplifier.

Figure 10.1–1(a) represents a generic transistor. This symbol is for conceptual use only, but it is a reasonable approximation of a real transistor. It is a *three–terminal* device, with two of the terminals associated with a conductance path and the third terminal associated with control. The conductance path being controlled lies between terminals B and C. The bias between terminals A and B controls the output current level I_C. In general, node B is common to both input control and to the output conductance path, as indicated.

In order that bias V_{AB} define the current level independently of output bias V_{BC}, it is necessary that the transistor be biased to operate in the ’active regime’, as indicated by figure 10.1–1(b). In the active regime the level of current I_C is set by bias V_{AB} and is approximately a constant for all V_{BC} except V_{BC} low.

When the transistor is operated in the active mode, terminal C is a *dependent* node. Variations in V_C have very little effect on the current level, so that this node serves as a relatively ’stiff’ current source. Because of its stiffness, node C is the favored choice as an output node.

Terminal B also can serve as output node since it is on the output path. But it is not as stiff as terminal C since a variation in V_B will have a strong effect on I_C. Terminal A is not used as an output terminal since it is not along the output path.

Note that when the transistor is in the active regime as represented by figure 10.1–1(b), the current level is a constant with respect to V_{BC}. Therefore the slope (= conductance) = 0, which is exactly the behavior of an ideal current source.

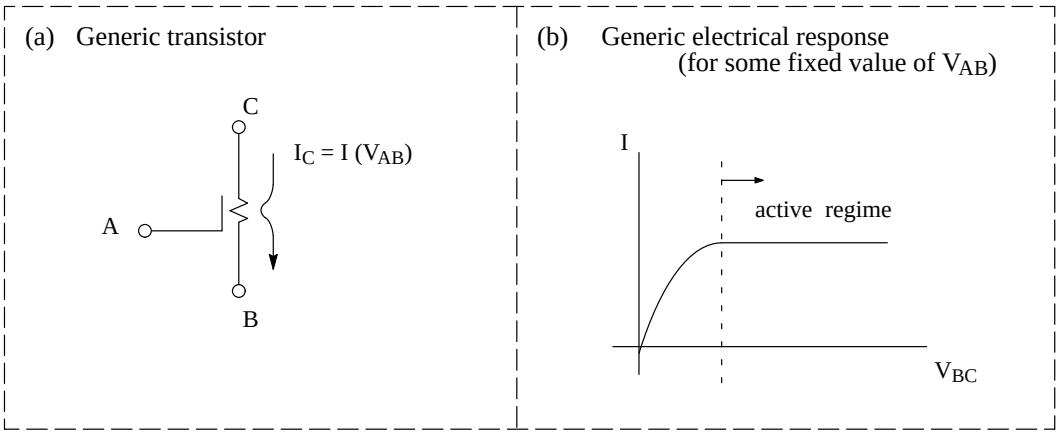


Figure 10.1–1: Transistor as a dependent current source

For use of the transistor as a an amplifier, we have to think of it as a voltage–to–current transducer (VCT), as represented by figure 10.1–2. In this case the VCT is a real device, and so I_C is will not be linear with respect to V_{AB}. Output current I_C could be dependent on $(V_{AB})^2$, or it could be exponential with respect to V_{AB}, or it could be a Mazzola function with respect to V_{AB}, – whatever. But for a small increment in level, we can assume that it is approximately linear. In fact circuit simulation software assumes that it is linear, then readjusts it as the calculation is updated with each iteration.

As an ideal element, the VCT is characterized by an output 'signal' current i_C that is controlled by 'signal' voltage v_{AB} , according to:

$$i_C = g_m v_{AB} \qquad (10.1\text{–}1)$$

where the transfer parameter from control voltage v_{AB} and the output signal i_C current is of the form of a "transfer conductance", or *transconductance*, usually designated as g_m.

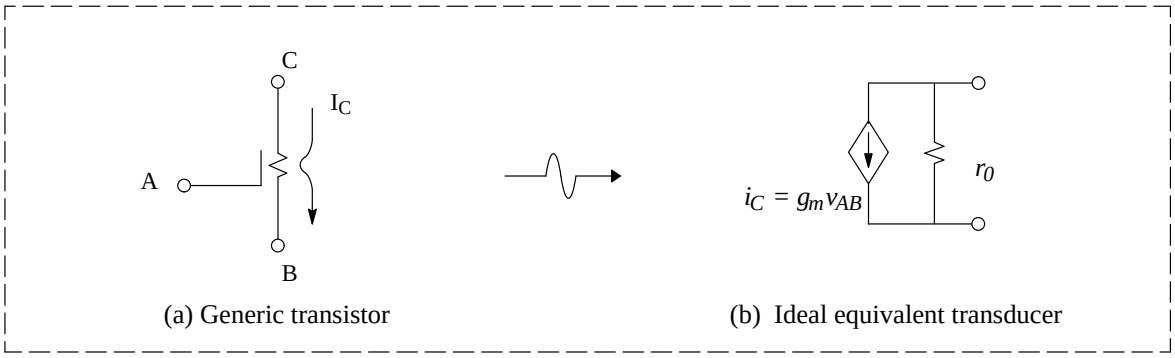


Figure 10.1–2 Small–signal interpretation of transistor as a nearly–ideal, dependent current source

We also have to recognize that the transistor is not a completely ideal current source, and therefore our interpretation of the transistor as a VCT must be amended so that it also has a finite output resistance, as represented by figure 10.1–2(b). Output resistance r_0 is expected to be large, consistent with the ideal behavior of a current source. When the transistor is used to amplify small signals, which is usually the case, the approximation between transistor and VCT is excellent, since the signals may be interpreted as small increments for which the conductances g_m and g_0 are just the *slopes* of the I vs V characteristics, as represented by figure 10.1–3.

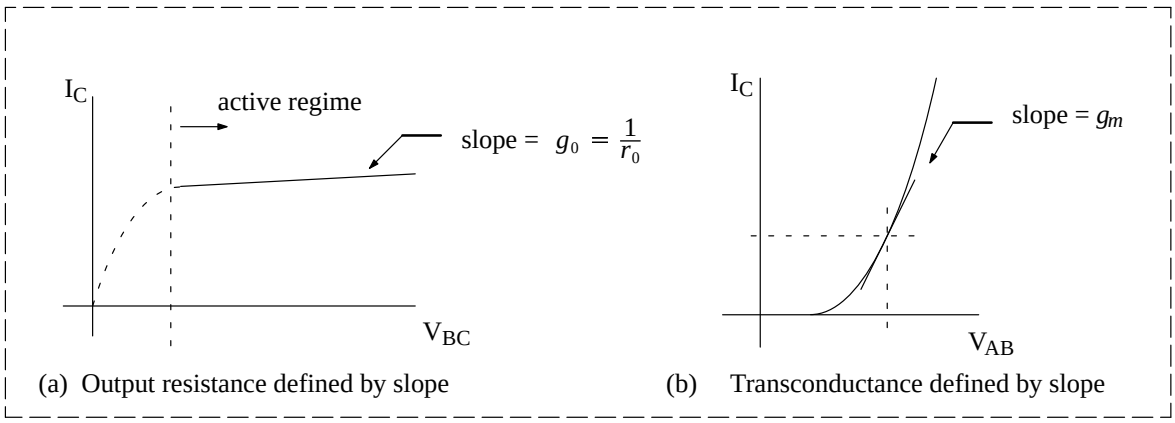


Figure 10.1–3 Interpretation of current–source parameters in terms of the *slopes* associated with the transistor current–voltage characteristics.

In terms of small signal levels, a small incremental change in output current δI_C should take place when there is a small incremental (small–signal) change in the (input) control voltage δV_{AB}. In mathematics speak, this is ex-

pressed as

$$\delta I_C = \frac{\partial I_C}{\partial V_{AB}} \delta V_{AB} = g_m \delta V_{AB} \qquad (10.1\text{–}2)$$

This is of exactly the same form as equation (10.1–1) as given for the VCT, provided that we make the correlation that $\delta I_C \rightarrow i_C$ and $\delta V_{AB} \rightarrow v_{AB}$. As indicated by figure 10.1–3(b) and by equation (10.1–2) transconductance, g_m, is a *transfer* slope that can be picked off the transfer current–voltage characteristics of the transistor. Of course this is also the derivative

$$g_m = \frac{\partial I_C}{\partial V_{AB}} \qquad (10.1\text{–}3a)$$

and usually can be determined directly from the equation of $I(V_{AB})$. Its value depends on the bias point at which the transistor is operated.

And output resistance r_0 is defined by the small slope g_0:

$$g_0 = \frac{\partial I_C}{\partial V_{CB}} = \frac{1}{r_0} \qquad (10.1\text{–}3b)$$

Its value also depends on the bias point at which the transistor is operated.

There are a wealth of semiconductor, vacuum, and electro–optical devices in the transistor kingdom that will have this behavior. But for semiconductors, there are essentially only two generic species of transistor. These are devices for which:

(1) output conductance (and current) are defined by means of bias across a *pn* junction
(2) output conductance (and current) are defined by the effect of an E–field on a semiconductor substrate.

We call these two species:

(1) the 'bipolar–junction' transistor, (BJT)
(2) the field–effect transistor (FET).

Although each of these types of transistor may have similar roles within a circuit, each also has characteristics that make it particularly suited for certain tasks:

(1) The BJT is usually considered to be the 'heavy–lifter' of the transistor kingdom, oriented toward control of larger levels of current.

(2) The FET is usually associated with the light, fast action, particularly in the design of VLSI circuits.

But the division is not emphatic. We can use BJTs in VLSI design, and we can use FETs the size of an orange–juice can for circuits for which high–level current levels must be controlled.

10.2 BIPOLAR–JUNCTION TRANSISTORS AND SINGLE–TRANSISTOR BJT CIRCUITS

The bipolar–junction transistor (BJT) is a three–layer semiconductor device of construction like that represented by figure 10.2–1. In the active mode of operation one of the junctions is forward biased and the other is reverse biased. The layer in the middle of the sandwich is very thin, typically 1–2 microns in thickness. So the carriers that are emitted across the forward–biased junction and into this thin layer find themselves in the immediate vicinity of the strong E–field resulting from the reverse–bias of the second junction. This strong E–field snatches them up just like the bigbad wolf did with the 3×10^{16} little piggies and whisks them across the second junction. The second junction therefore acts as a collector of nearly 100% of the carriers that are emitted across the first junction. The efficiency of this process is adjusted to a maximum by judicious construction and doping techniques.

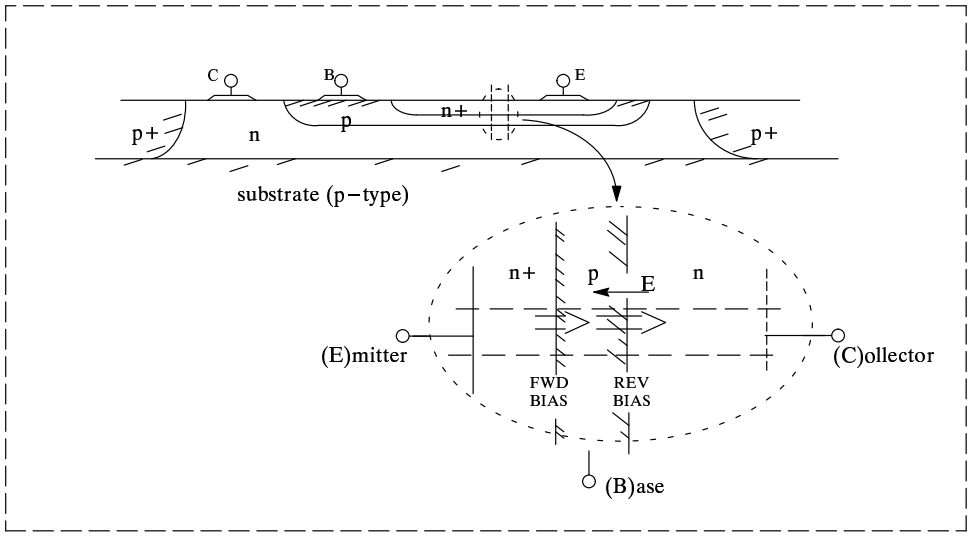


Figure 10.2–1: Representative cross–section of the (planar) BJT

The terminal connected to the forward–biased junction is therefore called the *Emitter* terminal, since carriers are (figuratively) emitted from this node and then injected across the junction. The terminal node connected at the other end, associated with the reverse–biased junction, is called the *Collector* terminal, since the carriers that are swept across the collector junction are "collected" at this node. Usually, for transistors of planar construction as represented by figure 10.2–1 , the emitter is the topmost layer and the collector is the layer just above the substrate. The substrate doesn't do anything, its just a table on which the transistor island is laid. The middle layer of the sandwich is called the *Base* layer. The appropriate labelling and symbol(s) for the BJT is shown by figure 10.2–2. The emitter–base–collector nomenclature is also identified in terms of the layers, by figure 10.2–1.

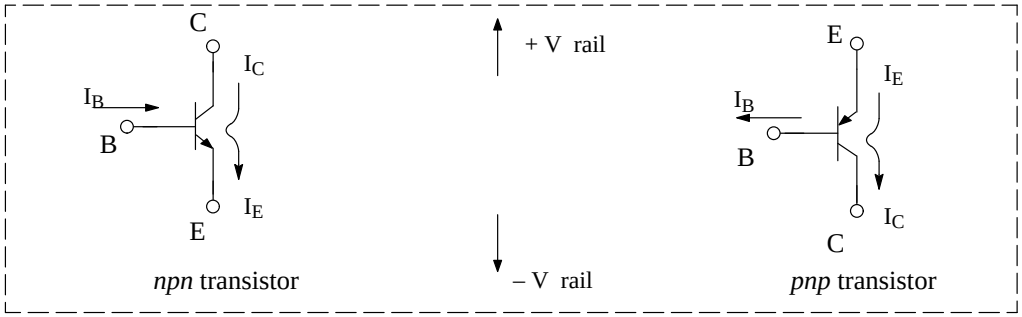


Figure 10.2–2: Labelling nomenclature for the BJT. Since it is a three–layer device, there are two possible genders for the BJT, *npn*, and *pnp*.

As seen by figure 10.2–2, there are two possible genders of BJT, since the semiconductor sandwich may be either *npn* or *pnp* in form. Both forms have two junctions back–to–back. The *npn* form is more commonly used, but the *pnp* also is appropriate, an we will treat them with equananimity. Since the *pnp* transistor is complementary in form to the *npn*, we will often use these two genders of transistor in sequence pairs in our circuit designs, so that the weaknesses of one will be strengthened by the other, much like what happens when the two genders of the human species decide to pair up.

Note that the voltage biases and directions of current flow for the *pnp* transistor are opposite to those for the *npn* transistor.

It is pretty obvious from the circuit symbols used in figure 10.2–2 that $I_E \neq I_C$, even though we like to assume that they are nearly equal. If we add up the currents, and obey Kirchoff's current law which is the usual polite thing to do, then

$$I_E = I_C + I_B \qquad (10.2\text{–}1)$$

But, we also assume that the transistor is a very efficient collector, so that

$$I_C = \alpha_F I_E \qquad (10.2\text{–}2)$$

where α_F should almost be equal to 1.0, or maybe at least to 0.998. or maybe 0.90, – whatever. Ideally, we can assume that the Collector for an efficient transistor will collect almost 100% of the charge–carriers emitted by the Emitter.

However, we don't usually use equation (10.2–2) because it makes more sense to define a 'control' equation in which the output current I_C is controlled by input current I_B. No sweat, we just combine equations (10.2–1) and (10.2–2) and get

$$\frac{I_C}{\alpha_F} = I_C + I_B$$

for which

$$I_C\left(\frac{1}{\alpha_F} - 1\right) = I_B$$

which we rewrite as

$$I_C = \frac{\alpha_F}{1 - \alpha_F} I_B \quad = \beta_F I_B$$

Since α_F is very nearly equal to unity, then we expect β_F to be reasonably large. The equation that we therefore put to the most use is the *control* equation for the BJT

$$\boxed{I_C = \beta_F I_B} \qquad (10.2\text{–}3)$$

where β_F is the *forward current gain*. The forward current gain is also referred to as h_{FE} in some of the older books, probably falls right after the section on alchemie.

A collateral control equation that is handy is

$$I_E = (\beta_F + 1) I_B \qquad (10.2\text{–}4)$$

since $I_E = I_C + I_B$.

A typical value for forward current gain is $\beta_F = 100$. If we happen to be using transistors for high–current, high–voltage applications, the emitter–collector efficiency is reduced and β_F may only be about 25. In general, the *pnp* sister transistor is a little less efficient than the *npn*, and so this fact must be accommodated in circuit design where symmetry is important. Otherwise we just treat them all alike. If we have no idea what the forward current gain of a transistor might be, as is often the case since they are usually passed on to us by Mom, or Aunt Jane, or little sister, and there are usually no performance characteristics included. Then we will assume that $\beta_F = 100$, as a default.

10.3 BIASING OF SINGLE–TRANSISTOR BJT CIRCUITS.

In order for the BJT to exercise control over current, it must be emplaced in a path somewhere in between two voltage rails and in series with other conductive components, much like the circuit shown by figure 10.3–1.

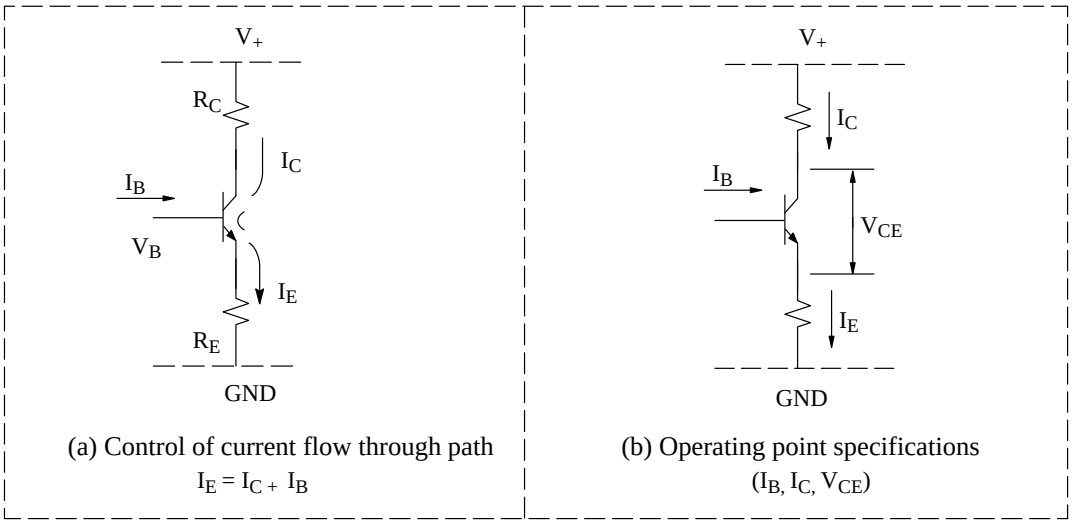


Figure 10.3–1: BJT placed within a conductive path

Although this is not the only way in which we will place a transistor in a circuit, it is the most representative. As given by figure 10.3–1(a) it controls and defines the flow of current between the upper and lower voltage rails according to the biases that are applied and induced within the network.

The equilibrium current flow and voltages in and around the transistor are defined as its *operating point,* and we specify it by the values of (I_B, I_C, and V_{CE}).

Now if we really attempt to solve this transistor circuit with the transistor as a real device, we would have to assume a bias across the junction and use it to find the current, then with this current, assess the junction equations to find junction voltage. With corrected junction voltage the current level would have to be updated. Then we would have to re–evaluate the junction voltage, – etc.

It would have to be an iterative process.

Entertaining though this process might be, the extra accuracy that we gain would be minimal. We are just as well off if we accept a little slop and assume that a bias across a forward–biased *pn* junction is a reasonable value, consistent with the current levels through the junction. Typical default values for a forward–biased *pn* junction carrying currents at mA levels would be:

$$V_{(emitter\ junction)} \equiv 0.7V \quad default \qquad (10.3\text{–}1)$$

As indicated by figure 10.3–2, this corresponds to

$$V_{BE} = 0.7V \quad (for\ npn) \qquad (10.3\text{–}2)$$

Keep in mind that the *pnp* transistor will have opposite polarity across its base–emitter junction. But not to worry, we just look at the direction in which current flows through the junction, and then can easily see what the appropriate polarity should be.

Figure 10.3–2 represents an example in which we look at the current flow and determine the operating point. In this case we are looking at an *npn* transistor, and an applied base bias of V_B = +4.0 V

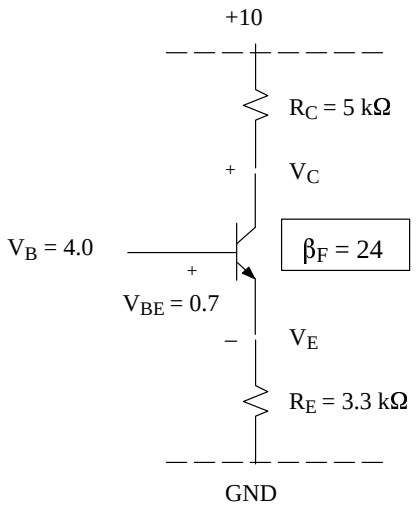


Figure 10.3–2 EXAMPLE, operating–point analysis of the BJT

Now if V_B = 4.0V and V_{BE} = 0.7 V, then

$$V_E = V_B - V_{BE} = 4.0 - 0.7 = 3.3V$$

which we don't need a calculator to determine unless we just like to exercise our fingers. Naturally, if we know the value for V_E , then we can determine the current I_E straight up, since

$$I_E = \frac{V_E - V_{EE}}{R_E} = \frac{3.3 - 0}{3.3} = 1.0mA$$

Note that we may label the lower rail V_{EE}. Although this labelling might add more flavor to the collection of formulas we use for show–and–tell, it mostly is just clutter, and so most of the time we will let GND be GND.

Since we know the value of β_F, then we can determine the value of I_B using equation (10.2–4)

$$I_B = \frac{I_E}{\beta_F + 1} = \frac{1.0}{24 + 1} \quad = 0.04mA$$

From knowledge of I_B we can also find I_C, by:

$$I_C = I_E - I_B = 1.0 - 0.04 = 0.96mA$$

Knowledge of the value for I_C also enables us to find V_C, since

$$V_C = V_+ - I_C R_C = 10 - 5 \times 0.96 = 5.2V$$

The last item that we need to identify the operating point is V_{CE}. Since we know V_C and we know V_E, then

$$V_{CE} = V_C - V_E = 5.2 - 3.3 = 1.9V$$

Pretty simple, huh? No sweat.

Actually these are only approximate answers, since V_{BE} is obviously not just a simple 0.7V as we assumed. But these calculations are "good enough". If we want a better refinement of these values then we turn it over to SPICE

and let Mr. SPICE iterate to his heart's content.

Now let us make a small modification. Change the value of R_E to 2.0 kΩ .

The value of V_E is still 4.0 – 0.7 = 3.3 V, from which we can compute I_E , for which

$$I_E = \frac{V_E - V_{EE}}{R_E} = \frac{3.3 - 0}{2.0} = 1.65mA$$

Proceeding as we did before,

$$I_B = \frac{I_E}{\beta_F + 1} = \frac{1.65}{24 + 1} \quad = 0.066mA$$

and then

$$I_C = I_E - I_B = 1.65 - 0.066 = 1.584mA$$

Then we can find V_C, and V_{CE}, as

$$V_C = V_+ - I_C R_C = 10 - (5 \times 1.584) = 2.08V$$

$$V_{CE} = V_C - V_E = 2.08 - 3.3 = -1.22V \quad ???!!$$

Wait a minute! There is NO WAY that V_E can be at a higher voltage than V_C!

Well, did we make a mistake?
–Not according to our equations and our math. –Check it –

So what is wrong?

There was a little precondition that we assumed. We assumed that the transistor was operating in "the active mode", for which one junction is forward biased and the other junction is reverse–biased. In this case, the transistor had *both* junction forward biased! So there was *no way* that it could be in the "active" mode.

So that means that all of our control equations are shot to hell, and therefore we cannot use either equation (10.2–3) or (10–2–4).

But not to worry. We simply make a little default assumption. We always assess the circuit as if it were in the active mode. And if it is not, then it is in a 'non–active' mode for which V_{CE} = low. We then assume a default value for V_{CE} of

$$V_{CE} = 0.3V \qquad \textit{default,} \text{ non–active (=saturation) mode} \qquad \textit{(10.3–3)}$$

For the BJT, the non–active mode is often called the "saturation" mode, since the current will reach a limit defined by the resistances in the circuit rather than being defined by the transistor.

Using the $V_{CE}(sat)$ default for this example, we then find that

$$V_C = V_E + V_{CE} = 3.3 + 0.3 = 3.6V$$

Then we can find the current I_C by means of

$$I_C = \frac{V_+ - V_C}{R_C} = \frac{10 - 3.6}{5} = 1.28mA$$

and then we can find I_B, by

$$I_B = I_E - I_C = 1.65 - 1.28 = 0.37mA$$

so that the operating point is

$$(I_B, I_C, V_{CE}) = (0.37,\ 1.28,\ 0.3)$$

Keep in mind that we always first assume that the transistor is in the active mode. If this assumption fails, then we assume that the transistor must be in a saturated (non–active) mode of operation.

It is a two–step process. If the transistor is biased correctly, then the second step is unnecessary.

We usually do not bias transistors in the way indicated by figure 10.3–2, with V_B defined separately from the other voltage biases. It is just as good, and probably better, to make use of the voltage supply rails and let the bias V_B be accomplished by means of a voltage–divider circuit, as shown by figure 10.3–3.

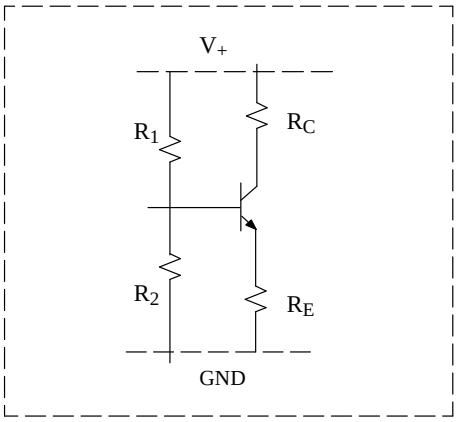


Figure 10.3–3 Four–resistor bias network with transistor in the middle of the frame.

The two resistors R_1 and R_2 form a voltage–divider which will produce bias V_B at the base of the transistor, as well as supply base current I_B.

Keep in mind that this arrangement implies that the source V_B to the base has an equivalent resistance that must be included in our analysis, as defined by one of our old friends, *Thevenin's Theorem.* The Thevenin equivalent of the voltage divider is shown by figure 10.3–4.

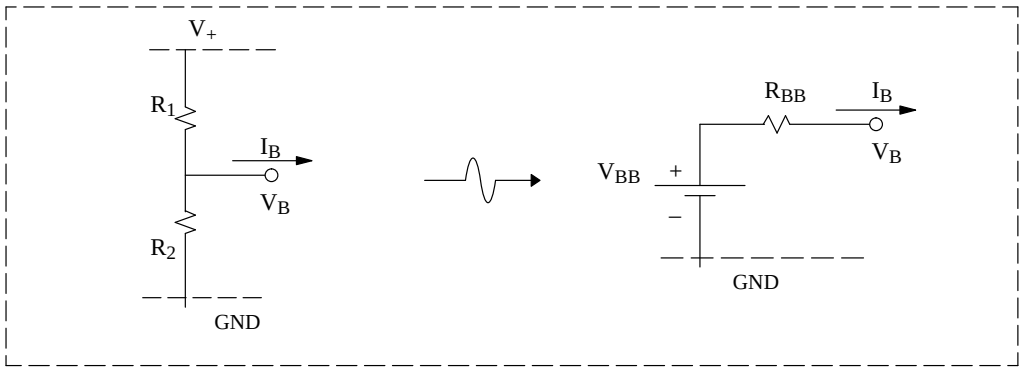


Figure 10.3–4 Thevenin equivalent voltage source to voltage divider

And the Thevenin equivalent values are

$$V_{BB} = \frac{R_2}{R_1 + R_2} V_+ \qquad ,$$

$$R_{BB} = R_1 \parallel R_2 \qquad (10.3\text{–}4)$$

The complete equivalent circuit for figure 10.3–3 is represented by figure 10.3–5, and will let us analyze this typical BJT bias circuit.

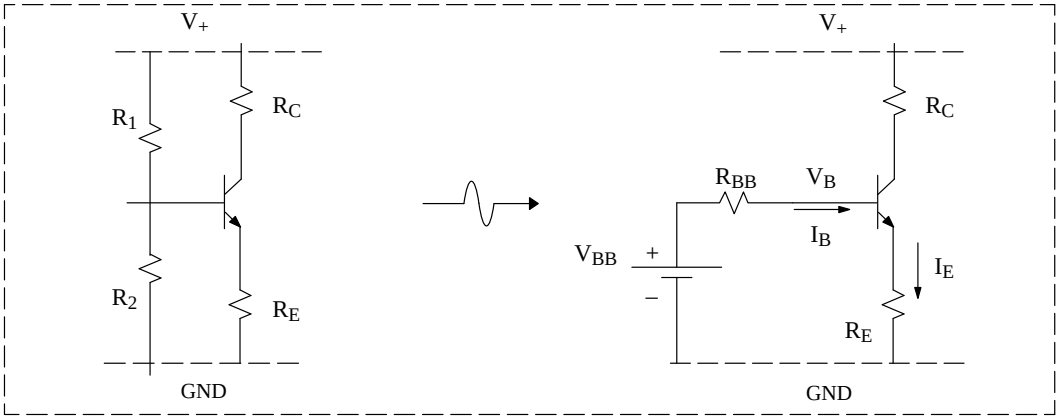


Figure 10.3–5 Thevenin equivalent to 4–resistance bias of (*npn*) BJT

If we look just at the base–emitter circuit and apply Kirchoff's voltage law, we find that

$$V_{BB} - I_B R_{BB} - V_{BE} - I_E R_E - V_{EE} = 0$$

Assuming that the transistor is in the active regime, then we can use equation (10.2–4) to give us a definition of the current that will flow in the circuit. Turning the crank on the algebra, we get

$$I_B = \frac{V_{BB} - V_{BE} - V_{EE}}{R_{BB} + (\beta_F + 1)R_E} \qquad (10.3\text{–}5a)$$

This is a recipe formula that we might expect to recur many times. It usually is simplified by the fact that V_{EE} = GND, and therefore V_{EE} need not even be included in the formula.

We might note that if we bias a *pnp* transistor using the 4–resistance frame, as indicated by figure 10.3–6, then we have practically the same result as equation (10.3–5a) for the base current I_B,

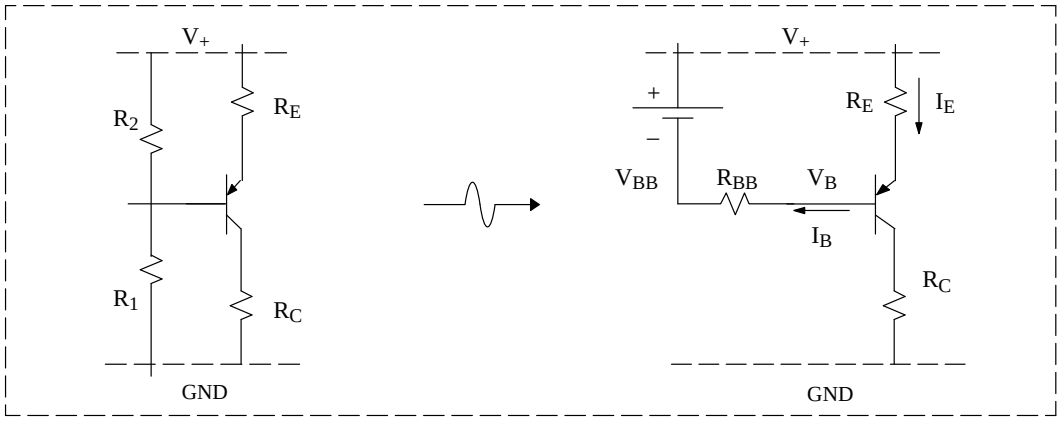


Figure 10.3–6 Thevenin equivalent representation for 4–resistance bias of (*pnp*) BJT

for which the recipe form will be

$$I_B = \frac{V_{BB} - V_{BE} - V_+}{R_{BB} + (\beta_F + 1)R_E} \qquad (10.3\text{–}5b)$$

Of course, in this instance, $V_{BE} = -0.7$ V since the *pnp* biases and current flows are *opposite* to those for the *npn* transistor. If you check all of the signs, everything works out OK. Note that in this instance $V_{EE} = V_+$.

Let us consider an example:

EXAMPLE 10.3–1: Four–resistance bias frame:

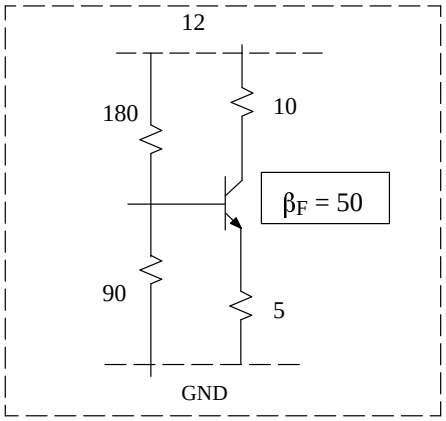


Figure E10.3–1 Example: Analysis of a 4–resistance bias frame for the BJT

SOLUTION: The voltage–divider attached to the base consists of resistances R_1 and R_2. Its Thevenin equivalent will have electrical characteristics

$$V_{BB} = \frac{R_2}{R_1 + R_2}V_+ = \frac{90}{270} \times 12 = 4V \quad , \; R_{BB} = R_1 \| R_2 = 180 \| 90 = 60k\Omega$$

as reflected by equation (10.3–3).

Now, applying these numbers to the algebraic analysis that we just did, which culminated in equation (10.3–5), we get

$$I_B = \frac{V_{BB} - V_{BE} - V_{EE}}{R_{BB} + (\beta_F + 1)R_E} = \frac{4 - 0.7}{60 + (50 + 1)5} = .0105mA$$

Then we will find that

$$I_C = \beta_F I_B = 50 \times .0106 = 0.523mA$$

From the knowledge of I_C we can determine V_C and V_E:

$$V_C = V_+ - I_C R_C = 12 - 0.523 \times 10 = 6.76V$$

$$V_E = V_{EE} + I_E R_E = 0 + (0.523 + .0105) \times 5 = 2.67V$$

Then the output bias voltage V_{CE} is:

$$V_{CE} = V_C - V_E = 6.76 - 2.67 = 4.09V$$

so that the operating point is

$$\boxed{(I_B, I_C, V_{CE}) = (0.105,\ 0.523,\ 4.09)}$$

In example 10.3–1, note that $V_{CE} \simeq 4$ V or $\simeq$ 1/3 V_+ . As a design option we should note that when V_{CE} is about 1/3 of the voltage difference between the upper and lower supply rails, we have an output margin that usually gives the output signal a large amplitude swing with relatively little distortion. It is best to hand the proof of this option off to SPICE.

Note that if R_C is too large, then V_C can be driven down to a point for which we no longer can assume that the transistor is operating in the active regime, and therefore our nice equation (10.3–5) is no longer valid.

For example, if $R_C = 20$ kΩ, then

$$V_C = V_+ - I_C R_C = 12 - 0.532 \times 20 = 1.35V$$

Which is impossible. There is no way that V_C can be less than V_E. The transistor has been driven into saturation.

Although it is reasonably straightforward to determine the approximate operating point by use of the default for $V_{CE}(sat) = 0.3$V, we usually don't. If the transistor proves to not be in the active mode, we punt. Then we redesign the circuit, probably by reducing R_C.

So whenever we assess a transistor circuit, we always make a snake check to see if it is really in the active mode.

The flag is the magnitude of V_{CE}, or better yet, the value of V_C relative to V_B, since it is the bias V_{BC} that identifies whether–or–not the BC junction is in reverse bias, as is required for active mode operation.

It is worthwhile to recognize that β_F is usually sufficiently large so that we can make a reasonable estimate of the current flowing through the transistor just from the biases provided by the resistances R_1 and R_2, and the resistance R_E. If β_F = large, then

$$I_C \approx I_E \approx \frac{V_{BB} - V_{BE} - V_{EE}}{R_E} \qquad (10.3\text{–}6)$$

for which, this example

$$I_C \approx I_E \approx \frac{V_{BB} - V_{BE} - V_{EE}}{R_E} = \frac{4 - 0.7}{5} = 0.66ma$$

As compared to the answer that we obtained with $\beta_F = 50$, we see that the result is not too bad. Not great, but if we are in a hurry, want to make a quick, rough, assessment, it is probably OK. Most of the time β_F is larger than 50, so the rough estimate is not at all unreasonable. For instance, if we let $\beta_F = 200$, we would get $I_C = 0.62$ mA ≈ 0.66 mA.

It is also worthwhile to take a look at a sister example, one for which we bias a *pnp* transistor. Consider the example represented by figure E10.3–2

EXAMPLE 10.3–2: Four–resistance bias frame, *pnp* transistor.

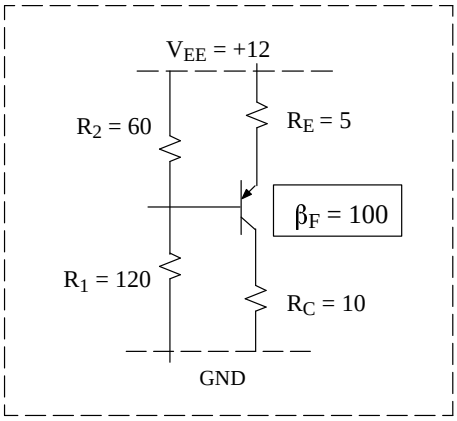


Figure E10.3–2 Four–resistor bias network with *pnp* transistor.

Note the subscripts. This nomenclature is used so that equations (10.3–5a) and (10.3–5b), are virtually the same.

Thevenin equivalent values for the R_1, R_2 string are evaluated as they are for any voltage divider:

$$V_{BB} = \frac{R_1}{R_1 + R_2} V_+ = \frac{120}{180} \times 12 = 8.0V \quad ,$$

$$R_{BB} = R_1 \parallel R_2 = 60 \parallel 120 = 40k\Omega$$

Taking these values and applying them to equation (10.3–5b) we get

$$I_B = \frac{V_{BB} - V_{BE} - V_{EE}}{R_{BB} + (\beta_F + 1)R_E} = \frac{8 - (-0.7) - 12}{40 + (100 + 1)5} = -.00606mA$$

The negative sign indicates that the current is flowing out of the base, just like it is supposed to do. Taking this magnitude of I_B we get I_C and V_C and V_E, as follows:

$$I_C = \beta_F I_B = 100 \times .00606 = 0.606mA$$

$$V_C = 0.0 + I_C R_C = 0.606 \times 10 = 6.06V$$

$$V_E = V_+ - I_E R_E = 12 - (0.606 - .0061) \times 5 = 8.94V$$

From which we find that V_{CE} will be

$$V_{CE} = 6.06 - 8.94 = -2.88V$$

As expected, the polarity of this bias voltage is *opposite* to that for the *npn* transistor. The operating point is

$$\boxed{(I_B, I_C, V_{CE}) = (0.0061,\ 0.606,\ 2.88)}$$

10.4 SMALL–SIGNAL ASSESSMENT OF THE BJT AND BIAS CONSIDERATIONS

Once the transistor is biased into an active state, then it can control the output by applying wovulations to the input voltage, and thereby end up wovulating the output current I_C. Naturally, we expect that these input modulations are of small amplitude, so that equations (10.1–1) and (10.1–2) are appropriate, with a change in the subscript notation to reflect that we are using a BJT. Then:

$$i_C = g_m v_{BE} \qquad (10.4\text{–}1)$$

If we are to use the transistor as a signal amplifier we must know how it transfers signals, and therefore we must have transconductance, g_m, at our disposal. It is a derivative as indicated by equation (10.1–3), so we have need to identify a model for current I_C vs input bias V_{BE} . This may be accomplished in a relatively straightforward manner by means of a *circuit model*, using dependent sources, as indicated by figure 10.4–1.

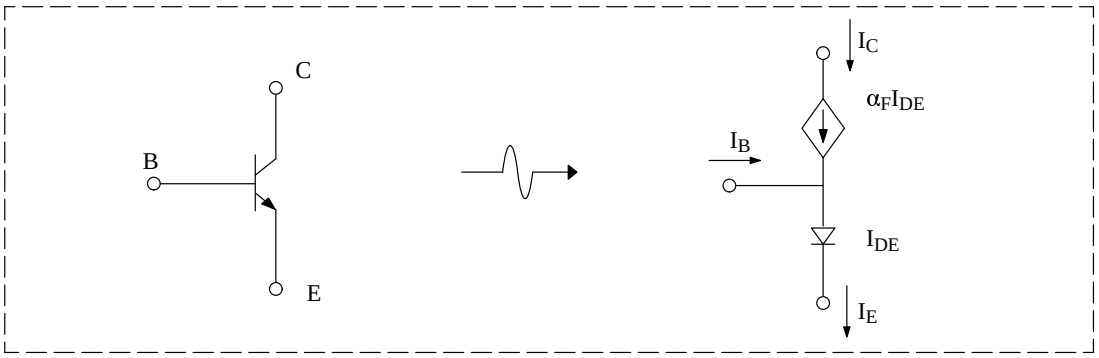


Figure 10.4–1: Circuit model for (*npn*) BJT

With this circuit model we can then assume that I_C is controlled directly by the diode bias V_{BE}, for which

$$I_C = \alpha_F I_{DE} = \alpha_F I_{SE}\left(e^{V_{BE}/V_T} - 1\right) \qquad (10.4\text{–}2)$$

Note that this equation is also consistent with equation (10.2–2), for which α_F is the factor that indicates the efficiency of the emitter–collector process In this case we are actually making emphasis that the emitter current is just a diode current.

Although the model indicated by figure 10.4–1 and equation (10.4–2) is adequate, a little better model can be defined that accommodates the bilateral symmetry options associated with the BJT, since it is a matter of choice about which junction we forward bias and which we reverse bias. This more general model is called the *Ebers–Moll model*, and is of the form as represented by figure 10.4–2

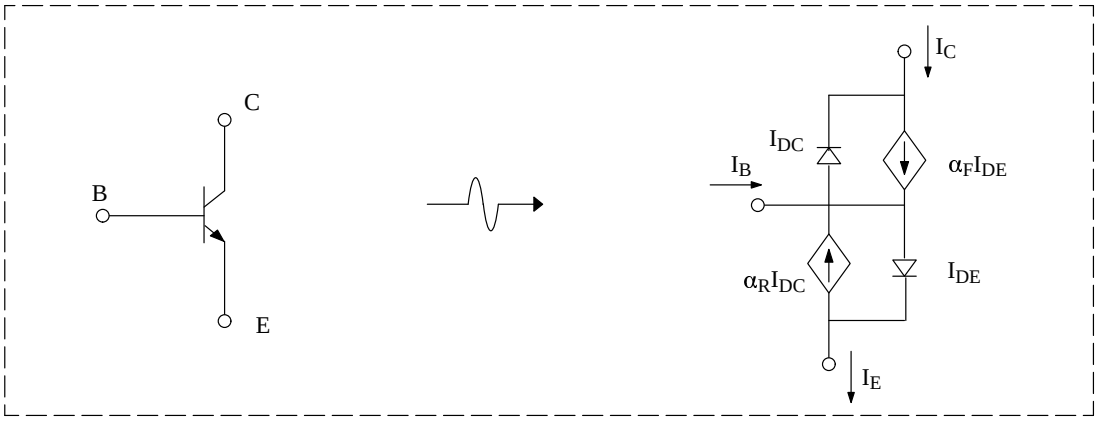


Figure 10.4–2: Ebers–Moll circuit model for (*npn*) BJT

As indicated by figure 10.4–2 the Ebers–Moll model is one that applies the concept of figure 10.4–1 twice, once for each polarity of operation. The parameter α_R is the factor associated with the efficiency of the (reverse) emitter–collector process. The reverse mode is not usually as well–formed as it is for the forward emitter–collector process and therefore β_R is also not nearly as good. Typical β_R has value 0.5.

If we use the Ebers–Moll model, then

$$I_C = \alpha_F I_{DE} = \alpha_F I_{SE}\left(e^{V_{BE}/V_T} - 1\right) - I_{DC} \qquad (10.4\text{–}4)$$

which, since I_{DC} represents diode current for the junction in reverse bias, we might as well neglect it and use equation (10.4–2), which in a little more abbreviated form is

$$I_C = I_S\left(e^{V_{BE}/V_T} - 1\right) \qquad (10.4\text{–}5)$$

where we have just let $I_S = \alpha_F I_{SE}$ for convenience, since we wish to use equation (10.4–5) in a little more mathematics werks.

Explicitly, we see that equation (10.4–5) will give us the transconductance, since

$$g_m = \frac{d}{dV_{BE}}\left[I_S\left(e^{V_{BE}/V_T} - 1\right)\right] = \frac{1}{V_T} \times I_S\left(e^{V_{BE}/V_T}\right) \quad = \frac{I_C}{V_T}$$

so that

$$\boxed{g_m = \frac{I_C}{V_T}} \qquad (10.4\text{–}6)$$

Take note of the fact that g_m is proportional to the current I_C flowing through the transistor. Also, at nominal operating temperatures, V_T = thermal voltage $\simeq$ .025 V

Equation (10.4–6) tells us that, if we can specify the current flowing through the transistor by means of another element within the circuit that explicitly defines path current *I*, then we can also specify the transconductance.

Well, so what?

Well – , if we control g_m for the transistor, we essentially control its amplification strength. Good idea.

Therefore we also may elect to bias a transistor by means of a ”3–1/2” resistance frame as shown by figure 10.4–3, for which the current through the transistor is defined by a fixed current source as shown.

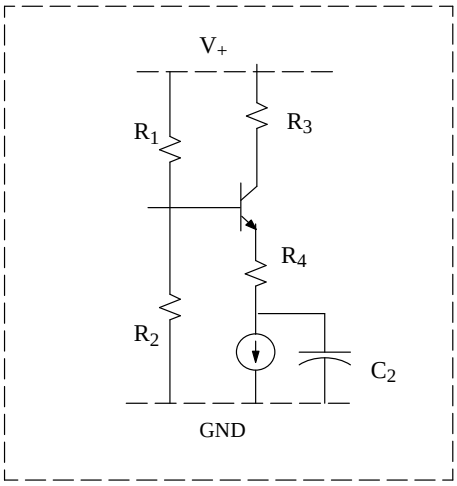


Figure 10.4–3 Three–resistor bias network for a transistor with current source used to define operating point.

The bias frame shown by figure 10.4–3 has something extra, a *bypass* capacitance, C_2. Mr. capacitance does not affect the operating point at all, because for steady–state operation, it is the same as an open circuit. Transistor circuits will always have a batch of capacitances located around the transistor and its bias frame, and they may all be ignored when evaluating the operating point.

Consider the following example:

We assume that C_E is large, that all resistances are in kΩ and that the current source is in mA.

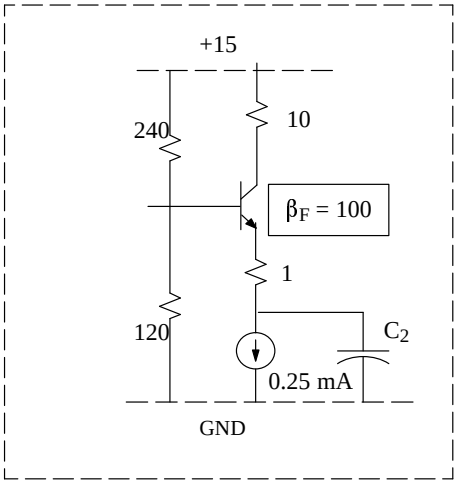


Figure 10.4–4 Example, *npn* transistor biased by means of a current source.

Since I_E is fixed by the current source, then the process is relatively simple. Assume that the circuit is operating in the active mode. Then

$$I_B = \frac{I_E}{\beta_F + 1} = \frac{0.25}{100 + 1} = .00247$$

Then, using equation (10.2–3), we get

$$I_C = \beta_F \times I_B = 100 \times .00247 = .247mA$$

We can determine V_C by

$$V_C = V_+ - I_C R_C = 15 - 0.247 \times 10 = 12.53V$$

Now, in order to find V_{CE}, we need to find V_E. But we have no idea what voltage will fall across the fixed current source since ANY voltage can fall across a current source. But, not to worry. We will just find V_B, then use it to find V_E.

In order to find V_B, we need to find V_{BB} and R_{BB}. This is straightforward, done just like before for other examples, and gives

$$V_{BB} = \frac{R_1}{R_1 + R_2} V_+ = \frac{120}{360} \times 15 = 5.0V \quad ,$$

$$R_{BB} = R_1 \parallel R_2 = 120 \parallel 240 = 80k\Omega$$

Now V_B is just

$$V_B = V_{BB} - I_B R_{BB} = 5 - 0.00247 \times 80 = 4.81V$$

Then V_E is just one junction difference away from this value,

$$V_E = V_B - V_{BE} = 4.81 - 0.7 = 4.11V$$

so that V_{CE} is

$$V_{CE} = V_C - V_E = 12.53 - 4.11 = 8.42V$$

The operating point is then

$$\boxed{(I_B, I_C, V_{CE}) = (0.0025,\ 0.248,\ 8.42)}$$

For all our work represented for the process of finding the operating point for different options of bias configurations, we are often just as satisfied to accept an approximate operating point and let SPICE work out the refinements. In this respect, for the previous example, we might just as well assume that

$$I_C \approx I_E = I$$

as specified by the current source.

10.5 SMALL–SIGNAL EQUIVALENT MODEL OF THE BJT

If we use equation (10.4–6) as a guide, then the transistor can be conceptually replaced by a linear dependent current source like that indicated by figure 10.5–1

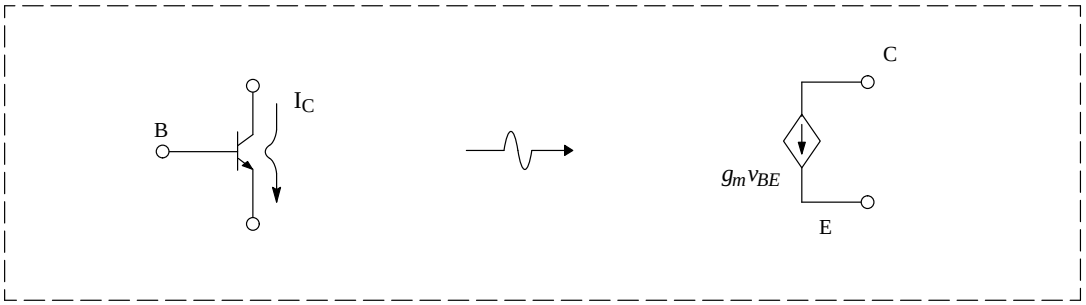


Figure 10.5–1. "Ideal" small–signal equivalent model for the BJT

But don't get excited. This model is a little too ideal and therefore is insufficient for a reasonable assessment of circuit performance. We know good and well that the output terminal at C must have an output resistance, since current has to increase a tad with increase of V_{CE} and we know that there has to be a finite input resistance since there is a conductance path that draws current I_B.

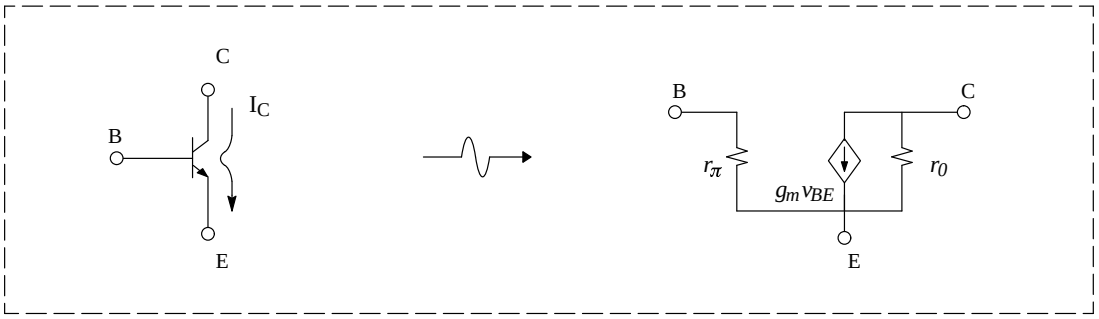


Figure 10.5–2. Realistic small–signal equivalent model for the BJT (hybrid–pi model).

The finite input resistance is a natural consequence of the junction since

$$I_B = \frac{I_C}{\beta_F} = \frac{1}{\beta_F} \times I_S\left(e^{V_{BE}/V_T} - 1\right)$$

and therefore the input slope is

$$\frac{dI_B}{dV_{BE}} = g_\pi = \frac{1}{r_\pi} = \frac{1}{\beta_F}\frac{dI_C}{dV_{BE}} = \frac{g_m}{\beta_F}$$

for which we can always use

$$\boxed{g_\pi = \frac{g_m}{\beta_F}} \qquad (10.5\text{–}1)$$

for which $r_\pi = 1/g_\pi$.

The output conductance g_0 is a consequence of the natural increase of I_C with respect to V_{CE}, as represented by figure 10.5–3. The output conductance shows up as the finite slope of I_C with respect to V_{CE}.

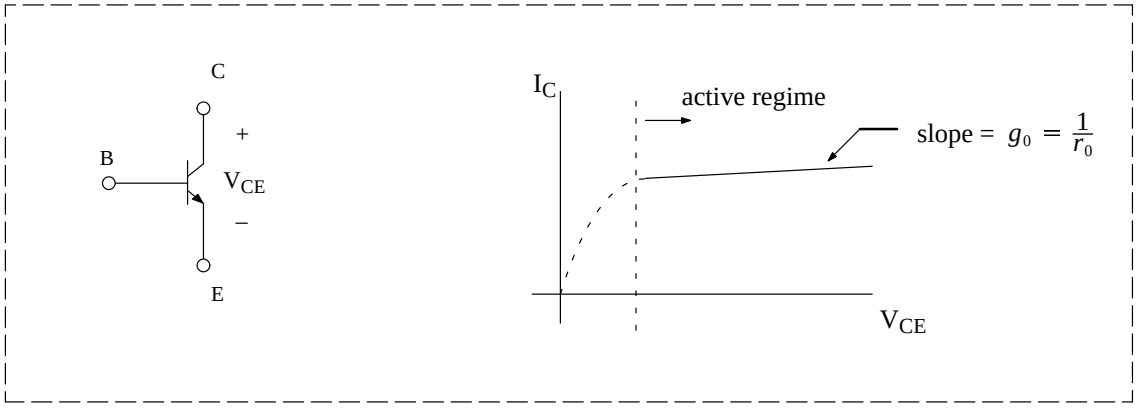


Figure 10.5–3 Output conductance and the Early effect.

This same phenomena was identified in section 10.1. This output slope for the BJT is of the form

$$g_0 = \frac{dI_C}{dV_{CE}}$$

consistent with equation (10.1–3). By analyzing the operation of the emitter–collector processes and the junction depletion regions, the slope can also be shown to be proportional to the current I_C. This analysis was done so in some of the initial studies of the properties of the BJT by James Early [ ] and he showed that,

$$\boxed{g_0 = \frac{I_C}{V_A}} \qquad (10.5\text{–}2)$$

where V_A is now called the *Early voltage*. The value of V_A is dependent upon transistor layer thicknesses and doping profiles. Typically it is about 100V.

The phenomena is called the *Early effect.* James Early died in 1988 and so maybe it should be now be called the late Early effect.

Whenever we assess the small–signals under control of the BJT we use the small–signal model indicated by figure 10.5–2, which is also called the *hybrid–pi* model of the BJT.

If the *pnp* transistor is analyzed it has exactly the *same* model, and same directions of small–signal current as the *npn* transistor. This is to be expected since, for the *pnp* transistor, I_C is negative, but so is V_{BE}, so that dI_C/dV_{BE} is the same, same polarity, same direction (from C to B) as for the *npn* transistor

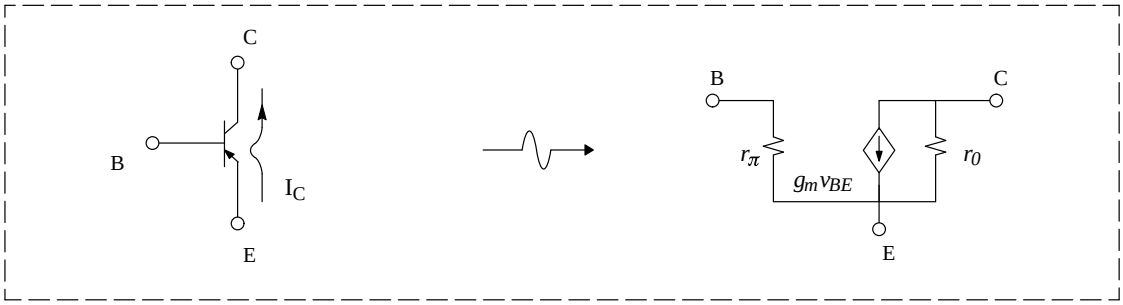


Figure 10.5–4. The small–signal model is the same for the *pnp* transistor as for the *npn* transistor

Note that, for figure 10.5–4, we show the *pnp* transistor in an orientation that is usually not used, since we like for the operating current to flow (down) from the upper rail to the lower rail. Therefore the small–signal model of the transistor circuit will have to reflect this orientation, with appropriate connections of the terminals to input and

output loads. We will show a few examples as we march through the several configurations that are useful for the BJT as a single–transistor amplifier cell.

We might also note, that although it is politically correct to use a voltage–controlled current source in defining the transfer characteristics of the transistor, it is also practical to use a current–controlled current source since

$$i_C = g_m v_{BE} = (\beta_F g_\pi) v_{BE} = \beta_F (g_\pi v_{BE}) = \beta_F i_B$$

Then the transfer element is a current–controlled transducer (CCT) instead of a voltage–controlled transducer, as indicated by figure 10.5–5.

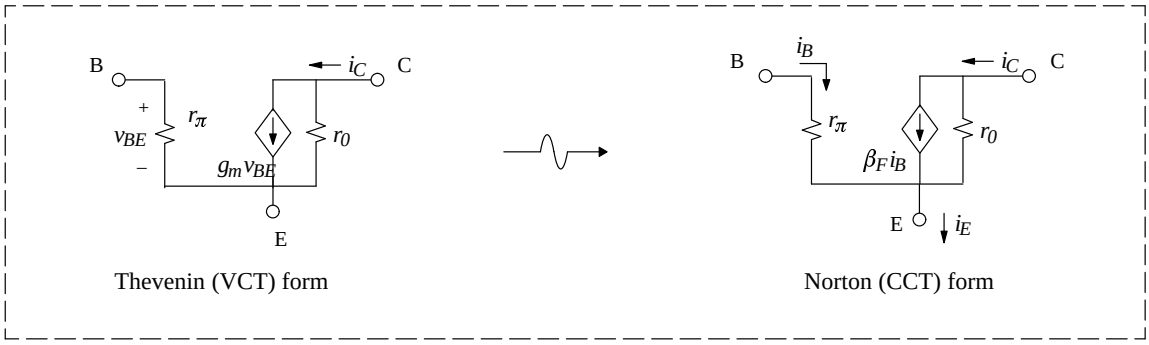


Figure 10.5–5. ”Ideal” small–signal equivalent model for the BJT

For the current–controlled transducer, the following small–signal equations are applicable and appropriate.

$$i_C = \beta_F i_B \qquad\qquad i_E = (\beta_F + 1) i_B$$

Note, again, the use of *lower–case* symbols for current, to indicate small–signal levels.

10.6 SINGLE TRANSISTOR BJT AMPLIFIERS: THE COMMON–EMITTER CONFIGURATION

Having made some identification of operating points and small–signal transistor models, let us examine an example working circuit using the BJT, the common–emitter (CE) configuration. The generic CE configuration is shown by figure 10.5–1

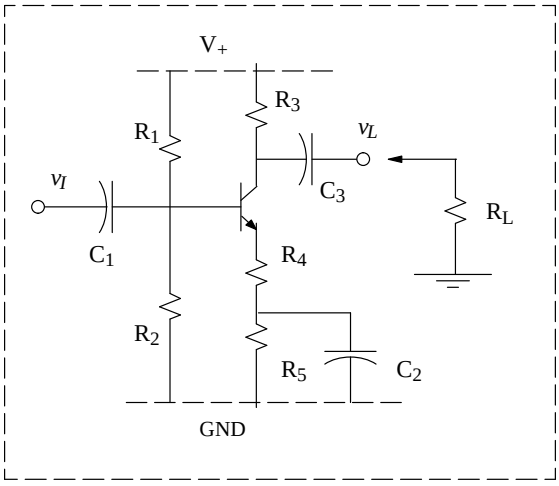


Figure 10.6–1 Common–emitter topology using an *npn* transistor. As notation, the small–signal input and output voltage levels are indicated as *lower–case* symbols.

The common–emitter topology is one for which the input signal is fed to the base through input capacitance C_1 and output signal taken off the collector node and applied to load R_L through capacitance C_3. The capacitances will only pass time–varying signals, but otherwise are an open circuit to steady–state, operating point levels. As a nomenclature, the small–signal rms amplitude is indicated by a lower case letter. The output signal v_O may also be written as v_L, since it is the (small–signal) rms amplitude across load R_L.

We might note that the bypass capacitance C_2 is used to bypass a part of the resistance in the emitter leg. Therefore the resistance R_{E2} is shunted, and only the resistance R_{E1} is visible to the time–varying signal. But as far as the analysis of the operating point is concerned,

$$R_E = R_4 + R_5 \qquad \text{for DC (operating point) analysis}$$

We have a circuit with small–signal amplitude v_I injected at the input and observed at the output v_O, and we have a small–signal transistor model. Therefore we may redraw figure 10.5–1 as a *small–signal equivalent* circuit for purpose of analysis of the signal amplification properties of the CE configuration.

Before we do so, recognize that the upper and lower rails, and the ground, (if separated), are voltage supply rails. As ideal voltage sources they have zero resistance between them. As far as a time–varying signal is concerned, no signal will fall across this zero resistance and so the voltage rails all have zero signal difference between them. Therefore we may, for small–signal purposes, assume that they are all an equivalent common point, which we will euphemistically call "AC ground". This concept will make our circuit considerably simpler, but will wrench the topology into a different form than that represented by figure 10.5–1. The small–signal topology for this configuration (CE) is indicated by figure 10.5–2.

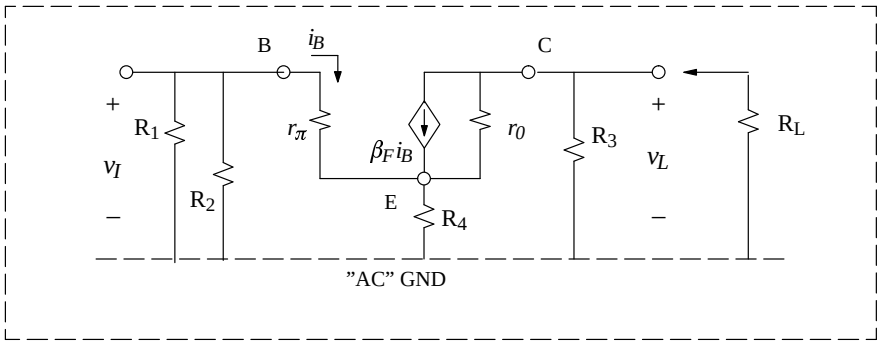


Figure 10.6–2 Two–port small–signal equivalent circuit to figure 10.6–1

We might take note that the small–signal equivalent circuit indicates the effect of the capacitances as elements that allow the free passage of all small–signals without regard to any attenuation effects. For example, the resistance R_{E2} does not show in figure 10.6–2 because it is completely shunted by capacitance C_2.

Naturally, this use of the capacitances is an approximation. In a more exacting analysis, we should assess the complex impedances of the circuit. But frequency–domain analysis is an indulgence at this point, and we will gain more insight by first analyzing the circuit as if the amplifier network were a plain linear network with resistances and dependent sources only. We will assume that the frequencies of the signals are sufficiently large and that the values of the capacitances are of sufficient size so that the capacitative impedances are small–to–negligible.

We also will find it convenient to *always* draw the small–signal circuit as a two–port network. This prerogative makes emphatic that the 'amplifier' nature of a transistor–driver circuit is of the form where there is an *input port* and an *output port.* In that respect we must not only find a transfer function with transfer gain, but also find an input impedance R_{in} and an output impedance R_{out} for the circuit. The transfer function that we usually determine is the voltage 'gain' or voltage transfer circuit.

The recipe is as follows:

Find operating point: (I_B, I_C, V_{BE}) by equilibrium (DC) analysis.	Find the small–signal parameters:	Find the two–port characteristics: $\left(R_{in}, R_{out}, \frac{v_L}{v_I}\right)$
If the circuit is not in the active mode –punt (and redesign, if you are the designer.)	For the BJT they are: (g_m, r_π, r_0)	We may find it easier to find some other transfer function besides v_L/v_I
	Construct small–signal equivalent circuit, analyze linear network	

In most cases we will not need to perform the second part of step 2, since many of the single–transistor configurations are already worked over by generations of EE students.

For the CE topology, we can best assess the circuit by making a minor approximation. We know that the resistance r_0 is large and therefore will make only a negligible contribution to currents in the emitter and the collector. Therefore, neglecting this small current, we can assess the signal voltage at node B (figure 10.6–2) by

$$v_B = i_B r_\pi + i_E R_4 \quad = i_B r_\pi + (\beta_F + 1) i_B R_4$$

Therefore the input resistance to the base of the BJT transistor, which we will call R_{iB}, is

$$\boxed{R_{iB} = \frac{v_B}{i_B} = r_\pi + (\beta_F + 1) R_4} \qquad (10.6\text{–}1)$$

and the input resistance is the entire set of resistances seen by the input current flowing into the input node, which will not only see R_1 and R_2, but also R_{iB}. The input resistance R_{in} will then be

$$R_{in} = \frac{v_I}{i_I} = R_{iB} \parallel R_1 \parallel R_2 \qquad (10.6\text{–}2)$$

We might note that the resistance R_{iB} is the resistance 'looking into' the base, and that it 'sees' the resistance connected to the emitter multiplied by the factor $(\beta_F + 1)$. This effect will always occur, since the emitter current, and thereby the equivalent effect, will be a factor $(\beta_F + 1)$ larger. For whatever network of resistances are connected to the emitter node, this 'emitter multiplication' will take place.

When we analyze a circuit, we may find it convenient to analyze it from the point of view of an electron, cruising along one of its conductive thoroughfares within the network. In this case, the electrons see that there is a multiplied resistance effect as it takes the route into the base of the BJT. The same multiplication effect is true, whether for *npn* or *pnp* transistors, since the same current multiplication takes place.

Now, at the collector of the transistor, there is a resistance, r_{out}, 'looking into' into the collector, of magnitude

$$r_{out} = r_0\left(\frac{r_\pi + (\beta_F + 1)R_4}{r_\pi + R_4}\right) \qquad (10.6\text{–}3)$$

This result can be obtained by nodal analysis at the collector, as represented by figure 10.6–3. In order to assess this output resistance we have to assume that the input signal is inactive, so that $v_I = 0$. Then the small–signal circuit will have R_1 and R_2 shunted, and will look like that of figure 10.6–3.

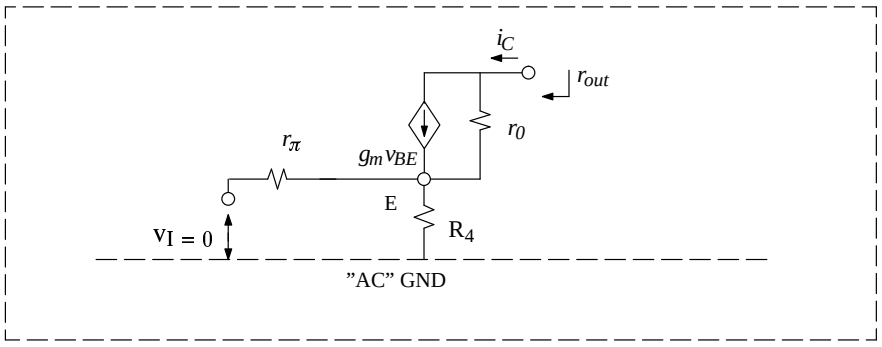


Figure 10.6–2 Small–signal equivalent circuit to figure 10.6–1

Then

$$i_C = g_m v_{BE} + v_C g_0 - v_E g_o = g_m(-v_E) + v_C g_0 - v_E g_0 = v_C g_0 - v_E(g_m + g_0)$$

and at node E

$$0 = v_E(g_\pi + g_0 + G_4) - g_0 v_C - g_m v_{BE} = v_E(g_\pi + g_m + G_4 + g_0) - g_0 v_C$$

The two equations can be simplified by neglecting g_0 when it is an additive term with g_π and g_m, for which:

$$0 = v_E((\beta_F + 1)g_\pi + G_4) - v_C g_0$$

$$i_C = -v_E g_m + v_C g_0$$

If vE is eliminated between these two equations then

$$\frac{v_C}{i_C} = \frac{1}{g_0}\left(\frac{(\beta_F + 1)g_\pi + G_4}{g_\pi + G_4}\right)$$

which is the same as equation (10.6–3), if we multiply numerator ands denominator by $r_\pi R_4$.

The output resistance is then the set of resistances that are seen by the output current, which includes both R_3 and r_{out}, as follows:

$$\boxed{R_{out} = \frac{v_O}{i_O} = R_3 \parallel r_{out}} \qquad (10.6\text{–}4)$$

Collector resistance r_{out} also can be identified as the resistance which we will see 'looking into' the collector. We might note that r_{out} is multiplied by an emitter multiplication factor also. As it turns out, the emitter resistance R_{E1} provides a feedback effect that causes multiplication effects at the other two terminals of the BJT.

The voltage transfer function, or voltage gain, can be obtained by noting that

$$v_O(= v_L) = -i_C R_3 \parallel R_L$$

But since $i_C = \beta_F i_B$, and since $i_B = v_B/R_{iB}$ then

$$v_L = -(\beta_F + 1) i_B R_3 \parallel R_L = -(\beta_F + 1)\left(\frac{v_B}{R_{iB}}\right) R_3 \parallel R_L$$

And since $v_B = v_I$, then, using equation (10.6–1) we see that

$$\boxed{A_V = \frac{v_L}{v_I} = \frac{-\beta_F R_C \parallel R_L}{r_\pi + (\beta_F + 1) R_4}} \qquad (10.6\text{–}5)$$

Well, I suppose that we could now sit back, with equations (10.6–1) thru (10.6–5) and say that we now have all that we need to determine the two–port characteristics necessary to define the BJT common–emitter configuration. As a calculation recipe, that is true. But we can save ourselves a lot of time if we take the liberty of making a few more approximations.

For example, we can assume that for most cases, r_{out} is humongous relative to R_3, typically on the order of MΩ, where R_3 is typically on the order of kΩ, therefore it is not a bad approximation to just identify R_{out} as

$$\boxed{R_{out} \approx R_3} \qquad (10.6\text{–}6)$$

and spare ourselves the calculation effort. Let SPICE compute the 'refined' value, plus any other details that we want.

We also can approximate equation (10.6–5) by dividing numerator and denominator by $(\beta_F + 1)$, for which

$$\frac{v_L}{v_I} = \frac{-\beta_F/(\beta_F + 1) R_3 \parallel R_L}{r_\pi/(\beta_F + 1) + R_4}$$

If we assume that β_F is large so that $\beta_F/(\beta_F+1) \simeq 1$ and that

$$\frac{r_\pi}{\beta_F + 1} \approx \frac{r_\pi}{\beta_F} = \frac{1}{g_m}$$

Then

$$\boxed{\frac{v_L}{v_I} \approx -\frac{R_3 \parallel R_L}{1/g_m + R_4}} \qquad (10.6\text{–}7)$$

If we have a really strong transistor, for which g_m = large, then the voltage transfer gain A_V is just a ratio of resistances in the load over the resistance in the emitter leg. Simple.

Equations (10.6–6) and (10.6–7) are usually accurate to within about 1–2%. That's good enough. Let the refinements be handled by SPICE.

EXAMPLE 10.6–1 Common–emitter amplifier configuration: Analyze the following circuit to determine the amplifier two–port transfer characteristics, R_{in}, R_{out}, v_o/v_I.

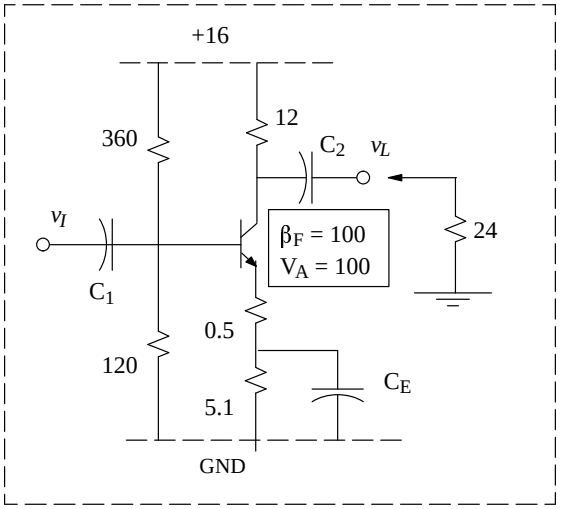


Figure E10.6–1 Common–emitter configuration exercise**.** Capacitances C_1, C_2, C_3 are all assumed to be large

We have a 4–resistance bias network with the emitter resistance split into R_4 and R_5. Then the resistance in the emitter leg is

$$R_E = R_4 + R_5 = 0.5 + 5.1 = 5.6k\Omega$$

We have a voltage–divider supplying the base with bias equivalent values of

$$V_{BB} = \frac{120}{480} \times 15 = 4.0V \quad ,$$

$$R_{BB} = 120 \parallel 360 = 90k\Omega$$

The base current I_B is then

$$I_B = \frac{V_{BB} - V_{BE}}{R_{BB} + (\beta_F + 1)R_E} = \frac{4 - 0.7}{90 + (100 + 1)5.6} = .00503mA$$

and then

$$I_C = 100 \times .00503 = 0.503mA$$

As a check, we should find V_C, V_E and V_{CE}, just to make sure that the BJT is operating in the active regime.

$$V_C = 16 - 0.503 \times 12 = 9.93V \qquad V_E = 0 + (0.503 + .005) \times 5.6 = 2.85V$$

for which V_{CE} = 9.93 – 2.85 = 7.08 V .

We might take note, that since $V_C > V_{BB}$, then the BC junction is reverse–biased for sure, which confirms that the BJT is indeed in the active regime. Therefore determination of V_{CE} as a snake check is somewhat redundant.

This operating point gives us the necessary bias information to determine the transistor parameters g_m, r_π, and r_o., from which we can then determine the two–port characteristics. Since $I_C \simeq 0.5$ mA, then, from equations (10.4–6), (10.5–1) and (10.5–2) we get

$$g_m = \frac{I_C}{V_T} = \frac{0.5}{.025} = 20\ mA/V \qquad g_\pi = \frac{g_m}{\beta_F} = \frac{20}{100} = 0.2\ mA/V$$

and ,

$$g_0 = \frac{I_C}{V_A} = \frac{0.5}{100} = .005\ mA/V$$

From these values of conductance we get resistance values

$$r_\pi = \frac{1}{g_\pi} = \frac{1}{0.2} = 5k\Omega \qquad\qquad r_0 = \frac{1}{g_0} = \frac{1}{.005} = 200k\Omega$$

This information is enough to let us evaluate the input and output characteristics of the example CE configuration. We can start by determining R_{iB}, using equation (10.6–1):

$$R_{iB} = r_\pi + (\beta_F + 1)R_4 = 5 + (100 + 1)0.5 = 55.5k\Omega$$

from which (equation (10.6–2)),

$$R_{in} = R_1 \parallel R_2 \parallel R_{iB} = 360 \parallel 120 \parallel 55.5 = 34.3k\Omega$$

We also can find r_{out}, using equation (10.6–3), for which

$$r_{out} = r_0\left(\frac{r_\pi + (\beta_F + 1)R_4}{r_\pi + R_4}\right) = 100k\Omega \times \left(\frac{5 + 101 \times 0.5}{5 + 0.5}\right) = 1009M\Omega$$

which is pretty darn large. The output resistance is then

$$R_{out} = R_3 \parallel r_{out} = 12 \parallel 1009 = 11.86k\Omega$$

Good grief! R_{out} is close enough to R_3 so that we might just as well assume R_{out} = 12 kΩ and forget about the extra labor of determining r_{out}.

And in that respect, let us compare the results of equations (10.6–5) and (10.6–7). If we use equation (10–6–5) to find A_V, then

$$A_V = \frac{v_L}{v_I} = \frac{-\beta_F R_3 \parallel R_L}{r_\pi + (\beta_F + 1)R_4} = -\frac{100 \times 12 \parallel 24}{55.5} = -14.4V/V$$

Note that we used the fact that the denominator is the same as R_{iB}. If we use equation (10.6–7) to find A_V, we get

$$A_V \approx -\frac{R_3 \parallel R_L}{1/g_m + R_4} = -\frac{12 \parallel 24}{1/20 + 0.5} = -\frac{8}{0.55} = -14.5V/V$$

The result is darn near the same. Might as well use the simpler equation.

Our two–port amplifier characteristics for this example are then

$$(R_{in}, R_{out}, A_V) = (34.3, 12, -14.5)$$

Many of these calculations are simple enough to do by inspection. And we will do so. Let the finer details be taken care of by SPICE.

A modification of the CE topology that we often elect is one in which the resistance R_{E2} is replaced by a current source, as indicated by figure 10.5–2. The advantage of this topology is that the operating current passing through the transistor is independent of the signal transistor, and therefore the circuit will be a little more ideal in its performance.

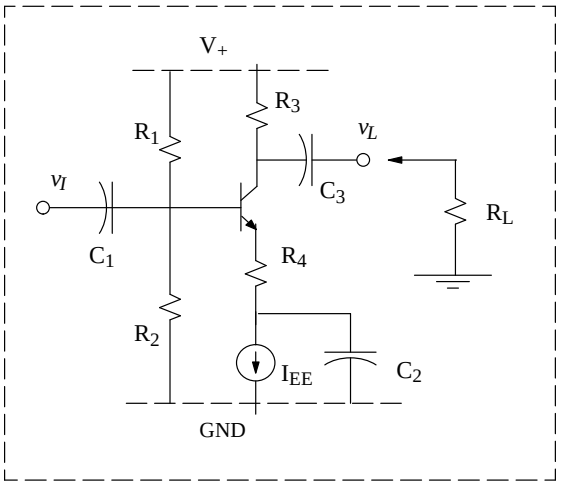


Figure 10.6–2 Common–emitter topology using a current–source bias to define the transconductance g_m and other transistor parameters.

Of course all of the action of the capacitances is the same as for figure 10.6–1, and therefore this circuit has exactly the same small–signal equivalent circuit, and the same durn equations. No change, no sweat. Just like before, except that the transistor parameters g_m, r_π, r_0 are easier to obtain since they depend on knowledge of the current I_C flowing through the transistor.

10.7 SINGLE TRANSISTOR BJT AMPLIFIERS: THE COMMON–COLLECTOR (VOLTAGE–FOLLOWER) CONFIGURATION

There are other options besides the CE topology that are advantageous as signal amplifiers. We can, for instance, take the output off the Emitter instead of the collector node. This topology is indicated by figure 10.7–1

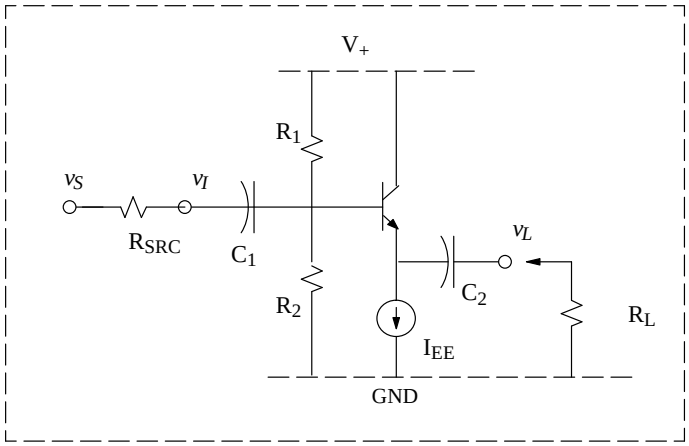


Figure 10.7–1 Common–collector topology using a current–source bias. This topology is also called an Emitter–follower, or more correctly, a voltage–follower circuit.

In this case we have elected to use a current–source bias. We could also have placed a resistance R_E where the fixed current source is located.

We might take note of the fact that resistance R_3 has been removed. We don't really need it unless we take a signal

off of the collector node. And with $R_3 = 0$ we are assured that the collector–base junction is *always* in reverse–bias since V_C is at the highest available bias level. Therefore this topology will always be in the active mode regime.

As in the case of the CE configuration we can construct a small–signal model of this topology by use of the small–signal model of the transistor and the identification that the voltage rails are both linked by their absence of internal resistance and therefore absence of any signal difference between them. This small–signal equivalent of figure 10.7–1 is shown by figure 10.7–2.

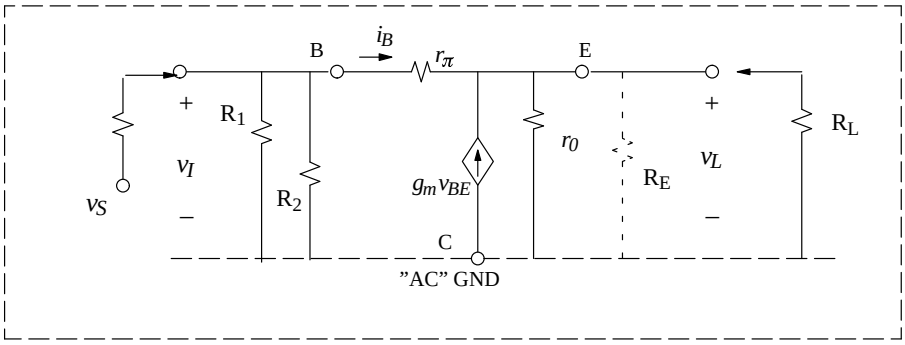


Figure 10.7–2 Two–port small–signal equivalent circuit to figure 10.7–1. If we happen to replace the current source with a resistance R_E, then it would appear as shown in dashed lines.

Note that there is nothing sacred about the orientation nor the rigidity of the small–signal transistor model of figure (10.5–4). We know that the signal is input to the base (B) at the input. We know that it is taken off the emitter (E) at the output. And we know that the collector (C) is connected directly to AC GND. That is the way that figure 10.7–2 is constructed. Then we bend the transistor small–signal model to fit this topology.

If we pretend that we are an electron and look into the base, we will see a resistance just like we saw "looking into" the base of the CE configuration. In this case, all that we see connected to the emitter is the load R_L, therefore,

$$\boxed{R_{iB} = \frac{v_B}{i_B} = r_\pi + (\beta_F + 1)R_L} \qquad (10.7\text{–}1a)$$

After all, the relationship between i_B and i_E is still a factor of $(\beta_F + 1)$. And resistance r_π is in series with the emitter–multiplied term, just like for the CE configuration.

If we happen to have the R_E included in the emitter leg, then topologically it falls in parallel with R_L, so that

$$\boxed{R_B = \frac{v_B}{i_B} = r_\pi + (\beta_F + 1)(R_E \parallel R_L)} \qquad (10.7\text{–}1b)$$

and the input resistance is then

$$\boxed{R_{in} = R_{iB} \parallel R_1 \parallel R_2} \qquad (10.7\text{–}2)$$

Now, if we look at the output node, which in this case is node E, and do a nodal analysis, then

$$v_L(g_O + g_\pi + G_L) - v_B g_\pi - g_\pi v_{BE} = 0$$

Since $v_{BE} = v_B - v_E$, and since $v_E = v_L$ and $v_B = v_I$, then

$$v_L(g_O + g_\pi + G_L) - v_I g_\pi - g_m(v_I - v_O) = 0$$

Solving in terms of v_L and v_I, we see that the voltage transfer gain is:

$$\boxed{\frac{v_L}{v_I} = \frac{g_m + g_\pi}{g_m + g_\pi + g_0 + G_L}} \qquad (10.7\text{–}3)$$

And, if we are a little more cavalier about accuracy, and recognize that $g_0 << g_m$ and even $g_\pi << g_m$, then

$$\boxed{\frac{v_O}{v_I} \approx \frac{g_m}{g_m + G_L}} \qquad (10.7\text{–}4)$$

If we do include a resistance R_E in the emitter leg, then the load on the emitter signal is $R_E||R_L = R_L'$. Then we can make a slight modification:

$$\boxed{\frac{v_O}{v_I} \approx \frac{g_m}{g_m + G_L'}} \qquad (10.7\text{–}5)$$

Since g_m is usually a reasonably large conductance and since the ratio is of positive sign, then $v_O/v_I \lesssim 1$, for which we can say that the output follows the input. So the circuit of figure 10.7–1 is therefore often called an *emitter–follower*, or more correctly, a *voltage follower* topology.

The output resistance can be obtained by assessing the current at the output node of the transistor when there is zero applied signal, $v_S = 0$, to the input node. When this is the case, the small–signal circuit can be thought of as being of the form as shown by figure 10.7–3

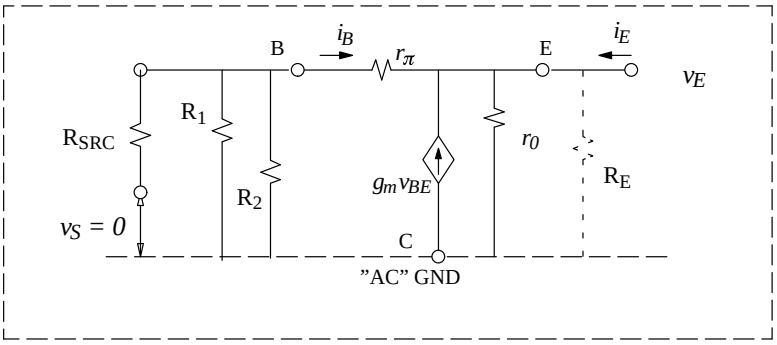


Figure 10.7–3 Assessment of output resistance. When we evaluate the output resistance at the output terminal it is necessary to have input signal = 0.

We can simplify the circuit of figure 10.7–3 considerably by condensing the resistance at the base to be of the form,

$$\boxed{R_{BS} = R_{SRC} \parallel R_1 \parallel R_2} \qquad (10.7\text{–}6)$$

for which, we would have a simpler circuit of the form as represented by figure 10.7–4

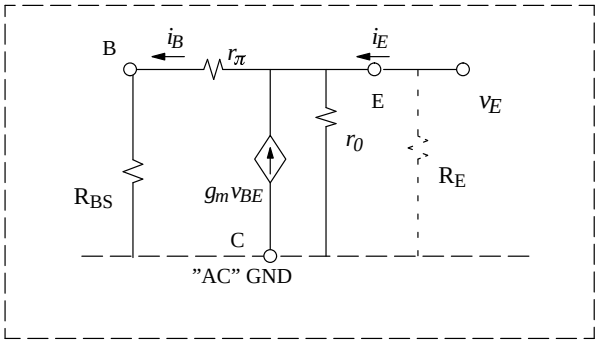


Figure 10.7–4 Assessment of output resistance, simplified.

If we make a nodal analysis at E, then

$$i_E = v_E(g_0 + g_\pi) - v_B g_\pi - g_m v_{BE}$$

But $v_{BE} = v_B - v_E$, so that

$$i_E = v_E(g_0 + g_\pi + g_m) - v_B(g_\pi + g_m) \approx v_{BE}(\beta_F + 1)g_\pi$$

neglecting the current small contribution g_0. We can determine v_{BE} from figure 10.7–4 by means of the voltage divider of r_π and R_{BS}, for which

$$v_{BE} = \frac{r_\pi}{r_\pi + R_{BS}} v_E$$

so that

$$i_E = v_E \frac{(\beta_F + 1) r_\pi g_\pi}{r_\pi + R_{BS}}$$

which gives a resistance "looking into" the emitter $\equiv Ri_E$, of

$$\boxed{R_{iE} = \frac{v_E}{i_E} = \frac{r_\pi + R_{BS}}{\beta_F + 1}} \qquad \textit{(10.7–7a)}$$

This result can also be expressed as

$$R_{iE} = \frac{r_\pi}{\beta_F + 1} + \frac{R_{BS}}{\beta_F + 1} \boxed{\approx \frac{1}{g_m} + \frac{R_{BS}}{\beta_F}} \qquad \textit{(10.7–7b)}$$

Since the resistance network connected to the base is reduced by a factor of $(\beta_F + 1)$, we often call this result, "inverse emitter multiplication". Naturally, this means that the resistance 'looking into' the emitter is *small.*

The output resistance is approximately the same as that given by equation (10.7–7) unless we happen to have an emitter resistance R_E in the bias leg of the circuit. Then

$$\boxed{R_{out} = R_{iE} \parallel R_E} \qquad \textit{(10.7–8)}$$

We might look at the three characteristic equations (10.7–2), (10.7–4) and (10.7–8). As indicated by these equations, the input resistance should be moderate–to–high, the output resistance should be low, and the voltage transfer gain should be nearly equal to unity, and of the same phase as the input signal. Therefore this circuit is often used as a 'buffer' stage. In this respect the high output resistance of a transducer can be matched to the relatively high input resistance of the emitter (voltage) follower. The voltage follower then can transfer the signal, almost one–to–one to a low–resistance output drive, for which it can easily drive a next stage, maybe one of the form of the CE configuration, which will more voltage signal gain, if that is desired.

10.8 SINGLE TRANSISTOR BJT AMPLIFIERS: THE COMMON–BASE (CURRENT–FOLLOWER) CONFIGURATION

As indicated by the small–signal model of the BJT signal current is controlled by the signal bias v_{BE}. We can therefore apply an input signal either to the base (B) or the emitter (E) to control the BJT. Another option is therefore one like that shown by figure 10.8–1, in which the input signal is applied to the emitter and the output is taken off the collector. The base may be shunted to AC ground by means of a capacitance, as shown. This configuration is called the *common–base* configuration, or the *current–follower* configuration.

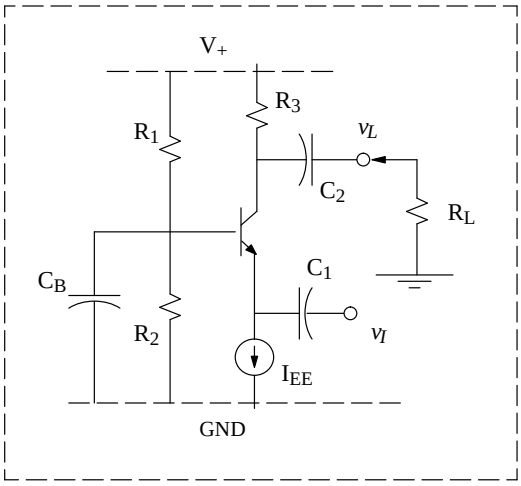


Figure 10.8–1 Common–base topology using a current–source bias.

We also could use a resistance R_E in place of the current source I_{EE}. Taking the same approach as done before, in which we construct a small–signal equivalent circuit for figure 10.8–1, we get the circuit of figure 10.8–2.

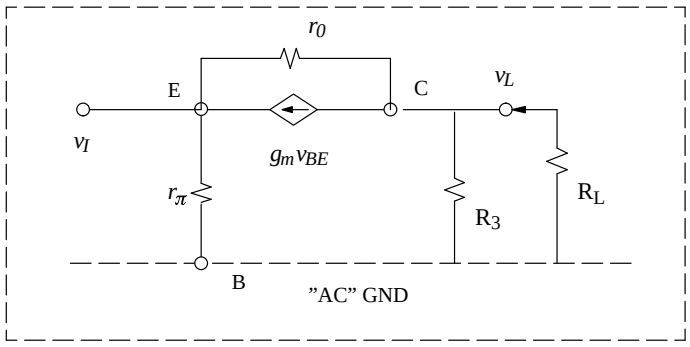


Figure 10.8–2 Small–signal equivalent model of the common–base configuration. Note that the bias resistances R_1 and R_2 are shunted by capacitance C_B and so do not appear in the small–signal circuit.

The input resistance is just the resistance that we would see "looking into" the emitter., just like that given by equation (10.7–7), except that $R_{BS} = 0$, since all of the resistances at the base node are shunted to AC ground by the capacitance C_B. Therefore the input resistance is

$$R_{in} = \frac{r_\pi}{\beta_F + 1} \approx \frac{1}{g_m} \qquad (10.8\text{–}1)$$

If we take a nodal analysis at node C, then we will get the equation

$$v_L(G_L + G_3 + g_0) - v_E g_0 + g_m v_{BE} = 0$$

And since $v_{BE} = v_B - v_E = -v_E$, since v_B is at signal GND, then

$$v_L(G_L + G_3 + g_0) - v_E(g_0 + g_m) = 0$$

for which we get the voltage transfer gain

$$\frac{v_L}{v_E} = \frac{v_L}{v_I} = \frac{g_m + g_0}{G_L + G_3 + g_0}$$

Or, neglecting the small conductance g_0, the voltage transfer gain is

$$\boxed{\frac{v_L}{v_I} \approx \frac{g_m}{G_L + G_3}} \qquad (10.8\text{–}2)$$

Now, the output resistance, for $v_I = 0$, will be just the resistances r_0 and R_3 in parallel, since, with $v_I = v_E = 0$, the current source is turned off. Then

$$\boxed{R_{out} = r_0 \parallel R_3 \approx R_3} \qquad (10.8\text{–}3)$$

Now, suppose that we elect to determine the current transfer ratio i_L/i_I . Using the chain rule, we get

$$\frac{i_L}{i_I} = \frac{i_L}{v_L} \times \frac{v_L}{v_I} \times \frac{v_I}{i_I} = G_L \times \left(\frac{g_m}{G_L + G_3} \right) \times \frac{1}{g_m}$$

which gives:

$$\boxed{\frac{i_L}{i_I} = \frac{G_L}{G_3 + G_L}} \qquad (10.8\text{–}4)$$

Hey! –This is just an equation for a current divider at the output!

What this result tells us is that this circuit topology is of the form of a *current* follower. The input current signal is transmitted to the output as a an approximately unity transfer ratio, then divided by the current divider at the output.

10.9 SINGLE TRANSISTOR BJT AMPLIFIERS: OVERVIEW AND APPROXIMATIONS

The three topologies that were analyzed in the three previous sections are the only three realistic circuit options. We may choose to make some variation in the bias networks or add feedback resistances, but as far as amplifier building blocks are concerned, these three is all thar is.

Naturally we can analyze them using the two–port fomulae, as listed by table 10.9–1. These formulae will provide all of the two–port characteristics necessary. But they are *not* highly accurate, and should not be treated as if they are. The only way that we can acquire an accurate analysis of performance characteristics is to put them through a circuit simulation. Even then, with normal variation in component parameters, we should not expect results any more accurate that to three significant figures.

Table 10.9–1 Formulas that describe the two–port characteristics for the three topologies

CE config:

$$R_{in} = R_{BB} \parallel R_{iB} \qquad R_{out} = R_3 \parallel r_{out}$$

$$\frac{v_L}{v_I} = \frac{-\beta_F G_B}{G_{out} + G_L} \approx \frac{-R_3 \parallel R_L}{R_4 + 1/g_m}$$

where:

$$R_{iB} = r_\pi + (\beta_F + 1)R_4$$

$$r_{out} = r_o\left(\frac{r_\pi + (\beta_F + 1)R_4}{r_\pi + R_4}\right)$$

$$R_{BB} = R_1 \parallel R_2$$

Emitter follower (Voltage follower)

$$R_{in} = R_{BB} \parallel R_{iB} \qquad R_{out} = R_{iE} \parallel R_4$$

$$\frac{v_L}{v_I} = \frac{g_e}{g_e + G_4 + G_L} \approx \frac{g_m}{g_m + G_4 + G_L}$$

where:

$$R_{iE} = \frac{r_\pi + R_{BB} \parallel R_{src}}{\beta_F + 1}$$

$$R_{iB} = r_\pi + (\beta_F + 1)(R_4 \parallel R_L)$$

$$g_E = \frac{1}{r_E} = g_m + g_\pi$$

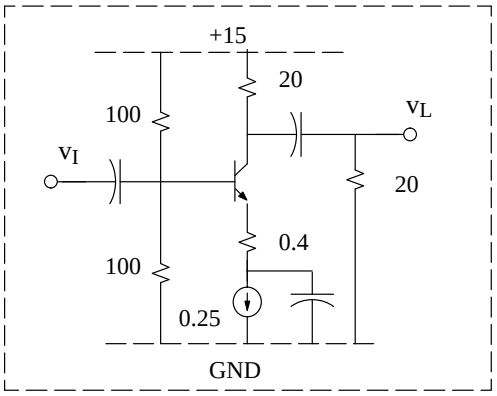
Common base (Current follower)

$$G_{in} = G_4 + g_m + g_\pi \qquad R_{out} = r_{out} \parallel R_3$$

$$\frac{v_L}{v_I} = \frac{g_o + g_m}{g_o + G_3 + G_L} \qquad \frac{i_L}{i_I} \approx \frac{G_L}{G_3 + G_L}$$

Given the simplicity of the approximations included in table 10.9–1, and the fact that accuracy is not to be expected, many of these topologies can be analyzed by inspection. Consider the following example.

EXAMPLE 10.9–1 CE Amplifier topology



Defaults: Capacitances large
Resistances in kΩ
Currents in mA

Assuming default $\beta_F = 100$, the transistor parameters are,

$$g_m \approx 0.25 \times 40 = 10\ mA/V \qquad r_\pi = 100/g_m = 10k\Omega$$

Note that we assume that I_C is approximately the same as the current specified by the current source. The minor difference between I_E and I_C represents a fringe correction, which we might as well ignore.

Also note: We very often do not know the value of β_F, and so we assume $\beta_F = 100$, unless we know otherwise.

Then input resistance R_{iB} to the base of the BJT is

$$R_{iB} \approx r_\pi + 100 \times 0.4 = 50k\Omega$$

Then the input resistance is (approximately)

$$R_{in} \approx 100 \parallel 100 \parallel 50 = \boxed{25k\Omega}$$

the output resistance *Rout* is (approximately)

$$R_{out} \approx R_3 = \boxed{20k\Omega}$$

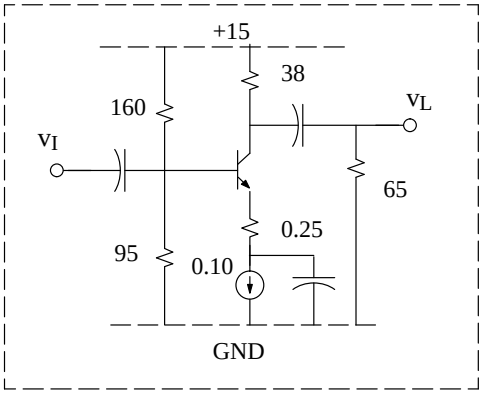
and the voltage transfer gain is (approximately)

$$\frac{v_L}{v_I} \approx -\frac{20 \parallel 20}{1/10 + 0.4} = \boxed{-20\ V/V}$$

Note that we did not have to even make a sideways glance at our calculators to do this exercise.

Even if the numbers are a little less convenient, the imprecise nature of the results accommodates an educated estimate. For example, consider the following example

EXAMPLE 10.9–2 CE Amplifier topology



The transistor parameters are

$$g_m \approx = 4\ mA/V \qquad r_\pi = 100/g_m = 25k\Omega$$

The input resistance is

$$R_{in} \approx 160 \parallel 95 \parallel 60 \approx 150 \parallel 100 \parallel 60 \approx \boxed{30k\Omega}$$

The output resistance is

$$R_{out} \approx \boxed{38k\Omega}$$

and the voltage transfer gain is

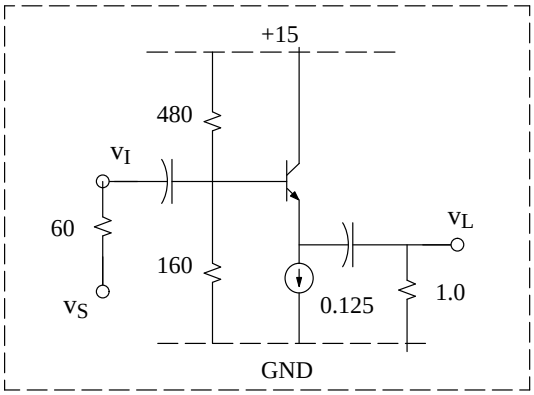
$$\frac{v_L}{v_I} \approx \frac{-38 \parallel 65}{1/4 + 0.25} \approx -\frac{24}{0.5} \approx \boxed{-48\ V/V}$$

As long as we are willing to recognize that there is no need for us to make a high accuracy calculation, then the quick, rough approximations made in example 10.9–2 are adequate. *Usually estimates within 10% are sufficient.* More precise assessments can be readily obtained from a simulation analysis using SPICE.

This estimate process can also be applied to the other topologies. Consider the following example:

EXAMPLE 10.9–3 Voltage–follower topology

Defaults: Capacitances large
Resistances in kΩ
Currents in mA



Assuming default β_F = 100, the transistor parameters are,

$g_m \approx 0.125 \times 40 = 5\ mA/V$ $\qquad$ $r_\pi = 100/g_m = 20k\Omega$

Then input resistance R_{iB} to the base of the BJT is

$$R_{iB} \approx r_\pi + 100 \times 1.0 = 120k\Omega$$

Then the input resistance is (approximately)

$$R_{in} \approx 480 \parallel 160 \parallel 120 = 120 \parallel 120 = \boxed{60k\Omega}$$

the output resistance *Rout* is (approximately)

$$R_{out} \approx \frac{r_\pi + 60 \parallel 480 \parallel 160}{\beta_F} \approx \frac{20 + 60 \parallel 120}{100} = \boxed{0.6k\Omega}$$

and the voltage transfer gain is (approximately)

$$\frac{v_L}{v_I} \approx \frac{5}{5+1} = \frac{5}{6} = \boxed{0.83\ V/V}$$

Note that this transfer gain is always less than unity. The source–to–load transfer gain can also be determined,

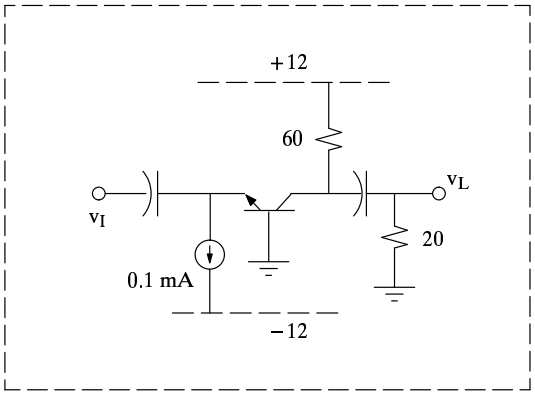
$$\frac{v_L}{v_S} = \frac{R_{in}}{R_{SRC} + R_{in}} \times \frac{v_L}{v_S} = \frac{60}{60+60} \times \frac{5}{6} \approx \boxed{0.42\ V/V}$$

No sweat.

More refined analysis of the two–port transfer characteristics for this topology, or for any other, is a task for SPICE.

As a final example, consider the current–follower topology. In this case we will choose to use a bipolar power supply, so that base bias by means of the R1, R2 voltage divider is unnecessary.

EXAMPLE 10.9–4 Current–follower topology



Assuming β_F = 100, (default) the transistor parameters are,

$g_m \approx 0.1 \times 40 = 4\ mA/V$ $\qquad$ $r_\pi = 100/g_m = 205k\Omega$

Then input resistance is the resistance R_e 'looking into' the emitter, and is

$$R_{in} = \frac{1}{g_m + g_\pi} \approx \frac{1}{g_m} = \boxed{0.25k\Omega}$$

The output resistance is approximately

$$R_{out} \approx R_3 = \boxed{60k\Omega}$$

and the current transfer ratio, for the current divider shown, is approximately

$$\frac{i_L}{i_I} = \frac{1/20}{1/20 + 1/60} \approx \boxed{0.8A/A}$$

If we want to find the voltage transfer ratio, then

$$\frac{v_L}{v_I} = \frac{i_I}{v_I} \times \frac{i_L}{i_I} \times \frac{v_L}{i_L} = g_m \times \frac{i_L}{i_I} \times R_L = 4 \times 0.8 \times 20 \approx \boxed{+64V/V}$$

So, as we see, analysis of this circuit is also very simple, provided we accept a little slop in the execution.

As a summary, we accept the following table of topology–oriented approximations

Table 10.9–2 Approximations for the three topologies

CE config:

$R_{in} = R_1 \| R_2 \| R_B$ where: $R_B \approx r_\pi + \beta_F R_4$

$R_{out} \approx R_3$ $\qquad$ $\frac{v_L}{v_I} \approx \frac{-R_3 \| R_L}{1/g_m + R_4}$

Common base (Current follower)

$G_{in} \approx G_E + g_m$ $\qquad$ $R_{out} \approx R_3$

$\frac{i_L}{i_I} \approx \frac{G_L}{G_3 + G_L}$

Emitter follower (Voltage follower)

$R_{in} = R_1 \| R_2 \| R_B$ $\qquad$ $R_{iB} \approx r_\pi + \beta_F(R_E \| R_L)$

$R_{out} = R_{iE} \| R_E$ where: $R_{iE} \approx \frac{r_\pi + R_{BS}}{\beta_F}$

$\frac{v_L}{v_I} \approx \frac{g_m}{g_m + G_E + G_L}$

CHAPTER SUMMARY:

For the class of transistors that we define as being of type BJT (bipolar junction transistor),

$$g_m = \frac{I}{V_T} \quad \approx 40I \text{ at normal room temperatures} \qquad (10.1\text{–}2)$$

where *I* is the operating point current flowing through the transistor. The transistor is assumed to be in the active regime for equation (10.1–2) to be valid.

For the class of transistors that we define as being of type FET (field–effect transistor),

$$g_m = 2\sqrt{KI} \qquad (10.1\text{–}3)$$

where I is the operating point current flowing through the FET. The FET must be be in the active regime for equation (10.1–3) to be valid.