

# Analog Hardware Neural Networks using Logarithmic Four-Quadrant Multiple Circuits

Masashi Kawaguchi  
Department of Electrical &  
Electronic Engineering  
National Institute of Technology,  
Suzuka College  
Suzuka, Japan  
masashi@elec.suzuka-ct.ac.jp

Naohiro Ishii  
Information Systems Architecture  
Course  
Advanced Institute of Industrial  
Technology  
Tokyo, Japan  
nishii@acm.org

Masayoshi Umeno  
Department of Electronic  
Engineering  
Chubu University  
Kasugai, Japan  
umeno@isc.chubu.ac.jp

**Abstract**—In the artificial intelligence, machine learning and neural network fields, many practical use models have been proposed. However, these models are based on a digital Von Neumann model's computer. There are a minority of studies in the field of analog learning neural networks. In our previous study, we used multiple circuits as connecting weights. Multiple circuits calculate the product of the two input values, input signals and connecting weights. However, the working range is very small because of the semiconductor characteristics. When constructing a network, one of the disadvantages is that the input and output range is limited. Furthermore, the circuit operation becomes unstable because of the characteristics of the multiple circuit. In this study, we proposed logarithmic four-quadrant multiple circuits as a connecting weight. From the experimental result, it is shown that this circuit operates stably over a wide range. The model works using pure analog electronic circuits. The learning time is quite short compare to a digital process computer. We improved the number of units and network layers. Moreover, we suggest the possibility of the realization of the hardware implementation of the deep learning model.

**Keywords**—Hardware Neural Network, Multiple Circuits, Logarithmic Circuits.

## I. INTRODUCTION

Recently, multilayer neural network models, in particular, a deep learning model, have been researched intensely. Performance has been greatly improved in the specialty of image / sound recognition. The internal mechanism of the recognition system is revealed more clearly; self-learning integrated circuit (IC) chips have also been realized. However, these models are operating on a general purpose Von Neumann model's computer with the application system. There are a minority of studies that construct an analog parallel hardware structure using a biological information processing mechanism. Proposed now is the neural network machine learning model with a pure analog network electronic circuit. Such a model will develop an original recognition or prediction system using the analog neural electronic circuit. In the field of multilayer learning models, many useful models such as image recognition or phenomenon prediction have been proposed. And there are many hardware realization models such as an image / sound sensor using large-scale parallel computer.

In this study, we proposed logarithmic four-quadrant multiple circuits as a connecting weight. From the experimental result, it is shown that this circuit operates stably over a wide range. The model works using pure analog electronic circuits. The learning time is quite short compare to a digital process computer.

## A. Analog Hardware Neural Network

The main strength of an analog machine learning network, is that its operation is realized by the real time linear system, not due to clock frequency behavior. On the other side, digital system behavior is due to the clock operation by the central processing unit (CPU) based on a Neumann computer. In previous research, innovative analog neural models were proposed [1-2]. In the complete analog circuit, one element is the is used for the implementation of the analog data saving unit, keeping the analog numerical value for a while time using analog memory [3]. The dynamic random access memory (DRAM) can be memorized in the condenser memory in a short period of time, because it was performed in the generic complementary metal oxide semiconductor (CMOS) [4]. However, when the charge is maintained for a long time in the capacitor, it needs the processing system to keep the numerical value data in the memory. The refresh process is required. Capacitors reduce the electric charge over time. It is not difficult to get back the electric charge of a condenser by a refresh process utilization in the general digital binary memory. Nevertheless, in the situation using analog memory, the refresh process is not easy because the memorizing data is linear analog data, it needs the time analysis system of electronic charge reducing curve. Other researchers proposed the memorize methods of connecting weights, the floatage gate type device [5] and magnetic substance memories [6].

## B. Pulsed Neural Network

Pulsed neural networks receive a great number of pulses as learning data and change the connecting weights due to the number of pulses. Such networks can maintain their connecting weights after learning by the number of pulses and outputs of the signal depending on the input value [7]. Nevertheless, it is necessary for a long time for learning because a great number pulses are required before complete learning. For example, the time interval average of the pulse is 10uS and 100 pulse are

needed before finishing the learning procedure. Approximately 1mS is needed to finished the learning.

### C. How to realize the Variable Connecting Weights?

Early analog hardware neural network models were configured with the operational amplifier and the resistance element. It is difficult to change the value of solid resistance for the learning process. In our previous study, proposed was a movement detection biomedical vision model using analog general electronic circuits. The suggested model is composed of four layers. There are differentiation circuit, difference circuit and multiple circuits in each layer for detecting pure motion output. From a technical standpoint, the proposed model makes elucidation of the artificial vision system mechanism possible, which can detect the target object, motion and velocity by the design and simulation using an analog network electric circuit [8-9]. On the other hand, there was an attempt to realize a multi-layered hardware neural network using an analog electronic circuit. In the machine learning and neural network field, many practical use models have been proposed. But, these models are based on a digital general Neumann computer. There are few practical studies concerning analog learning neural networks. Early analog circuits network models were configured of the difference circuits, multiple circuits and solid resistance. It is not easy to change the value of solid resistance for the learning process.

At first, a hardware neural network using variable resistance elements as the connecting weights was constructed. In the learning operation process, each resistance value needs to be adjusted by hand. Next, multiple circuits were used as the connecting weights. Multiple circuits can calculate the products of a two input signal. One is an input signal value. Another input as the connecting value is considered. In the former study, three layered neural network analog electronic circuits were designed. The model used multiple circuits by opamp and a metal-oxide-semiconductor field-effect transistor (MOSFET) as the connecting weights. The connecting weights vary easily by controlling the input signal. The model has two input units and one output unit with three layers. After the learning process, the model worked Exclusive OR (EX-OR) logic as the simulation program with integrated circuit emphasis (SPICE) simulation. This is a linear inseparable problem [10-11].

## II. NEURAL NETWORK BY ANALOG ELECTRONIC CIRCUIT

### A. Neural Network using Solid or Variable Resistance Elements

Early analog neural circuits models were configured of the difference circuits, multiple circuits and solid resistance. It is not easy to change the value of solid resistance for the learning process described in Fig.1. In past research, a hardware neural network was constructed using variable resistance. This variable resistance means the connecting weights of the network. The network has 9 units in the input layer, 3 units in the middle layer and 3 units in the output layer. The system was able to recognized simple patterns by pure analog circuits [12]. However, in the learning process, each resistance value needs to be adjusted by hand.

### B. Neural Network using Multiple Circuits

In our previous study, multiple circuits were utilized as the connecting weights. The connecting weights could be easily changed by controlling the input signal. Figure 2 shows the 2-input and 1-output neural circuit. It means the structure of one neuron. There are three input units, two input signals and one threshold value. The input unit calculates the product of two voltages, input signal value and connecting weights. The connecting weights can be easily changed by operating the voltage of the MOSFET Gate signal in Fig. 2. Next, a learning neural network was constructed. It is a two-input unit and one-output unit basic perceptron model with a feedback circuit. Fig. 2 also shows the perceptron network of analog electronic circuits [14].

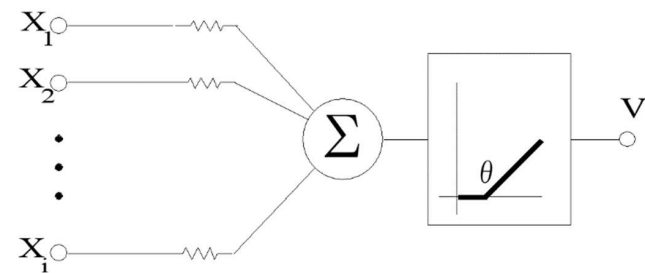


Fig. 1. Neuron model using resistance elements

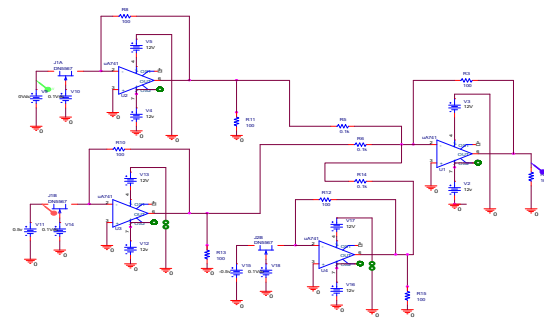


Fig. 2. Neuron model using multiple circuits

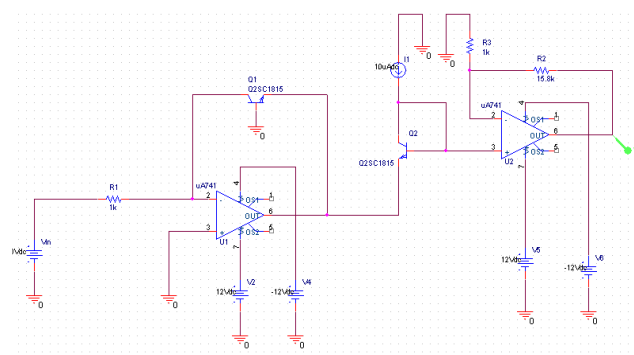


Fig. 3. Logarithmic conversion circuit

## III. LOGARITHMIC QUADRANT MULTIPLE CIRCUIT

In the previous section, the hardware learning network is explained. Although, in the situation of setting up a network, there is one problem. The operating range of the input and output

voltage level is limited. Moreover, the circuit behavior is sometimes unstable because of the multiple circuit feature using a semiconductor. It is called ‘Circuit Limitations’. One reason is a semiconductor specificity. Not all semiconductors are manufactured equally. Another reason is the output-voltage limitation of the semiconductor element. To solve this problem, we proposed logarithmic four-quadrant multiple circuits as a connecting weight. This circuit is composed of a Logarithmic circuit, additional circuit, exponential circuit, inverse circuit, comparator circuit, absolute circuit and analog switch. This circuit operates more stably than previous models. And this circuit has a wide operating range.

#### A. The Logarithmic Circuit and the Inverse Logarithmic Circuit

We show the logarithmic conversion circuit in Fig.3. When the base-emitter potential of the two transistors is small, the output is proportional to the logarithm ratio of the collector currents between the two transistors. The first stage operational amplifier performs logarithmic conversion. Since the base-emitter voltage of the first-stage transistor cannot be increased, the second-stage operational amplifier outputs the amplified signal of the first-stage operational amplifier. On the other hand, we show the inverse logarithmic conversion circuit in Fig.4. It indicates the exponential conversion circuit.

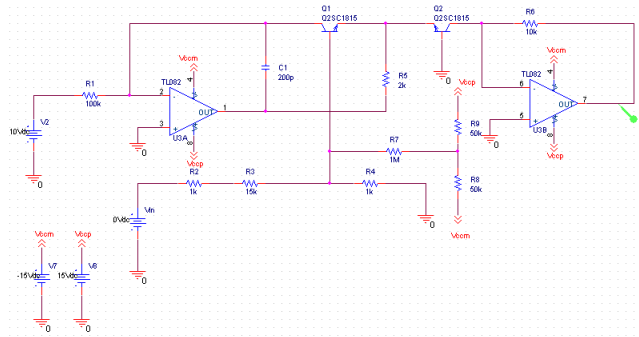


Fig. 4. Inverse Logarithmic Conversion Circuit (Exponential conversion circuit)

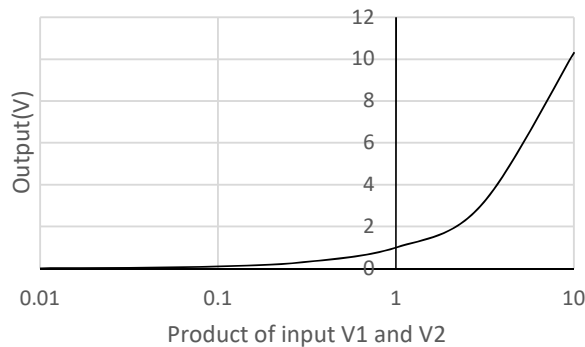


Fig. 5. Simulation result of Logarithmic Multiple Circuits.

#### B. The Multiple Circuit using Logarithmic Circuit

The mechanism of the multiple circuit is as follows. First, two logarithmically converted signals are input to the adder

circuit. Next, the output of the adder circuit is input to the inverse logarithmic conversion circuit. The output is the product of the two original input signals. This logarithmic multiple circuit is stable compared with the previous multiple circuit. Figure 5 shows the simulation result of Logarithmic Multiple Circuits. The horizontal axis of the logarithmic scale is the product of the input voltage. The vertical axis represents the output voltage. Although there is a slight error, it is shown that the multiplication circuit is operating in a wide range. However, the input voltage range is positive only because of the logarithmic characteristics. To realize a neural network, the four quadrants multiple circuit is required.

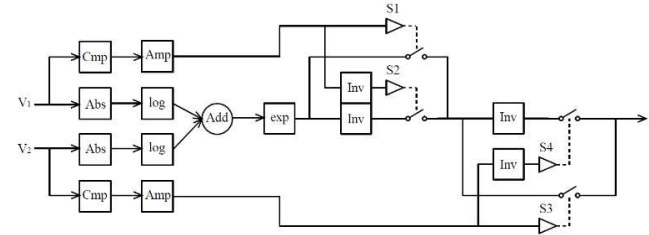


Fig. 6. Example of a figure caption. (figure caption)

#### C. The Logarithmic Four-Quadrant Multiple Circuits

Figure 6 shows the diagram of the logarithmic four-quadrant multiple circuits. These circuits are composed of an logarithmic circuit, additional circuit, exponential circuit, inverse circuit, comparator circuit, absolute circuit and analog switch. First, the input voltage  $V_1$  and  $V_2$  are converted to a positive value by the absolute value circuit. Next, positive values are input to the logarithmic conversion circuit. Each logarithmic value is input to the adder circuit. The output of the adder circuit is input to the inverse logarithmic conversion circuit, the exponential function circuit. The output of exponential function circuit is equal to the product of inputs  $V_1$  and  $V_2$ . However, this is the absolute value of product.

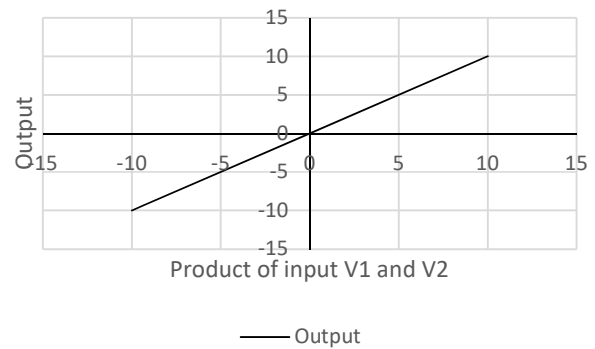


Fig. 7. Simulation result of logarithmic four-quadrant multiple circuits

On the other hand, inputs  $V_1$  and  $V_2$  are also input to the comparison circuit, respectively. The comparison circuit compares the ground voltage and the input voltage. If the input voltage is positive, a positive constant value is output. Alternatively, if the input voltage is negative, a negative constant value is output. The output of the comparison circuit becomes the input of the amplifier circuit. This circuit amplifies

the operating voltage of the next-stage analog switch. If  $V_1$  is positive, the analog switch  $S_1$  operates. The output of the exponential function circuit is flows to the next stage. On the other hand, If  $V_2$  is negative, the analog switch  $S_2$  operates. The output of the exponential function circuit is inverted and flows to the next stage. Thus, the output value of the analog switch is the product of  $V_1$  and  $V_2$ , and the positive and negative signs are the same as  $V_1$ . In the same way, by the analog switch  $S_3$  and  $S_4$ , if the value of  $V_2$  is positive, the current is flows to the output. Alternatively, if the value of  $V_2$  is negative, the current is inverted and flows to the output. Finally, the output value is the product of inputs  $V_1$  and  $V_2$ . This circuit operates as a four-quadrant multiplier.

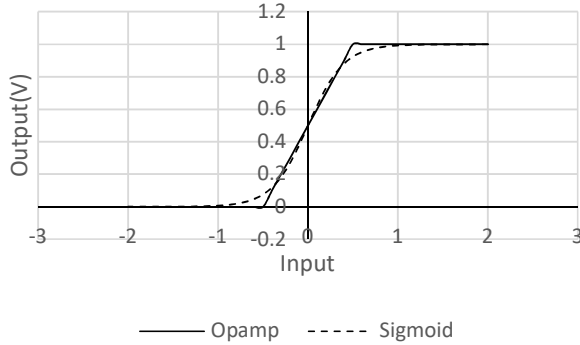


Fig. 8. The output of Opamp and Sigmoid function.

Figure 7 shows the simulation result of logarithmic four-quadrant multiple circuits. The horizontal axis is the product of the input voltage. The vertical axis represents the output voltage. The graph is a straight line. Although there is a slight error, it is shown that the four-quadrant multiplication circuit is operating in a wide range. The horizontal axis of the graph is the product of the output voltages, and the vertical axis is the output of the four-quadrant multiplication circuit. It is shown that the four-quadrant multiplication circuit operates stably over a wide range. In our previous research, the input operating voltage was in the range of approximately  $\pm 200$  mV. And the output operating voltage was in the range of approximately  $\pm 1$  V in the reason of circuit limitation [14]. Due to the wide operating voltage range, this circuit has excellent stability.

#### D. The Activation Function of Proposed Neural Network

The proposed circuit is based on an operational amplifier. The activation function of the neural network can be approximated by an operational amplifier. Figure 8 shows the characteristics of the operational amplifier and sigmoid function, which is typical activation function. The output of the operational amplifier is similar to the sigmoid function.

#### E. The Feedback Circuit of Neural Network Learning

We designed the feedback circuit of neural network learning as shown in Fig. 9. It is the separate neural network of each teaching signal, “T<sub>1</sub>” and “T<sub>2</sub>”. This model is possible of real time learning. In Figure 9, “Mul” means multiple circuits, “Add” means additional circuits and “Sub” means subtraction circuits. And this figure extracts only a learning feedback part of back propagation network. There are two input lines,  $I_1$ . However,

$I_1X_1$  and  $I_1X_2$  are each learning pattern. In the additional circuit, the each products of multiple circuit are added, they are  $X_1W_1$  and  $X_1W_2$ . In the same way, the each products  $X_2W_1$  and  $X_2W_2$  are added by the additional circuit. Next, the subtract circuit calculates the error between the output of additional circuit and teaching signal. Finally, the another subtract circuit calculates the original connecting weight and the total error. This subtract circuit outputs the new connecting weights. This is a simplification figure, showing the one input signal, one output signal and two kinds of learning patterns.

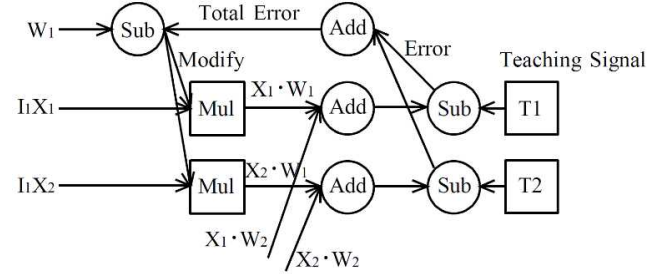


Fig. 9. The structure of 2-input, 1-output, 2-patterns and 3-layers analog neural network

#### IV. THREE LAYERS NEURAL NETWORK

We constructed a three layer neural network, an input layer, middle layers and an output layer. There are two input units, two middle units and one output unit. We combined the neural unit described in the preceding chapter. In Figure 10, we show the block diagram of a general neural network model. This figure has been simplified; the connecting weight part and feedback part are omitted. It uses the multiple circuit for easy changing of the connecting weight. “Mul” means multiple circuits and “Add” means addition of circuits in Fig. 10. Due to the characteristics of the circuit, one unit is required for each learning pattern. The model described in Fig. 8 indicates the neural network two input pattern and two kinds of learning patterns.

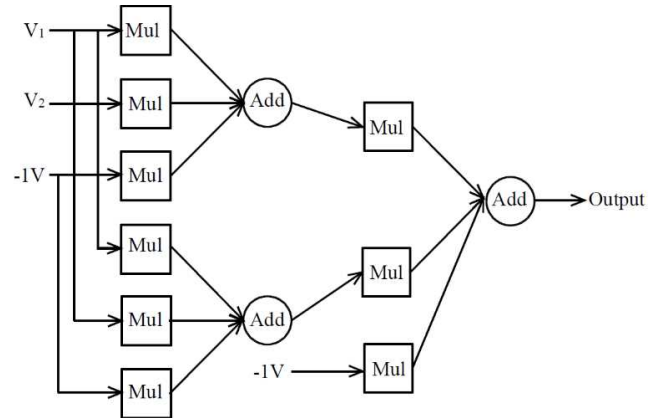


Fig. 10. Three layers neural network

The experimental result is shown in Fig. 11. We confirmed when the range of the voltage is between -0.05V and 0.15V, this circuit operated normally. The linear graph is the output of middle layer and the dotted liner graph is the output of the final layer in Fig. 9[11]. In the middle layer, we realized a good output

signal. In the output layer, we obtained a little distortion signal. However, this will not present a significant problem on the neural network output.

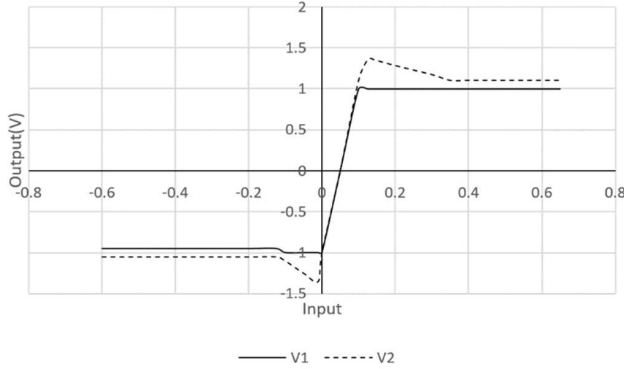


Fig. 11. Experimental Result of Three-Layers Neural Circuits.

## V. DEEP LEARNING MODEL

Recently, a deep learning model has been proposed. Deep learning is a kind of algorithms in the learning model. It attempts high-level categorizing of data using multiple non-linear transformations and one method of machine learning. In the field of image recognition and speech recognition, the deep learning method has attracted the attention.

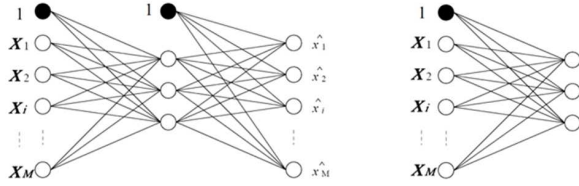


Fig. 12. Learning the Auto-encoder and Removing the Decoding Part of Stacked Auto-encoder

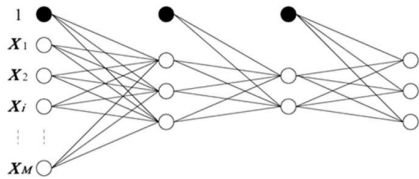


Fig. 13. The Compressed Internal Representation.

### A. The stacked auto encoder

The stacked auto-encoder is one method of deep learning. This is the pre-learning method of a large number layer network. How to construct the deep layer network is as follows. After the learning process of the stacked auto-encoder is completed, the decoding part (output layer) of stacked auto-encoder is removed and the coded portion (from the input layer to the intermediate layer) is kept as in Fig. 12. Thus, we obtain the network which converts from input signal to compressed information representation in Fig. 13. Moreover, we obtain a more compressed internal representation, as the compressed representation input signal to apply the auto-encoder learning.

Thus, we obtain a multi-layered hierarchical network, recursively repeated auto-encoder learning, and stacked the encoding part of the network. This constructed multilayer network is called stacked auto-encoder. In this way, after building a multi-layer network, to add the identified network using the output of the final layer, a new supervised learning method is proposed. Stacked auto-encoder has been applied to the various subjects, as well as the DNN which stacks the RBM. Recently, the learning experiment of a feature extractor from a large amount of image has become famous.

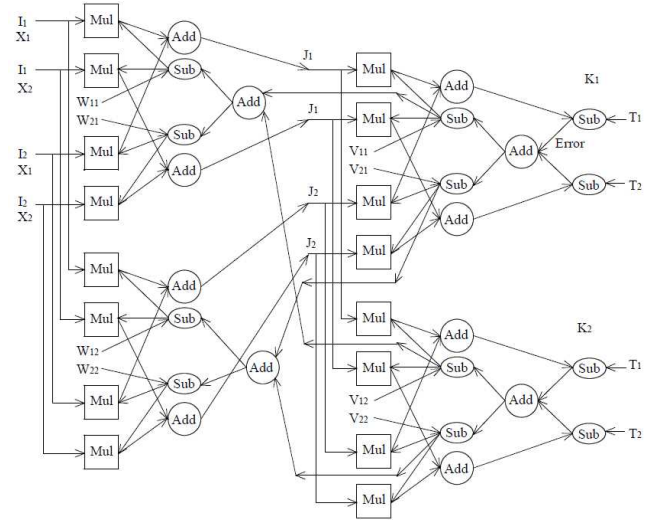


Fig. 14. The structure of 2-input, 1-output, 2-patterns and 3-layers analog neural network

In previous research, we described the dynamical neural network learning model. However, this model has only one input unit and one output unit. To realize the hardware deep learning model, we have to increase the number of units in each layer. We enhanced the neural network model as shown in Fig. 14. Fig. 12 indicates the structure of a 2-input, 2-output, 2-patterns and 3-layers analog neural network. There are two input lines,  $I_1$ . However,  $X_1$  and  $X_2$  are each a learning pattern. These are simplification figures, showing the one input signal and two kinds of learning patterns. This model suggests the possibility of the realization of the hardware implementation of the deep learning model.

## VI. CONCLUSION AND FUTURE WORK

### A. Conclusion

We proposed logarithmic four-quadrant multiple circuits as a connecting weight. This circuit is composed of a logarithmic circuit, additional circuit, exponential circuit, inverse circuit, comparator circuit, absolute circuit and an analog switch. This circuit operates more stably than previous models. And this circuit has a wide operating range.

Next, we constructed a three layer neural network, two-input layers, two-middle layers and one output layer. We confirmed the operation of the three layer analog neural network with the multiplying circuit by SPICE simulation. The connection weight can be changed by controlling the input voltage. This model has extremely high flexibility characteristics. When the analog



neural network is operated, the synapse weight is especially important. It is how to give the synapse weight to this neural network. To solve this problem, it is necessary to apply the method of the back propagation rule that is a general learning rule for the multiple electronic circuits. This neural circuit model is possible for learning. Another merit is the fast learning speed; this model refers to a biomedical neuron model. The proposed model is applicable to analog sensors with soft information processing. It is expected the application for biomedical sensor, robotics sensor, control mechanism etc.

Especially, a deep learning model has been developed very rapidly in the research area of image / sound recognition. Recently, multilayer neural network models, in particular, a deep learning model have been intensely researched. The performance has been extremely improved in the specialty of image / sound recognition. A high performance artificial intelligence model using the learning system using analog circuit is being awaited for in the near future. Moreover, the deep learning method has been proposed recently [15]. If this system improved toward the deep learning model, many applications will be realized. It is a kind of algorithms in the learning model. It attempts the high-level categorizing of data using multiple non-linear transformations and one method of machine learning. In the field of image recognition and speech recognition, the deep learning method has attracted the attention. We suggested the possibility of the realization of the hardware implementation of the deep learning model. It will improve the artificial intelligence element with self-dynamical learning. The realization of an integration device will enable the learning time to be reduced. The proposed model is robust with respect to fault tolerance. Future tasks include system construction and mounting a large-scale integration.

#### B. Future Scope using Deep Learning Model

The deep learning model is one kind of machine learning model. The performance of the recognition is improving more and more. This model is used for practical purposes in the field of image detection and video/sound recognition. This model will be developed in the field of advanced technology, self-driving, robotics and artificial intelligence. In the original BP learning neural network is a three-layer structure. However, the structure of the general deep learning model includes nine layers. And there are also three layered sub-networks, like a convolution network [15]. Furthermore, learning of the algorithm in the field of the deep learning model uses a stacked auto-encoder. This algorithm can detect the feature data and abstract expression data from the input image using large quantity learning data. The proposed AC operation circuits prompts the possibility for a flexible structure neural network like a deep learning model [16-17]. The model will develop the artificial intelligence unit under the environment of automated operation and be tough and beneficial for a fault tolerance network. Increasing the number of units, large-scale system development and creating integrated circuit are future problems [18-19].

#### REFERENCES

- [1] C. Mead, Analog VLSI and Neural Systems, Addison Wesley Publishing Company, Inc., 1989.
- [2] C. P.Chong, C. A. T. Salama, K. C. Smith, "Image-Motion Detection Using Analog VLSI," IEEE Journal of Solid-State Circuits vol.27, No.1, 1992, pp. 93-96.
- [3] Z. Lu, B. E. Shi, "Subpixel Resolution Binocular Visual Tracking Using Analog VLSI Vision Sensors," IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing, vol.47, No.12, 2000, pp. 1468-1475.
- [4] T. Saito and H. Inamura, "Analysis of a simple A/D converter with a trapping window," IEEE Int. Symp. Circuits Syst., 2003, pp. 1293-1305.
- [5] F. Luthon, D. Dragomirescu, "A Cellular Analog Network for MRF-Based Video Motion Detection," IEEE Transactions on Circuits and Systems-I: Fundamental Theory and Applications, vol.46, No.2, 1999, pp. 281-293.
- [6] H. Yamada, T. Miyashita, M. Ohtani, H. Yonezu, "An Analog MOS Circuit Inspired by an Inner Retina for Producing Signals of Moving Edges," Technical Report of IEICE, NC99-112, 2000, pp. 149-155.
- [7] T. Okuda, S. Doki, M. Ishida, "Realization of Back Propagation Learning for Pulsed Neural Networks Based on Delta-Sigma Modulation and Its Hardware Implementation," ICICE Transactions, J88-D-II-4, 2005, pp 778-788.
- [8] M. Kawaguchi, T. Jimbo, and M. Umeno, "Motion Detecting Artificial Retina Model by Two-Dimensional Multi-Layered Analog Electronic Circuits," IEICE Transactions, E86-A-2, 2003, pp. 387-395.
- [9] M. Kawaguchi, T. Jimbo, and M. Umeno, "Analog VLSI Layout Design of Advanced Image Processing For Artificial Vision Model," IEEE International Symposium on Industrial Electronics, ISIE2005 Proceeding, vol.3, 2005, pp. 1239-1244.
- [10] M. Kawaguchi, T. Jimbo, and M. Umeno, "Analog VLSI Layout Design and the Circuit Board Manufacturing of Advanced Image Processing for Artificial Vision Model," KES2008, Part II, LNAI, vol. 5178, 2008, pp. 895-902
- [11] M. Kawaguchi, T. Jimbo, and M. Umeno, "Dynamic Learning of Neural Network by Analog Electronic Circuits," Intelligent System Symposium, FAN2010, 2010, S3-4-3.
- [12] M. Kawaguchi, T. Jimbo, and N. Ishii, "Analog Learning Neural Network using Multiple and Sample Hold Circuits," IIAI/ACIS International Symposiums on Innovative E-Service and Information Systems, IEIS 2012, 2012, pp243-246.
- [13] Yoshua Bengio, Aaron C. Courville, Pascal Vincent: Representation Learning, "A Review and New Perspectives," IEEE Trans. Pattern Anal. Mach. Intell. 35(8), 2013, 1798-1828.
- [14] M. Kawaguchi, N. Ishii, and M. Umeno, "Analog neural circuit with switched capacitor and design of deep learning model," 3rd International Conference on Applied Computing and Information Technology and 2nd International Conference on Computational Science and Intelligence, ACIT-CSI, 2015, pp322-327
- [15] M. Kawaguchi, N. Ishii, and M. Umeno, "Analog Learning Neural Circuit with Switched Capacitor and the Design of Deep Learning Model," Computational Science/Intelligence and Applied Informatics, Studies in Computational Intelligence, 726, 2017, pp93-107.
- [16] M. Kawaguchi, N. Ishii, and M. Umeno, "Analog Neural Circuit by AC Operation and the Design of Deep Learning Model," DEStech Transactions on Computer Science and Engineering, 3rd International Conference on Artificial Intelligence and Industrial Engineering, 2017, pp228-233.
- [17] M. Kawaguchi, N. Ishii, and M. Umeno, "Analog Learning Neural Circuit with Switched Capacitor and the Design of Deep Learning Model," COMPUTATIONAL SCIENCE/INTELLIGENCE AND APPLIED INFORMATICS, 726, 2018, 93-107.
- [18] M. Kawaguchi, N. Ishii, and M. Umeno, "Learning Neural Circuit by AC Operation and Frequency Signal Output," Computer and Information Science, ICIS2019, best paper, 849, 2020, 15-30.
- [19] M. Kawaguchi, N. Ishii, and M. Umeno, "AC Operation Hardware Learning Neural Circuit Using V-F Converter System," Sensor Networks and Signal Processing, Springer, 176, 2020, 297-310.