

Further we note that $RJM(H)$ and $RRJM(H)$ might be investigated and used in the future in many fields of mathematics and engineering.

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A Tunable Gaussian/Square Function Computation Circuit for Analog Neural Networks

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Abstract—A Gaussian/square function computation circuit suitable for analog neural networks is proposed. It can realize Gaussian and square functions when operating in weak and strong inversion region, respectively. It is shown that the center, width, and peak amplitude of the dc transfer curve can be controlled separably. Measurement results on 3- μm CMOS fabricated chips confirm theoretical and simulation findings.

Index Terms—Gaussian circuit, similarity measure, squaring circuit.

I. INTRODUCTION

Similarity measure is an essential computation in many neural network models such as the Hamming-net classifier, associative memory, and self-organization feature map. Well-known measures include inner product, directional cosine, Manhattan distance, Euclidean distance, and bell-shape Gaussian-like function, etc. Among these, Euclidean distance similarity measure is most popular in neural network systems [1]–[3]. Analog multipliers in principle can be used for the square function in Euclidean distance similarity measure. A more efficient way is to design a circuit that performs the squaring function directly by exploiting the square-law behavior of MOS transistors [4]–[7]. N -dimensional Euclidean distance similarity measure can be computed by tying the outputs of N squaring circuits.

Gaussian function finds applications in several successful neural networks implementations, such as the activation function in radial basis function networks [8], [9] and the Gaussian ("bump")-type similarity measure [10]. For the realization of Gaussian function, one circuit using the concept of "current correlator" is developed for weak inversion operation [10]. However, in this circuit the width of dc transfer curve can not be adjusted. An improved version of this circuit consists of two parallelly connected differential pairs with different values of transconductance [11]. The effective transconductance of the whole circuit can be varied by properly distributing currents flowing into the two differential pairs. Consequently, one can tune the width of its dc transfer curve, albeit limitedly. One circuit [12] exhibits sufficient tuning range, but is too complex for VLSI implementations. Another tunable Gaussian function circuit working in strong inversion region contains several differential pairs [13]. Width tuning is achieved by selectively connecting input differential pairs to the bias current.

In most practical analog neural networks VLSI, flexible tuning of function parameters is a must due to the inherent learning/adaptive characteristics of neural networks. In this paper, we propose a Gaussian/square function computation circuit, in which the center, width, and peak amplitude of the dc transfer curve can be adjusted independently. In Section II, the dc characteristics of the proposed circuit working in weak and strong inversion regions are derived. Moreover, effect of transistor mismatch is also studied. In Section III,

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implementation and testing results are presented. Finally, conclusions are drawn in Section IV.

II. CIRCUIT DESCRIPTION

In the analysis, the following I - V relationship of MOS transistors are adopted. For strong inversion,

saturated region

$$I_{DS} = \frac{K}{2} (V_{GS} - V_t)^2 \quad (1)$$

linear region

$$I_{DS} = K \left[(V_{GS} - V_t)V_{DS} - \frac{1}{2}V_{DS}^2 \right] \quad (2)$$

where $K = \mu_o C_{OX}(W/L)$. For weak inversion [14]

$$I_{DS} = I_s e^{\kappa V_G/V_T} (e^{-V_S/V_T} - e^{-V_D/V_T}) \quad (3)$$

where I_s is proportional to W/L and κ —a constant between 0.7 and 1 is the back-gate coefficient describing the effectiveness of gate voltage change on channel surface potential.

Among all the Gaussian function circuits mentioned previously, the “bump” circuit using a “current correlator” is the most compact one [10] [see Fig. 1(a)]. The output current of the “bump” circuit operating in weak inversion is given by (assuming M1–M6 are matched and no channel-length modulation effect)

$$\frac{1}{2} I_b \operatorname{sech}^2 \left(\frac{\kappa V_{in}}{2V_T} \right). \quad (4)$$

However, SPICE simulations [Fig. 1(b)] show that the output curve is not symmetric, especially in strong inversion region. This is obviously caused by structural asymmetry in the “current correlator.” Recently, a symmetric Gaussian function circuit is proposed [see Fig. 1(c)] [15]. This circuit has symmetric I - V curves when working in strong inversion region as well as in weak inversion region [see Fig. 1(d)]. Similar circuit has also been applied to the design of the “soft differential pair” [16].

Assuming M1–M8 are matched, the output current of Fig. 1(c) can be expressed by (see [10] and Appendix for details)

weak inversion

$$\begin{aligned} I_o &= 2 \frac{I_L I_R}{I_L + I_R} \\ &= I_b \operatorname{sech}^2 \left(\frac{\kappa V_{in}}{2V_T} \right) \end{aligned} \quad (5)$$

strong inversion

$$\begin{aligned} I_o &\approx \sqrt{2I_L I_R} - \frac{\sqrt{2} - 1}{2} (I_L + I_R) \\ &= \frac{1}{2} \left(I_b - \frac{\sqrt{2}}{2} K V_{in}^2 \right). \end{aligned} \quad (6)$$

Equation (5) has been demonstrated to be a Gaussian-like function [10], and it is also evident that (6) describes a square function.

As to the tunability, the center and peak amplitude can be tuned by varying V_{in}^- and I_b , respectively; while the width can not be tuned, as implied by (5) and (6). Note that if $I_L + I_R (= I_b)$ is kept constant, the width can be tuned independently by changing the transconductance of the differential pair. To achieve this purpose, we propose a new Gaussian/square function computation circuit as depicted in Fig. 2. This circuit differs from Fig. 1(c) in that I_L and I_R are first folded to the outer branches and then fed to the “current correlator.” In this way, $I_L + I_R$ in Fig. 2 remains constant ($= I_x$) even when I_b is being varied for width adjustment. Note that in order to get zero output current for large input signal, I_b must be larger than I_x ($m \geq 1$) during the tuning process.

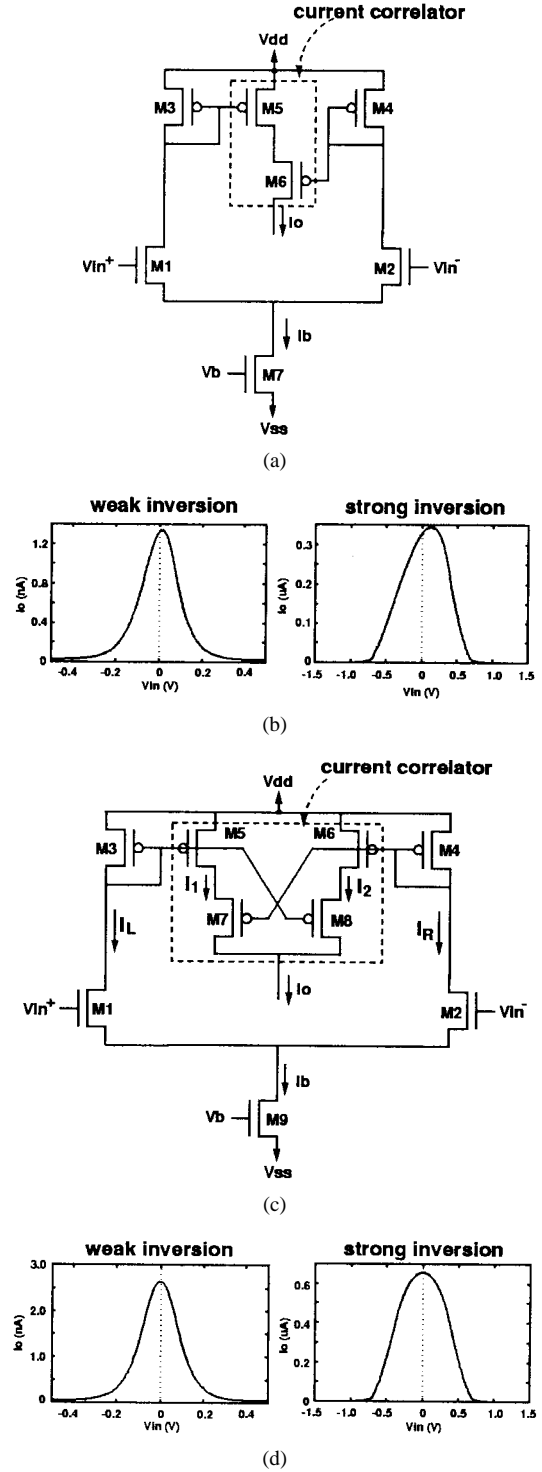


Fig. 1. (a) The “bump” circuit. (b) Simulation results of (a). (c) A symmetric version of (a). (d) Simulation results of (c).

A. Strong Inversion Operation

The output current of Fig. 2 can be expressed by

$$I_o \approx \sqrt{2I_L I_R} - \frac{\sqrt{2} - 1}{2} (I_L + I_R) \quad (7)$$

where in this circuit

$$I_L = I_1 - I_d \quad \text{and} \quad I_R = I_2 - I_d \quad (8)$$

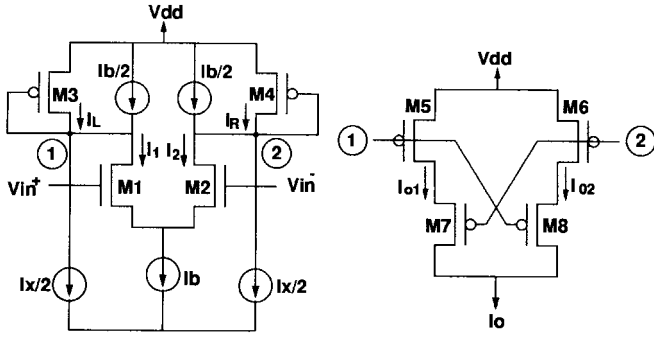


Fig. 2. The proposed similarity computation circuit.

with $I_d = (I_b - I_x)/2$. The relationship between I_1 , I_2 , and V_{in} is given by

$$V_{in} = V_{in}^+ - V_{in}^- = \sqrt{\frac{2I_1}{K}} - \sqrt{\frac{2I_2}{K}}. \quad (9)$$

After manipulating (7)–(9), we get

$$I_o \approx \left(1 - \sqrt{2}\right) \frac{I_x}{2} + \sqrt{\frac{I_b^2}{2} \left(1 - \frac{K}{2I_b} V_{in}^2\right)^2 - \frac{1}{2} (I_b^2 - I_x^2)}. \quad (10)$$

Using Taylor's expansion at $V_{in} = 0$, I_o can be expressed by

$$I_o = \frac{I_x}{2} \left[1 - \frac{\sqrt{2}}{2} m \cdot \frac{KV_{in}^2}{I_x} + \text{higher order terms} \right] \quad (11)$$

$$\approx \frac{I_x}{2} \left[1 - \left(\frac{V_{in}}{V_w} \right)^2 \right] \quad (12)$$

where $m = I_b/I_x$. Equation (11) is valid only for $I_o \geq 0$. The width (V_w) of the square function can be derived from (11) as $\sqrt{2I_x/(\sqrt{2}mK)}$ by omitting the higher order terms. The peak output current equals I_x and occurs when $V_{in} = 0$. Hence, the width can be tuned by $m(I_b)$ independently of the peak amplitude. Fig. 3(a) shows the relationship between width and I_b . Here, the width is determined by minimizing the maximum difference between the simulated curve from SPICE and an optimal square function. Fig. 4 shows the simulated dc transfer curves and the corresponding errors introduced by higher order terms in (11). The normalized errors are less than 4% in the operating range of interest.

B. Weak Inversion Operation

The I - V characteristic of a simple differential pair biased in weak inversion region can be described by [14]

$$I_1 = I_b \frac{1}{1 + e^{-\kappa V_{in}/V_T}}, \quad I_2 = I_b \frac{1}{1 + e^{\kappa V_{in}/V_T}}. \quad (13)$$

The output current can be derived as

$$\begin{aligned} I_o &= \frac{2I_L I_R}{I_L + I_R} \\ &= I_x \left[m^2 \operatorname{sech}^2 \left(\frac{\kappa V_{in}}{2V_T} \right) + 1 - m^2 \right] \\ &= I_x \left[1 - m^2 \tanh^2 \left(\frac{\kappa V_{in}}{2V_T} \right) \right] \end{aligned} \quad (14)$$

which is a Gaussian-like function and is valid only for $I_o \geq 0$. Again, peak output current occurs when $V_{in} = 0$ and equals I_x . So, σ can be tuned by $m(I_b)$ independently of the peak amplitude as in strong inversion region. The dependency of σ on I_b is illustrated in Fig. 3(b).

In both regions, the circuit achieves a wide peak amplitude range by controlling I_x . The tuning range of width (σ) is determined

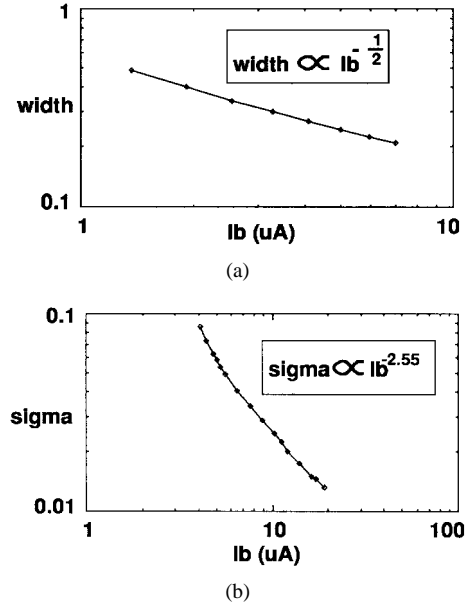
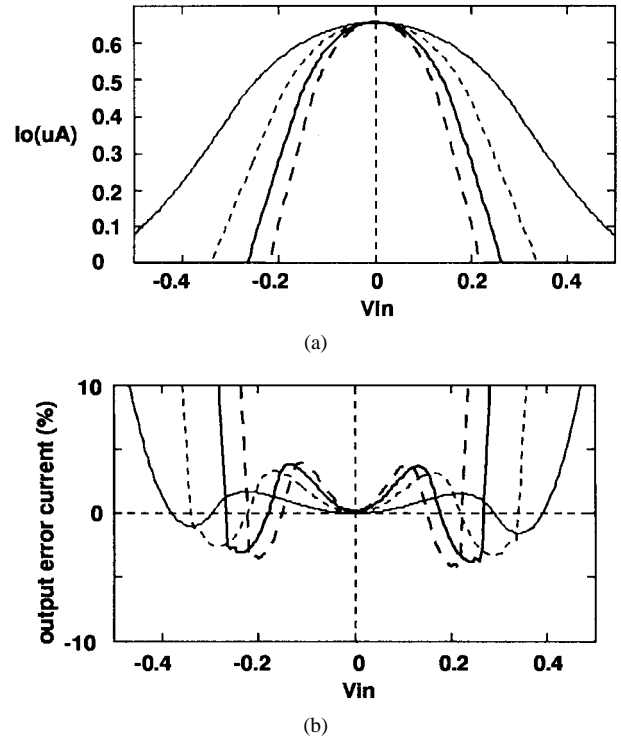
Fig. 3. The dependency of width (σ) on I_b : (a) strong inversion region and (b) weak inversion region.

Fig. 4. The characteristic of the square circuit: (a) dc transfer curves for various width (from SPICE simulations) and (b) the corresponding errors.

by the available maximum and minimum transconductance of the input differential pair, which in turn depends on I_b . The minimum transconductance allowed can be found by setting I_b to I_x because $I_b \geq I_x$. Note that $I_b/2$ at the top of Fig. 2 is produced by mirroring half of the current sink I_b . Therefore, if the transistor (M_b) corresponding to the current source enters linear region, the mirroring scheme fails, which sets the upper limit of the transconductance (lower limit of width). Once M_b enters linear region, the tuning of width and peak amplitude become dependent. As indicated in Fig. 3, the circuit has better width(σ)-tuning efficiency when operating in weak inversion region than in strong inversion region.

To estimate the effect of device mismatch, some Monte Carlo analysis are conducted. In the analysis, the channel length of all transistors in Fig. 2 are randomly varied according to a Gaussian distribution with 3σ equal to 3% of the nominal value. For weak inversion operation, 50 simulation trials show that 3σ offset voltage is 6.60 mV, and 3σ peak output current error is 0.22 nA for 2.60-nA nominal current. Further simulations reveal that a quarter of the aforementioned voltage and current error can be attributed to the “current correlator.” For strong inversion operation, the resulting 3σ offset voltage is 23.01 mV, and 3σ peak output current error is 47.70 nA for 649.20-nA nominal current. Also, a quarter of error can be attributed to the “current correlator.”

Simulations show that asymmetry is mainly caused by bias current mismatch between M3 and M4. Assume that $I_L = I_1 - (I_d - \Delta I/2)$ and $I_R = I_2 - (I_d + \Delta I/2)$. For weak inversion operation, the output current can be rewritten as

$$\begin{aligned} I_o + \Delta I_o &= 2 \frac{\left(I_1 - I_d - \frac{\Delta I}{2}\right) \left(I_2 - I_d + \frac{\Delta I}{2}\right)}{I_x} \\ \Rightarrow \frac{\Delta I_o}{\Delta I} &= \frac{I_1 - I_2}{I_x} \\ &= \frac{I_b}{I_x} f(V_{in}) \end{aligned} \quad (15)$$

where $f(V_{in}) = \tanh(\kappa V_{in}/2V_T)$. The ratio of input referred error voltage to ΔI can be expressed by

$$\begin{aligned} \frac{\Delta V_{in}}{\Delta I} &= \frac{\Delta I_o}{\Delta I} \cdot \frac{\partial V_{in}}{\partial I_o} \\ &= -\frac{V_T}{\kappa I_b} \cdot \cosh^2\left(\frac{\kappa V_{in}}{2V_T}\right). \end{aligned} \quad (16)$$

For strong inversion operation,

$$\begin{aligned} I_o + \Delta I_o &= \sqrt{2 \left(I_1 - I_d - \frac{\Delta I}{2}\right) \left(I_2 - I_d + \frac{\Delta I}{2}\right)} - \frac{\sqrt{2}-1}{2} I_x \\ \Rightarrow \frac{\Delta I_o}{\Delta I} &= \frac{\sqrt{2} I_b}{4\sqrt{I_L I_R}} \cdot g(V_{in}) \end{aligned} \quad (17)$$

where

$$g(V_{in}) = \sqrt{\left(\frac{K}{I_b}\right) - \left(\frac{K V_{in}}{2 I_b}\right)^2} \cdot V_{in}.$$

The ratio of input referred error voltage to ΔI can be expressed by

$$\begin{aligned} \frac{\Delta V_{in}}{\Delta I} &= \frac{\Delta I_o}{\Delta I} \cdot \frac{\partial V_{in}}{\partial I_o} \\ &= -\frac{1}{K} \sqrt{\frac{4K}{I_b} \cdot \frac{1 - K \frac{1}{4I_b} V_{in}^2}{1 - K \frac{I_b}{I_x^2} V_{in}^2}}. \end{aligned} \quad (18)$$

Unmatched input differential pair leads to some offset voltage. Mismatch between the four transistors of the “current correlator” and mismatch between M3 and M4 have minor effect on symmetry.

MOS transistor characteristics are strongly temperature-dependent, especially in weak inversion [17]. Here only the temperature effects in weak inversion are discussed. The I - V characteristics of MOS transistor in weak inversion are similar to bipolar transistors, therefore some known circuit techniques used in bipolar circuits can be adopted to reduce temperature dependence of the proposed circuit.

In order to reduce the temperature dependency of peak amplitude and width (σ) of the output current, [see (14)], $I_x/2$ and the transconductance of M1/M2 must be kept constant over the specified temperature range. Current source $I_x/2$ can be implemented using a

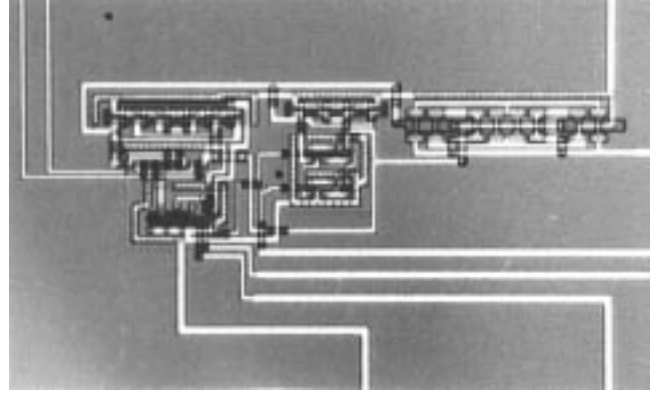


Fig. 5. Microphotograph of the circuit in Fig. 2.

PTAT source and a source with negative temperature coefficient [18]. Another method to achieve stable bias current is current regulation [19]. The transconductance of M1/M2 can be kept constant by making I_b a PTAT current source because the transconductance is proportional to $I_b/(kT/q)$.

III. MEASUREMENTS

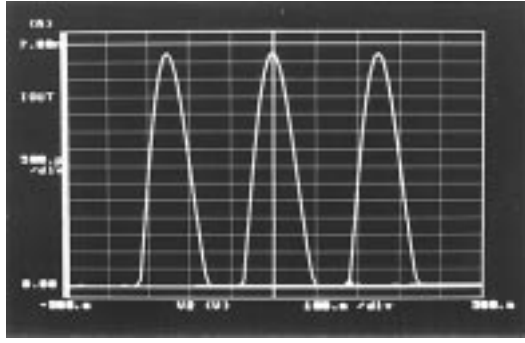
The circuit in Fig. 2 was fabricated using 3- μm DPSM CMOS technology. The microphotograph of the circuit is shown in Fig. 5. A conservative minimal channel length of 15 μm is chosen for reduced channel length modulation effect and larger linear range of the differential pair. The circuit size is $560 \times 180 \mu\text{m}^2$. During the experiment, ± 2.5 -V power supply is used. Figs. 6(a)–(c) and 7(a)–(c) show the circuit behaviors in weak and strong inversion regions, respectively. It is clear that the center, width, and peak amplitude can be controlled independently. From Fig. 6(b), we see that the measured input offset voltage is around 3–4 mV, within the 3σ limit predicted by simulation. Note that (16) and (18) are even functions of V_{in} , therefore the output curves are skewed as shown in Figs. 6(b) and 7(b). Because $\Delta V_{in}/\Delta I$ is inversely proportional to I_b and directly proportional to V_{in} , the skew in the outermost curves are more significant than those in the inner curves as shown in Fig. 7(b). Similar phenomenon can also be found when the circuit operates in strong inversion region [see Fig. 6(b)].

IV. CONCLUSION

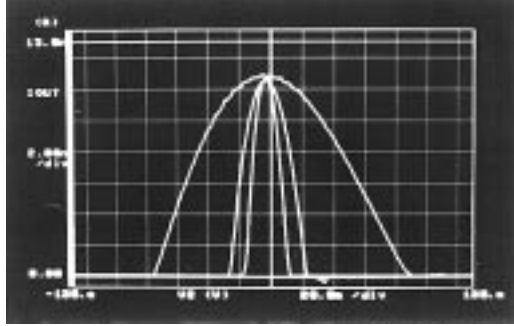
Based on the “current correlator” [10], a new Gaussian/square computation circuit for analog neural networks is proposed. Apart from analysis of the weak inversion behavior, the circuit is characterized by detailed formulation and measurements in strong inversion region. This circuit exhibits independent programmability in center, width, and peak amplitude. Thanks to this property, in most cases, the input offset voltage and deviated peak amplitude introduced by channel length modulation and device mismatch can be removed during the training process. Furthermore, this circuit is versatile in the sense that when operating in the strong inversion region, it calculates squared difference, whereas in the weak inversion region, it realizes Gaussian-like function. Therefore, it can find applications in various neural network systems.

APPENDIX

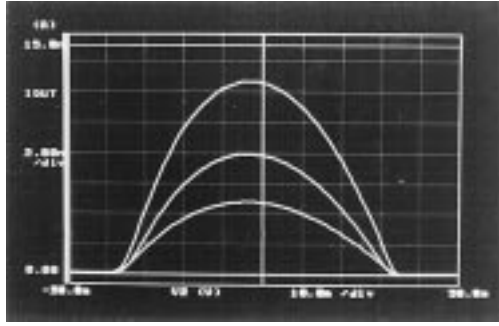
The behavior of the circuit in Fig. 2 in strong inversion region is formulated as follows: Assuming that the aspect ratios of M1–M8 are matched, and transistors M5/M6 and M7/M8 operate in linear and strong inversion, respectively. The current through M5 and M7



(a)



(b)



(c)

Fig. 6. Programmability of the circuit in Fig. 2 in weak inversion region: (a) center, (b) width, and (c) peak amplitude.

is given by

$$I_{o1} = \frac{K}{2} (V_3 - V_2 - |V_{tp}|)^2$$

$$= K[(V_{dd} - V_1 - |V_{tp}|)(V_{dd} - V_3) - \frac{1}{2} (V_{dd} - V_3)^2]. \quad (A1)$$

Substituting $V_1 = V_c + V_{id}/2$ and $V_2 = V_c - V_{id}/2$ into (A1) yields

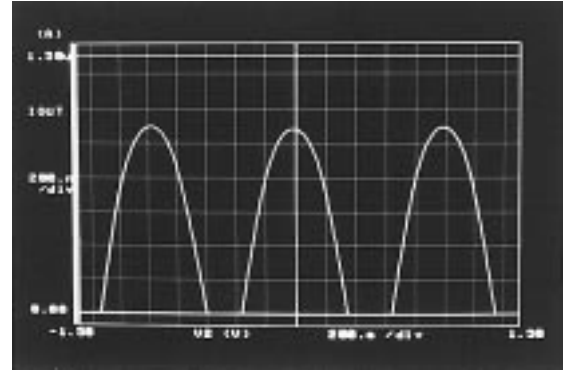
$$I_{o1} = \frac{K}{2} \left(V_3 - V_c - |V_{tp}| + \frac{V_{id}}{2} \right)^2$$

$$= K \left[\left(V_{dd} - V_c - |V_{tp}| - \frac{V_{id}}{2} \right) (V_{dd} - V_3) - \frac{1}{2} (V_{dd} - V_3)^2 \right]. \quad (A2)$$

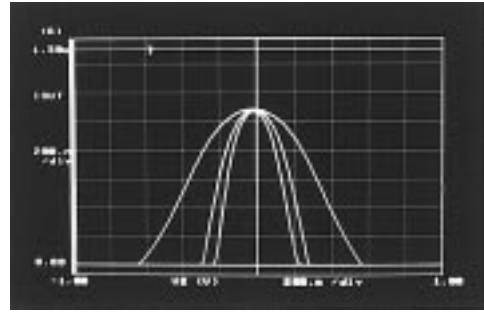
Let $\bar{V}_c = V_{dd} - V_c - |V_{tp}|$ and $\bar{V}_3 = V_{dd} - V_3$. Equation (A2) is then reduced to

$$I_{o1} = \frac{K}{2} \left(\bar{V}_c + \frac{V_{id}}{2} - \bar{V}_3 \right)^2$$

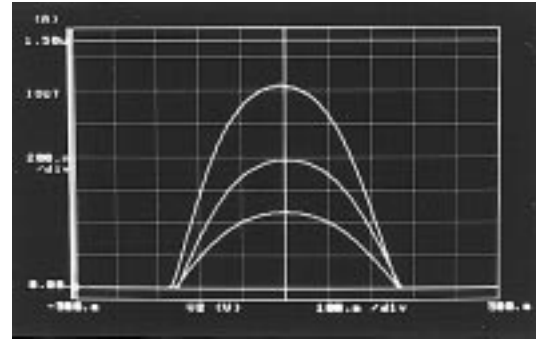
$$= K \left[\left(\bar{V}_c - \frac{V_{id}}{2} \right) \bar{V}_3 - \frac{1}{2} \bar{V}_3^2 \right]. \quad (A3)$$



(a)



(b)



(c)

Fig. 7. Programmability of the circuit in Fig. 2 in strong inversion region: (a) center, (b) width, and (c) peak amplitude.

Solving for \bar{V}_3 , we obtain

$$\bar{V}_3 = \bar{V}_c - \frac{\sqrt{2}}{2} \left[\bar{V}_c^2 - V_{id} \bar{V}_c - \left(\frac{V_{id}^2}{2} \right) \right]^{1/2}.$$

When this result is substituted into (A3), we obtain, after somewhat lengthy manipulations,

$$I_{o1} = \frac{K}{4} \left\{ \bar{V}_c^2 - \bar{V}_c V_{id} + \left(\frac{V_{id}^2}{2} \right) \right. \\ \left. + \sqrt{2} V_{id} \bar{V}_c \left[1 - \frac{V_{id}}{\bar{V}_c} - \left(\frac{V_{id}}{2\bar{V}_c} \right)^2 \right]^{1/2} \right\}. \quad (A4)$$

Similarly,

$$I_{o2} = \frac{K}{4} \left\{ \bar{V}_c^2 + \bar{V}_c V_{id} + \left(\frac{V_{id}^2}{2} \right) \right. \\ \left. + \sqrt{2} V_{id} \bar{V}_c \left[1 + \frac{V_{id}}{\bar{V}_c} - \left(\frac{V_{id}}{2\bar{V}_c} \right)^2 \right]^{1/2} \right\}. \quad (A5)$$

Adding (A4) and (A5), and using Taylor's expansion, we have

$$I_o = I_{o1} + I_{o2} \\ = \frac{K}{2} \left\{ \bar{V}_c^2 + \frac{V_{id}^2}{2} - \sqrt{2} V_{id} \bar{V}_c \left[\frac{V_{id}}{\bar{V}_c} + \frac{3}{8} \left(\frac{V_{id}}{\bar{V}_c} \right)^3 + \dots \right] \right\}$$

where all terms containing even powers of V_{id}/\bar{V}_c have been cancelled. Assume that $V_{id} \ll \bar{V}_c (= V_{dd} - V_c - |V_{tp}|)$, we retain the first term of the above equation, then

$$I_o \approx \frac{K}{2} \left[\bar{V}_c^2 + (1 - 2\sqrt{2}) \left(\frac{V_{id}}{2} \right)^2 \right]$$

or

$$I_o \approx \frac{K}{4} [(V_{dd} - |V_{tp}| - V_1)^2 \\ + (V_{dd} - |V_{tp}| - V_2)^2 - \sqrt{2}(V_1 - V_2)^2]. \quad (A6)$$

Equation (A6) is the relationship between the output current and the node voltage (V_1 and V_2). Since M3 and M4 are diode-connected transistors, and operate in the saturated region. Thus, the drain currents of M3 and M4 are given by

$$I_L = \frac{K}{2} (V_{dd} - |V_{tp}| - V_1)^2, \quad I_R = \frac{K}{2} (V_{dd} - |V_{tp}| - V_2)^2 \\ \Rightarrow V_{dd} - |V_{tp}| - V_1 = \sqrt{\frac{2I_L}{K}}, \quad V_{dd} - |V_{tp}| - V_2 = \sqrt{\frac{2I_R}{K}}. \quad (A7)$$

When the differential is biased in saturated region, its I - V relationship is well known as

$$V_{in} = V_{in}^+ - V_{in}^- = \sqrt{\frac{2I_L}{K}} - \sqrt{\frac{2I_R}{K}} \quad (A8)$$

and

$$I_b = I_L + I_R. \quad (A9)$$

Substituting (A9) into (A8) and solving for I_L and I_R , we get

$$I_L = \frac{I_b}{2} + \frac{I_b}{2} \left(\frac{KV_{in}^2}{I_b} - \frac{K^2 V_{in}^4}{4I_b^2} \right) \quad (A10)$$

$$I_R = \frac{I_b}{2} - \frac{I_b}{2} \left(\frac{KV_{in}^2}{I_b} - \frac{K^2 V_{in}^4}{4I_b^2} \right). \quad (A11)$$

Substituting (A7), (A10), and (A11) into (A6), we have

$$I_o = \sqrt{2I_L I_R} - \frac{\sqrt{2}-1}{2} (I_L + I_R) = \frac{1}{2} I_b - \frac{\sqrt{2}}{4} K V_{in}^2. \quad (A12)$$

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Comments on "A High Speed Realization of a Residue to Binary Number System Converter"

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In the above paper [1], a new residue to binary converter design based on the theory presented in [2] which uses 4 operand modular adder to compute the value of X^* is described. An improvement in which computational simplification of X^* and its realization using 3 operand modular adder is presented.

X^* is given by

$$X^* = |A + B + C - X_1|_{2^{2n-1}} \quad (1)$$

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