2
Sampling pulse generator circuits

2.1 Pulse width and rise time

The problems considered in this chapter concern devices and circuits which can produce very short pulses. The sampling pulse generators, found in the most advanced sampling and digitising oscilloscopes, may produce pulses as short as 50 ps. The first point to consider, however, is the shape of the pulse itself. This might seem to be a very trivial matter, but it does hold the key to good pulse generator circuit design.

Fig. 2.1 illustrates what is meant. Every real pulse has finite rise and fall times, τ_r and τ_f in Fig. 2.1, as well as a pulse width, τ. The rise and fall times are traditionally taken between the times at which the level is at 10 % and 90 % of the pulse amplitude, A. For the sampling pulse generator, the pulse width, τ, is best taken as shown in Fig. 2.1: the time that the pulse lies above 90 % of its maximum amplitude.

What is important here is that a well-designed pulse generator circuit will always have some clearly identifiable part that defines the pulse width. For example, this could be a length of transmission line or a *CR* time constant. Whatever defines the pulse width, it must have negligible effect upon the rise and fall times, and these both need to be made as short as possible. In the case of a sampling pulse generator, where a very small pulse width is of primary concern, it is vital to obtain very short rise and fall times.

2.2 Circuit shape

In chapter 1, great emphasis was put upon the concept of circuit shape: the form that a circuit diagram has as a preliminary design sketch, the first idea the designer has, the circuit as it is before any calculations of circuit values can be made.

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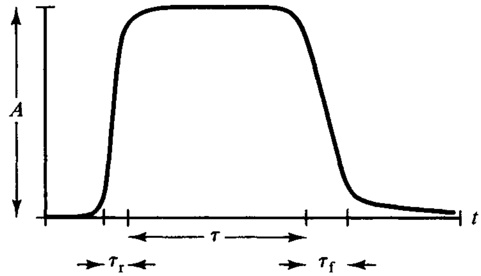

Fig. 2.1. *Defining the rise time, fall time, and width of a pulse.*

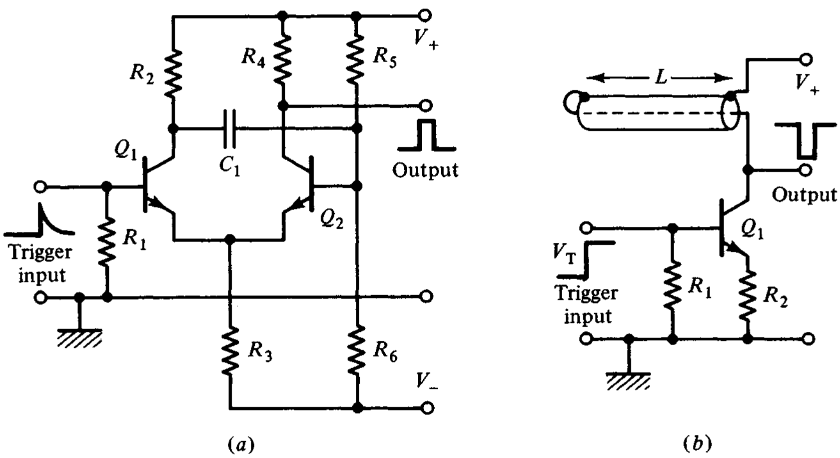

Fig. 2.2. *Two contrasting pulse generator circuit shapes.*

Fig. 2.2 shows two pulse generator circuit shapes to illustrate this point of view. In Fig. 2.2(*a*), the well-known monostable multivibrator [1] is shown. This is a very old circuit idea, and may have been first described by White [2]. In the form shown here, transistor Q_2 is normally held on, this being arranged by the choice of the bias resistors R_5 and R_6. This means that Q_1 is held off because of the emitter coupling between Q_1 and Q_2. A short trigger input pulse drives Q_1 on and Q_2 off. Q_2 remains off while C_1 charges up, and the time constant that determines how long Q_2 stays off, assuming that the devices do not saturate, is

$$T = C_1[R_2 + R_5 R_6/(R_5 + R_6)]. \tag{2.1}$$

Unfortunately, this time constant must also determine how rapidly the emitter junction of Q_2 begins to turn on again at the end of the pulse, and this means that the fall time of the output pulse must depend to a certain extent upon the pulse length. This contradicts the expectations of the final paragraph of section 2.1: whatever decides pulse width should not effect rise or fall times.

Fig. 2.2(*b*) shows another possible circuit shape for a pulse generator. This is also a very old circuit idea, patented by Blumlein in 1940 [3]. The circuit shown here involves only a single transistor and a length of transmission line which has a good short circuit made at its far end. The transistor is normally off until an input step, V_T, turns Q_1 on so that it takes a current $I_C = (V_T - V_{BE})/R_2$. The transistor does not saturate.

The voltage level at the collector of Q_1 will drop by an amount $I_C Z_o$, where Z_o is the characteristic impedance of the transmission line. If this is a good quality low loss line, Z_o will be almost a pure resistance and the initial edge of the output pulse, which is negative going in this circuit, is determined mainly by the transistor turn-on time. The same applies to the trailing edge of the pulse because, again if the transmission line is good, this edge is simply the reflection of the initial edge, reflected and inverted by the short circuit. The pulse length in this circuit is very accurately defined as $\tau = 2L/v_p$, where v_p is the propagation velocity of the line: typically 60% of the velocity of light.

It follows that the circuit shape shown in Fig. 2.2(*b*) might be a good choice for generating the very short pulses that are needed for sampling circuits. As the pulse length is determined by a length, L in Fig. 2.2(*b*), and light travels 30 cm in 1 ns, the lengths involved for the generation of pulses considerably less than 1 ns in duration are conveniently small.

The problem which is obviously outstanding in the circuit shown in Fig. 2.2(*b*) is the switching device. No bipolar transistor can be expected to turn on in a time which is very much smaller than 100 ps. It is necessary to find some other kind of switching device.

2.3 The step recovery diode

The switching device that is almost universally used in sampling pulse generator circuits is the step recovery diode. This was originally called the charge storage diode, in an important paper dealing with the theory of this new device [4]. The terms snap-off diode and snap-back diode are also used.

The step recovery diode represents a rather unexpected change in the direction of fast switching device development. Earlier work had concentrated upon two main lines, both using three terminal active

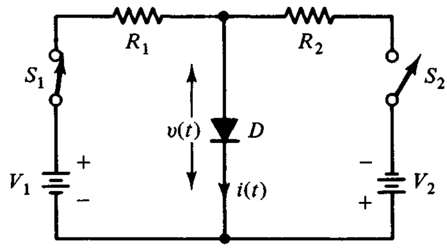

Fig. 2.3. *An experimental set-up for the study of reverse recovery in a diode.*

devices. These two main lines are conveniently illustrated using Figs. 2.2(*a*) and 2.2(*b*) again.

One line of development attempted to produce very fast switching by using amplifying devices, of very large gain–bandwidth product, in regenerative switching circuits of the kind shown in Fig. 2.2(*a*). Such circuits can provide very fast turn-on, much faster than the rise time of the input pulse that triggers this turn-on. However, the limitation is in the bandwidth of the circuit, and it is very difficult to generate well-shaped pulses, in the sense of Fig. 2.1, which are much shorter than 1 ns with circuits using the regenerative idea.

A second line of development involved circuits of the shape shown in Fig. 2.2(*b*), but using some kind of three terminal triggerable device instead of the simple amplifying device shown here. Such devices as thyratrons, triggered spark gaps, mercury wetted relays, avalanche transistors, four layer solid state devices, and an interesting cold cathode gas filled device known as a krytron, can all be found in the extensive literature on this topic. These triggerable devices do have very high speed possibilities, but they all suffer from jitter: there is a considerable statistical fluctuation in the time between the arrival of the trigger input pulse and the actual turn-on of the device.

The step recovery diode is a radical break in the tradition of fast switching. In the first place, it is a *two* terminal device. Secondly, its fast properties are associated with the way in which it turns *off*.

2.4 Step recovery diode theory

A step recovery diode is usually a silicon diode which has been made in such a way that it shows two special features in the reverse recovery mode: long minority carrier storage time followed by very short turn-off time. Fig. 2.3 shows a simple experimental set-up for the study of reverse recovery which will make clear what is meant here.

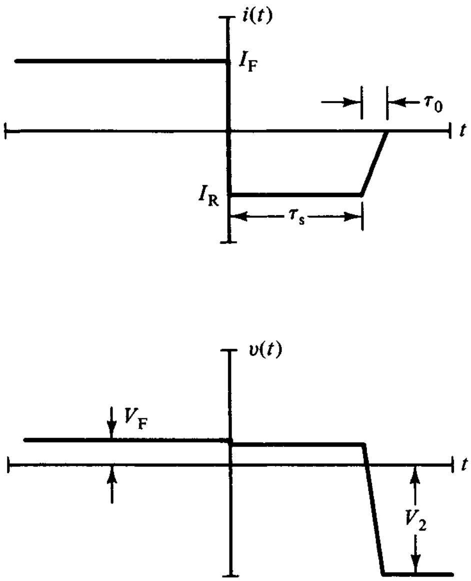

Fig. 2.4. *The waveforms that would be observed from the circuit shown in Fig.* 2.3.

In Fig. 2.3, a silicon diode, D, is shown connected to two voltage sources, V_1 and V_2, via current limiting resistors R_1 and R_2, and with switches, S_1 and S_2, to control the experiment. This is, of course, a thought experiment at this stage. An experimental circuit will be given towards the end of this chapter so that the reader can make real measurements.

As Fig. 2.4 shows, for $t < 0$, when S_1 is closed and S_2 is open, the diode takes a forward current I_F and has a forward voltage V_F across it. In the case of silicon, V_F is close to 0.7 V for a very wide range of current.

At $t = 0$, S_1 is opened and S_2 is closed. This causes a reverse current to flow through the diode, and Fig. 2.4 shows that the values of V_2 and R_2, in Fig. 2.3, have been chosen, in this thought experiment, so that $I_R = I_F$.

The reversal of current through the diode has very little effect upon the voltage across it: this is still close to 0.7 V. The reason for this is that a silicon pn junction stores charge when it is put into forward conduction, and it is not possible to change the voltage across the junction until there is a considerable change in the minority carrier density close to the junction region [5, 6, 7]. The small drop in forward voltage, shown in Fig. 2.4, is due to the reversal of the ohmic drop across the bulk of the diode structure.

It follows that quite a large reverse current can flow for a storage time, τ_s, as shown in Fig. 2.4, and then the diode does really turn off. The

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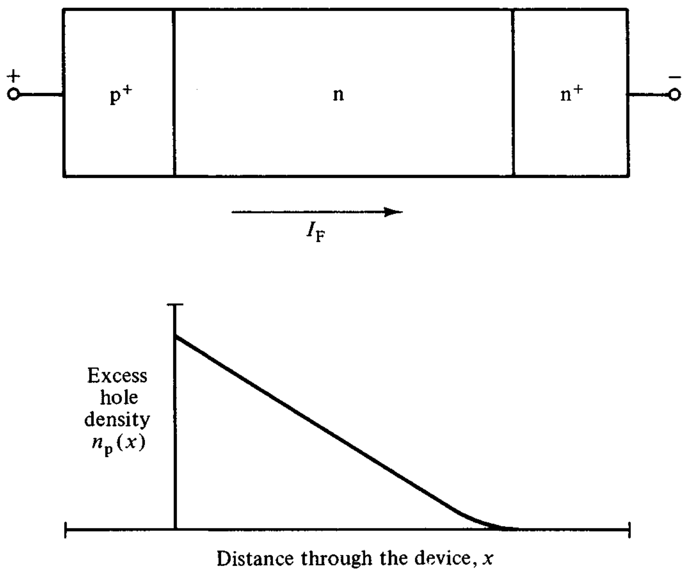

Fig. 2.5. *A diode with a* p^+nn^+ *structure in forward conduction and the resulting minority carrier density across the n region.*

current falls to zero and the voltage across the diode becomes V_2, in the reverse direction, and all this happens in turn-off time τ_0. The actual values of τ_s and τ_0 are determined by doping levels and geometry, and these are considered next.

In an ordinary, small signal, silicon diode, like the classical 1N914 device, every attempt is made by the device designer to reduce the total reverse recovery time, $\tau_s + \tau_0$ in Fig. 2.4. Designers of step recovery diodes aim for quite different behaviour. It will be seen in section 2.7 that circuit design requirements call for a storage time of a few nanoseconds, for a step recovery diode that is to be useful in a sampling pulse generator circuit. The turn-off time, τ_0, in contrast, must be made as short as possible. This can be achieved by using a diode geometry of the kind shown in Fig. 2.5: a p^+nn^+ structure.

In Fig. 2.5, the p^+nn^+ diode is shown passing a forward current, I_F. The p^+ and n^+ regions are very heavily doped, while the n region is very lightly doped and is thin compared to a diffusion length. It follows that the minority carrier density in the n^+ and p^+ regions can be ignored in order to obtain a qualitative picture of what is happening. What is important is the density of holes in the n region, and this is shown in Fig. 2.5. At the p^+n junction, which is abrupt, there is a high density of holes injected from the p^+ region. The density of minority carriers falls almost linearly across the thin n region, to become very small at the nn^+ junction. This happens because of the two boundary conditions at the nn^+ junction: (1) continuity of the slope of $n_p(x)$, and (2) $n_p(x) \approx 0$. The first condition gives continuity to the hole current density,

$$J_p = -eD_p \, dn_p(x)/dx \tag{2.2}$$

where e is the electronic charge and D_p is the diffusion constant for holes. The second condition comes from the fact that the diffusion length for holes,

$$L_p = (D_p T_p)^{\frac{1}{2}} \tag{2.3}$$

will be very small in the heavily doped n^+ region where the hole lifetime, T_p, is small and $n_p(x)$ must vanish rapidly as x continues to increase. D_p depends only slightly upon doping level.

It follows that the forward current in this diode is mainly carried by majority carriers in the p^+ and n^+ regions, but in the n region the forward current is a diffusion current of minority carriers, holes, and this diffusion current is down the gradient shown in Fig. 2.5. When the current through the diode is reversed, using the thought experiment shown in Fig. 2.3, it is not possible for the excess hole density distribution, shown in Fig. 2.5, to change very rapidly.

What will happen is shown in Fig. 2.6. Just after the reversal of the current, the excess hole density must drop within the part of the n region which lies close to the p^+n junction. This reverses the slope of $n_p(x)$ and causes a diffusion current in the direction of I_R. Note that a diffusion current must still flow in the old direction, the direction of I_F, over the remaining part of the n region, where the slope of $n_p(x)$ remains, for the moment, unchanged. The new diffusion current, near the p^+n junction, is greater, however.

Fig. 2.6 shows the continuation of the process as $n_p(x)$ reverses slope over more and more of the n region, the maximum value of $n_p(x)$ moving away from the p^+n junction and the amplitude of $n_p(x)$ falling as time passes. The key to the very fast turn off in the step recovery diode can be seen in the last curve: the one for $t = \tau_s$. This shows that nearly all the excess minority carrier charge has vanished at the same instant that $n_p = 0$ at the p^+n junction. It is only when $n_p = 0$, at the p^+n junction, that the reverse voltage across the junction can develop. If there are still some minority carriers left within the n region, these will flow across the p^+n junction and slow up this establishment of reverse voltage.

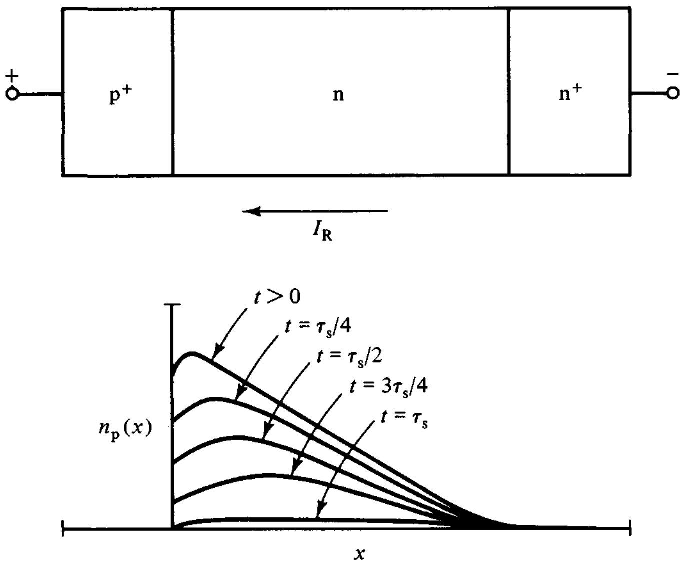

Fig. 2.6. The excess hole density as a function of space and time during the flow of reverse current, I_R, in the p^+nn^+ diode. Note that the voltage across the diode is still in the forward direction.

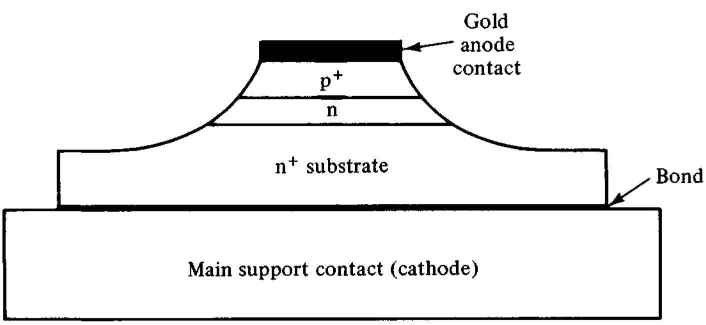

Fig. 2.7. The mesa structure which is used for the step recovery diode.

2.5 Step recovery diode design

A real step recovery diode, in contrast to the academic representation shown in Figs 2.5 and 2.6, will take the form shown in Fig. 2.7 [8]. This is the so-called 'mesa' structure, a Spanish word which first came into the English language as a technical term in physical geography to describe a high table land which is a remnant of a former plateau. On a microscopic scale, this is exactly what the mesa diode, shown in Fig. 2.7, is.

The first step in the fabrication process is to diffuse a structure, of the kind shown in Fig. 2.8, into an n^+ substrate. A gold contact is then

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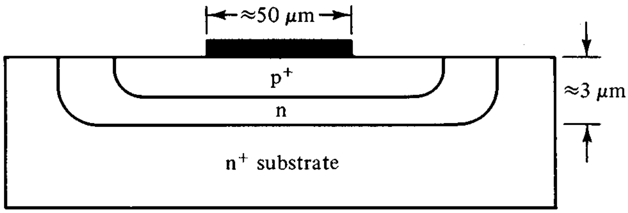

Fig. 2.8. The step recovery diode structure before plasma etching. Note the different scales horizontally and vertically. Also the thickness of the n^+ substrate, as in Fig. 2.7, has been considerably reduced for this diagram.

evaporated onto the centre of the p^+ region. By means of plasma etching, all the silicon which is not covered by the gold top contact is then removed, down to the n^+ substrate, leaving the structure shown in Fig. 2.7 behind.

The p^+nn^+ structure, which has been brought out in the discussion here, is the most common, but an n^+pp^+ step recovery diode may have advantages in speed [9]. The reason for using the mesa structure is that this gives a device which can be put into a package having negligible self capacitance. A step recovery diode is usually found in a minute ceramic package suitable for surface mounting on a ceramic substrate as part of a thick film circuit.

2.6 Using the step recovery diode

The step recovery diode can be used in a pulse generator circuit that is a development of the circuit shape shown in Fig. 2.2(*b*).

In Fig. 2.2(*b*), a transistor is shown in series with a length of transmission line, which is short circuited at the far end. The transistor switches on a current I_C and a voltage pulse, amplitude $I_C Z_o$, is generated across the transmission line.

The step recovery diode can only switch a current *off*. This means that, to produce a pulse, the device must be put in *parallel* with a length of transmission line and also in parallel with a constant current source, I. When the diode turns off, the current I will be switched into the line.

Now this is all very well, but it is obvious that this new parallel circuit cannot use a simple short circuit at the far end of the line. What is needed in this case is a large capacitor, in series with the input to the short circuited line, which will allow the d.c. level across the diode, V_F in Fig. 2.4, to become established, and yet present a negligible impedance to all the high frequency components of the very short pulse.

This is the shape of the experimental circuit which is described in the next section.

2.7 An experimental circuit

It was stated, at the beginning of this chapter, that a sampling pulse generator would be designed to produce a very short pulse, even as short as 50 ps. Circuits which work at such high speeds are usually constructed as hybrid circuits, using very small surface mounted components on a ceramic substrate with thick film printed interconnections.

The majority of readers may not have the facilities to make hybrid electronic circuits, using real step recovery diodes, or the very high speed test equipment which is needed to examine the dynamic behaviour of real step recovery diode circuits. For these reasons, an experimental circuit is described in this section, which is identical, as a circuit shape, to a real step recovery diode sampling pulse generator circuit, but which works at a much slower speed and can, therefore, be made up using quite conventional techniques.

Becker and Fomm [10] pointed out some years ago that many diodes which are designed as tuning diodes, varactor diodes, or what are often termed 'varicap diodes', can be used as step recovery diodes working at nanosecond switching speeds. This is to be expected because the tuning diode has the same p^+nn^+ or n^+pp^+ structure of the step recovery diode, but it is normally used under conditions of reverse bias and the reason for the very lightly doped n or p layer, in the tuning diode, is to obtain a wide variation in the capacitance of the reverse biassed p^+n, or n^+p, junction.

Tuning diodes are very easily available, in quite conventional types of package, and at low cost. This is because these diodes are widely used in television and FM tuners.

Fig. 2.9 shows the experimental circuit. Transistor Q_1 is normally off, and the step recovery diode, D_2, is in forward conduction because Q_2 is connected as a simple constant current sink. R_3, R_4 and R_6 are chosen to make this forward current in D_2 a few tens of milliamperes when V_- is at -15 V, but the actual value can be varied by using a variable negative supply. Q_2 is a simple general purpose transistor.

Q_1 is also a general purpose transistor, able to turn on a current of about 200 mA, maximum, when a negative going pulse, 5 V in amplitude, arrives at the input socket. R_1 and R_2 are chosen to give a 50 Ω termination to the input cable, C_1 being large, and the diode D_1 clamps the pulse input, from the point of view of Q_1, to the positive rail. (The idea of diode clamping is explained in all the elementary electronics texts [11], and will turn up repeatedly in the experimental circuits described in

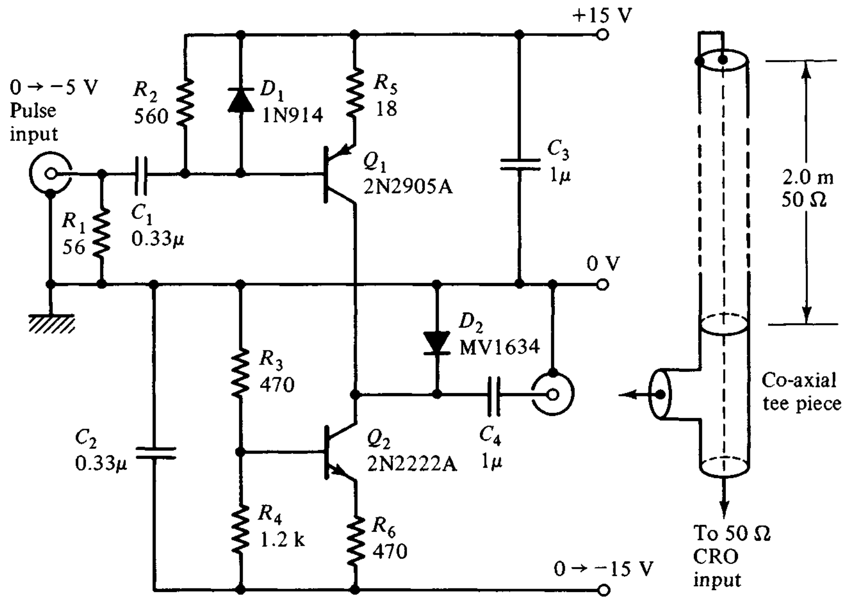

Fig. 2.9. An experimental pulse generator circuit using a tuning diode, type MV1634, to play the part of the step recovery diode, D_2.

this book.) R_5 is then chosen so that the current turned on by Q_1, $(V_T - V_{BE})/R_5$, V_T being the amplitude of the input pulse, is 200 mA when V_T is 5 V.

Now the current that is turned on in Q_1 flows into the constant current sink, Q_2, and, because it exceeds this current, a reverse current, $(I_{C1} - I_{C2})$, is established in the diode D_2. However, because Q_1 is an ordinary general purpose device, this current takes, perhaps, 10 ns to become established, and it should now be clear why a step recovery diode is designed to have a storage time of a few nanoseconds: it is necessary to establish the reverse current well in advance of the fast recovery.

Referring to Fig. 2.9, it can now be seen how this circuit generates a very short and well-shaped output pulse. When D_2 does turn off, or snap off, to use a more emphatic description, the current $(I_{C1} - I_{C2})$ is diverted, via C_4, into the two 50 Ω transmission lines which are connected in parallel to the co-axial socket shown on the right-hand side of Fig. 2.9. A voltage, $25(I_{C1} - I_{C2})$ V, is thus established across these transmission lines, but can only persist for the time taken for this voltage step to propagate along the 2 m length of line, to the short circuit, and then back again to collapse the voltage at the tee piece. As this total round trip of 4 m, at a velocity of, perhaps, 2×10^8 m/s, will take 20 ns, this should be the

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duration of the output pulse which would be seen on the oscilloscope connected to the far end of the other line, shown on the lower right-hand side of Fig. 2.9.

2.8 Constructional work

The circuit shown in Fig. 2.9 may be built up in a very conventional way, using a small circuit board, provided D_2 and C_4 are connected very close to the co-axial socket which is shown on the right-hand side of Fig. 2.9. The point is to keep the inductance of this part of the circuit as low as possible, so that very short leads are called for as well as a careful choice for C_4. A low inductance capacitor can be built up by putting several small ceramic capacitors in parallel.

The short circuit at the far end of the 2 m length of cable must also be of very low inductance. The simplest way of doing this is to slide back the braid of the cable, strip off the inner conductor's insulation, and then pull the braid over the inner conductor for a few millimetres and solder through the short circuit this forms. The kind of cable used is also important, but this point is raised in the next section.

2.9 Experimental work

Fig. 2.10 shows an oscillograph of what was actually observed with the circuit shown in Fig. 2.9, using the values and devices given on the figure. The MV1634 tuning diode which was used does not show a very fast step recovery, but it does give a well-shaped pulse when $I_{C1} = 180$ mA and $I_{C2} = 20$ mA. This means $I_{C1} - I_{C2} = 160$ mA and the output pulse is 4 V in amplitude. The positive power supply, V_+, was 15 V, while V_-, and the amplitude of the negative input pulse, were both adjusted to optimise the pulse shape. The delay in the diode turning off can be increased by increasing the magnitude of V_-, as this increases the diode forward current, I_{C2}. Similarly, increasing the amplitude of the input pulse will reduce the delay because the net reverse current, $(I_{C1} - I_{C2})$, is increased. Both adjustments influence the pulse shape because the ideal situation, shown in Fig. 2.6, where the stored charge vanishes at the same instant $n_p(x) = 0$ at the junction, is more, or less, approached.

Other tuning diodes can be found which behave in a very similar way to the MV1634. The BA138 diode gives a very similar shape of output pulse, of smaller amplitude because it has to operate at a larger value of I_{C2} in order to delay step recovery until Q_1 has been turned on fully. The BA142 diode has a faster step recovery than the MV1634, and will begin to show the limitations of a 250 MHz oscilloscope. A real step recovery

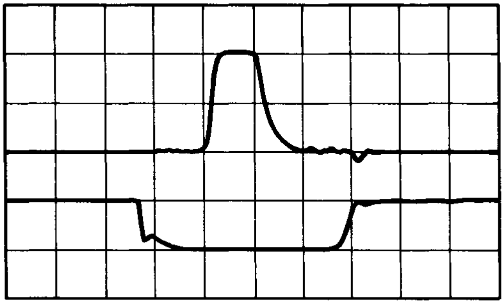

Fig. 2.10. *Waveforms observed from the experimental circuit of Fig.* 2.9. *The time base is* 20 *ns/div. The lower waveform is the input pulse on* 5 *V/div. The upper waveform is the output pulse on* 2 *V/div.*

diode, the 5082–0180 from Hewlett–Packard, is available in a conventional package but its recovery time is much too short for any analog oscilloscope to display it, and it is an expensive device: a selection of some 20 tuning diodes may be purchased for the price of a single 5082–0180.

The negative going edge of the output pulse, shown in Fig. 2.10, is slower than the rising edge. Referring to Fig. 2.1, this means that $\tau_f > \tau_r$, and there are two reasons for this. The first is that the negative going edge is only a reflection of the rising edge up to the time it reaches the co-axial tee piece, shown in Fig. 2.9. It then has to cross this tee piece and suffer the distortion due to the loading of D_2, which is now off and acting as a capacitance of about 20 pF. The second reason is the dispersion in the co-axial cable. From the simplest point of view, dispersion means an attenuation that increases with frequency. The negative going edge of the output pulse has to travel along an extra 4 m of cable on its journey to the oscilloscope, and suffer the consequent extra attenuation of its high frequency components. RG58C/U cable was used to obtain the results shown in Fig. 2.10, and this is the usual 50 Ω cable used for laboratory work which has an outside diameter of 5 mm. If a 2 m length of RG1788/U, a miniature 50 Ω cable of 1.8 mm outside diameter, is used instead, the negative going edge will be slower than that shown in Fig. 2.10 because of the greater dispersion in this smaller cable.

2.10 Conclusions

This chapter has discussed the problems of pulse generator circuit design in the particular case of the sampling pulse generator. This has to generate a very short pulse, of fixed amplitude and duration. The step recovery diode is certainly an excellent device for circuits of this kind, and it has been possible to propose an experimental circuit which uses a diode having step recovery properties, but working at a slower speed so that simple constructional and measurement techniques may be used.

Although the experimental circuit of Fig. 2.9 works at a speed which is, perhaps, two orders of magnitude slower than a real sampling pulse generator, it can still illustrate some of the problems of layout, and unexpected problems coming from component choice and test equipment, which turn up at the higher speed. Every version of a circuit of this kind will behave slightly differently, with different output pulse shape and different spurious signals appearing on the output. The length and amplitude of the pulse input, the grounding of circuit and test equipment, the earth-loops formed by the interconnection of test equipment: all these factors will influence what the experimentalist observes, and the whole point of the experimental work is to understand the real cause of every unexpected observation.

A real sampling pulse generator may, in some ways, avoid many of the difficulties that will be observed with the experimental circuit described here. This is because its final output pulse cannot be observed directly. It will be assumed that it has the correct amplitude and duration from the behaviour of the sampling gate, the subject of the next chapter, that the pulse generator controls. Another important point is that the sampling pulse generator and the sampling gate may, in a real sampling or digitising oscilloscope, be built together as one hybrid circuit: there will then be no problems introduced by a cable which has to carry the sampling pulse from generator to gate. In fact, as the next chapter will show, a sampling gate may well call for a controlling pulse that comes from a balanced source, in which case a balanced transmission line would be used to form the pulse, instead of the co-axial line shown in Fig. 2.9. Such a circuit is shown in the paper by Rush and Oldfield [12], and calls for a balanced reverse current source, in contrast to the single ended source shown in Fig. 2.9 as the single collector of Q_1. As a *circuit shape*, however, the balanced circuit is only the sum of two circuits, both having the shape of Fig. 2.9 but with one having all polarities of supplies and devices, with the exception of the centre of the circuit, D_2, reversed. This point is illustrated in Fig. 2.11 where a length, L, of balanced line, characteristic impedance Z_0, is shown connected to a balanced source of constant forward current for D_2, the step recovery diode, and a balanced pulsed source of reverse current, formed by Q_1 and Q_1'.

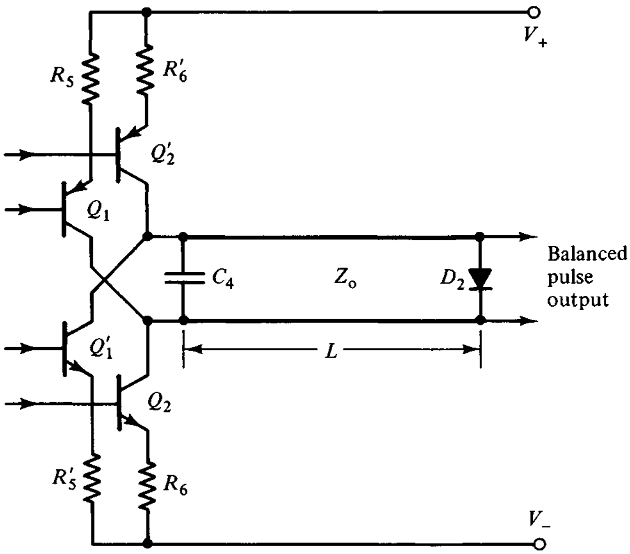

Fig. 2.11. *A balanced version of the sampling pulse generator. This is derived from Fig.* 2.9. *Components which correspond in both circuits have the same label in both, while those from the circuit of opposite polarity are marked with a dash. Bias networks and pulse inputs associated with the bases of the transistors have been omitted for simplicity.*

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