4

Comparator circuits

4.1 The analog to digital converter (ADC)

The sub-system which follows the sample and hold circuit, and its sampling pulse generator, in a digitising oscilloscope will be an ADC. In this particular case, the function of the ADC is to convert the output from the sample and hold circuit, which is an analog signal carried by a single channel, into a digital representation of this analog signal, carried in parallel by, typically, eight lines. An eight bit representation would be only just adequate for a digitising oscilloscope because this would give 256 discrete levels, meaning that a vertical display, 8 cm high, would have a vertical resolution of about 0.3 mm. This is about the same as a typical CRO spot diameter. More bits would be needed to handle the display offset, the sign of the signal, and the sensitivity range, but only the circuit problems of the ADC are considered in this chapter.

ADCs are not only found in digitising oscilloscopes. Any instrumentation problem that calls for an interface between a transducer or a sensor, nearly all of which give out an analog signal, and a digital computer, will call for an ADC. There is also another field of application, as Gordon [1] has pointed out in an important review. This is the field of communications where digital techniques are taking over more and more, in telephony and in television.

In its most basic form, an ADC may be considered as a sub-system, or device, of the kind shown in Fig. 4.1, where it is assumed that the analog input is always positive, lying between zero and V_{ref}, and is to be converted into an eight bit binary coded output. This device would usually be a single silicon integrated circuit.

There are a very large number of ways in which the ADC function may be realised. Gordon [1] identified twelve distinct types, six of which may

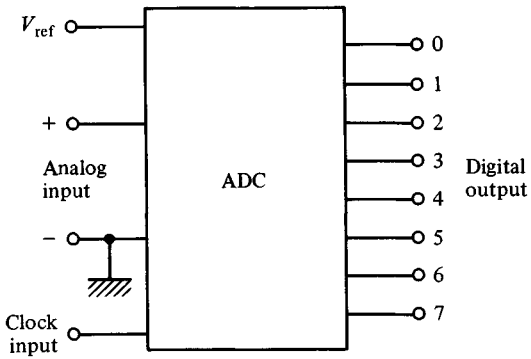

Fig. 4.1. *The analog to digital converter* (*ADC*).

be classified as slow and six fast. The slow designs use counting techniques to generate the digital representation of the analog signal. They all rely on converting the analog voltage into a time: for example, the time for a current to charge a capacitor. Fast designs use some kind of parallel data processing technique.

Nearly all ADC designs involve *comparators*. These circuits are the subject of this chapter and, as the name implies, their function is to compare a time varying signal with either another signal, or with some reference level. The comparator determines the instant when a charging capacitor has a certain voltage across it, or whether a voltage is above or below a certain level.

4.2 The flash ADC

Of all ADC designs, the so-called flash ADC is the fastest and is the one used in all fast digitising oscilloscopes. It is also the design which makes the most use of comparator circuits.

Fig. 4.2 shows the kind of structure that a flash ADC would have. The origin of this idea, as Kandiah has pointed out [2], is very old indeed. It is found in the 1940s, in the earliest pulse height analysers of nuclear physics instrumentation.

Fig. 4.2 has been drawn so that it corresponds to Fig. 4.1: again the eight bit digital output has been assumed. The flash ADC works by having 255 comparators to detect exactly where the analog input signal level lies, relative to the 256 levels that an eight bit digital output is able to represent. These comparators are represented by simple operational amplifier symbols in Fig. 4.2. An operational amplifier can, of course, be used as a comparator, but certainly not as a fast one.

The outputs from the 255 comparators, shown in Fig. 4.2, represent the

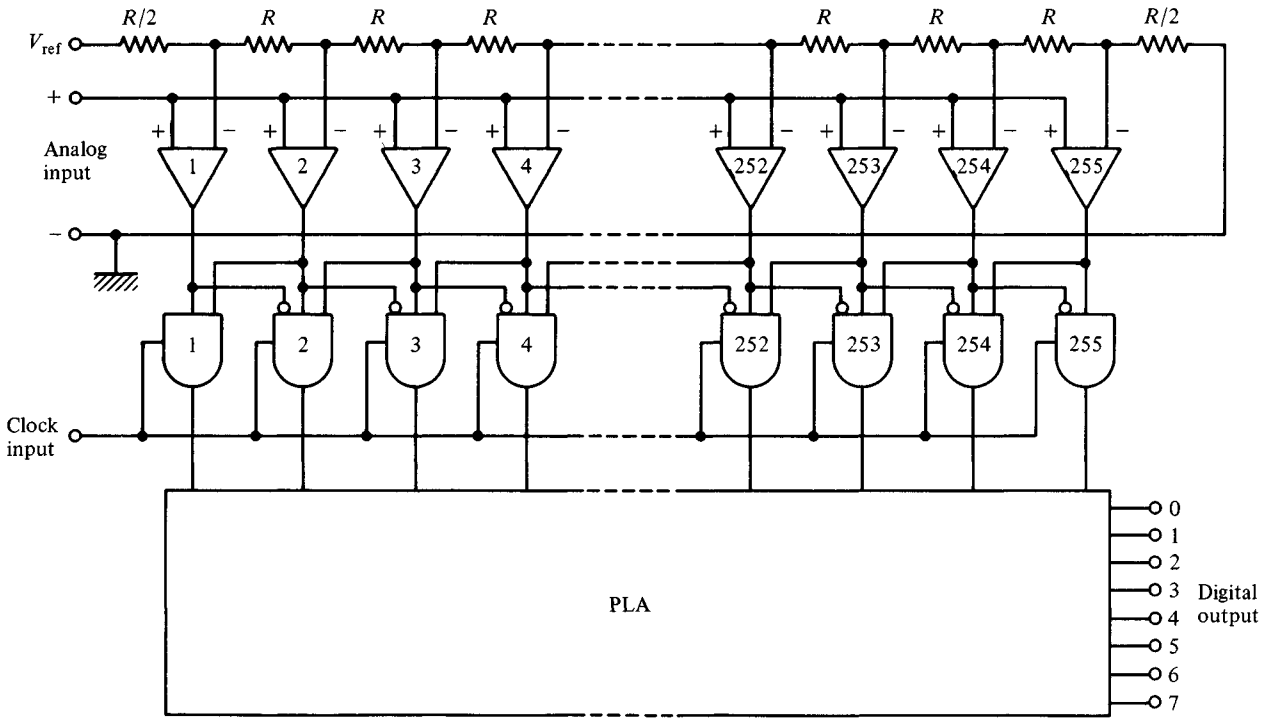

Fig. 4.2. The internal details of a typical flash ADC.

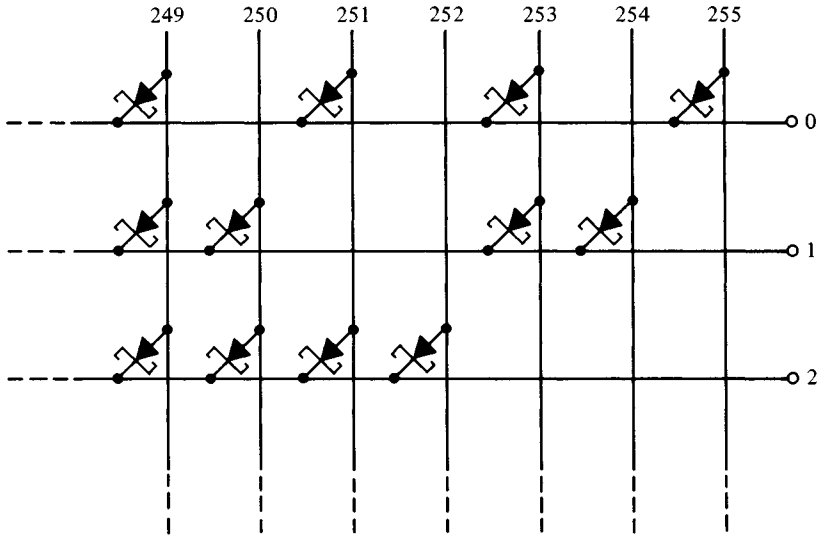

Fig. 4.3. *The PLA in Fig.* 4.2 *may be realised by means of a simple Schottky diode matrix. Here the details of the top right-hand corner of such a matrix are shown.*

analog signal level in what is called a 'thermometer code' [3]. This term is used because, as a glance at Fig. 4.2 will show, all the comparators which take a reference voltage on their inverting inputs that lies below the analog input signal level, will have their outputs high. In contrast, all the comparators which have high reference levels will have their outputs low.

The thermometer code, described above, has to be converted into the standard binary number representation that is needed at the output of the ADC. There are many ways of doing this encoding, and the method presented here has been adapted from the paper by Peterson [4], which described one of the earliest realisations of a flash ADC as a single monolithic silicon integrated circuit. This uses the 255 AND gates, shown in Fig. 4.2, to convert the thermometer code from the 255 comparator outputs into a '1 out of 255' representation. The only AND gate that can have a '1' at its output is the one which has the input, reading from left to right in Fig. 4.2, '011'. That is exactly the 'thermometer' reading. The '1 out of 255' code is then easily converted into the eight bit binary code. This could, for example, be done by means of a programmable logic array (PLA), and the simplest PLA would be a diode matrix. For completeness, a small part of such a diode matrix is shown in Fig. 4.3.

4.3 How system considerations influence circuit design

Having gone into some detail about the realisation of one particular kind of ADC, and also one particular kind of encoding structure for its output, it is now possible to bring up a point which is of crucial importance to electronic circuit design in general. This is the way in which system considerations influence circuit designers and play a major role in the kind of circuit shape at which they may finally arrive.

In the particular case being considered here, this discussion can begin by bringing in a very simple feature of the ADC that is shown in both Figs. 4.1 and 4.2. This is that the ADC must have a 'clock input'. The function of this clock input signal is to enable the ADC during the time that its analog input is held constant. In the digitising oscilloscope this time is after the sampling pulse, and after the sample and hold circuit has settled down to its new output value. The clock signal would be a square wave, of alternately '0', when the sampling pulse would be generated and the new held sampled value would be established, and then '1', when all the AND gates, shown in Fig. 4.2, would be enabled and the eight bit digital output would be available at the output of the ADC.

Now the above is only one way of realising this essential demand, of the complete digital system, that the output of the ADC is only valid when the analog input is constant. Having decided to solve the problem in this way, the circuit designer's attention would be directed towards the circuit detail, or circuit shape, of the AND gates in Fig. 4.2, and deciding how the enable function could best be implemented.

It is obvious, however, that the enable function could also be done by designing either the comparator circuits or the PLA, in Fig. 4.2, so that these circuits could accept the clock input signal. In fact, one of the most interesting published designs for a flash ADC, and one of the very first eight bit video ADCs to be made as a single integrated circuit [4], has the clock signal fed to comparators, AND gates, and the output encoding circuits. In this way it proved possible to make the ADC behave as its own sample and hold. It is clear that this overall system influence on the details of circuit design is a point of great importance, and it is fortunate that the flash ADC problem can illustrate it so well. To give this illustration, the remainder of this chapter considers simple comparator circuits briefly and then the evolution of the kind of comparator circuit design that has taken system considerations into account. This leads to the theory of such circuits and work with an experimental circuit.

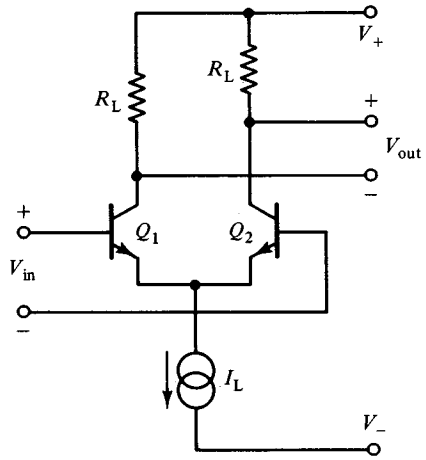

Fig. 4.4. *The simple long tailed pair circuit. A first step towards a good circuit shape for a comparator.*

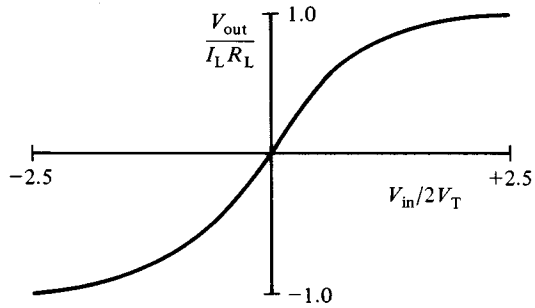

Fig. 4.5. *The transfer function for the circuit shown in Fig.* 4.4.

4.4 The simple comparator

A simple comparator could be made by using a device like an operational amplifier, and then omitting any feedback. The input circuit of such a simple comparator would almost certainly be the well-known, long tailed pair circuit, shown in Fig. 4.4, and this can be taken as a starting point in the evolution of a really fast kind of comparator circuit.

Fig. 4.4 has the transfer function shown in Fig. 4.5. This follows [5] from the equation for the collector current of a bipolar transistor. In general:

$$I_C = I_{CBO} \exp(V_{BE}/V_T) \tag{4.1}$$

where,

$$V_T = kT/e \tag{4.2}$$

which is about 25 mV at room temperature.

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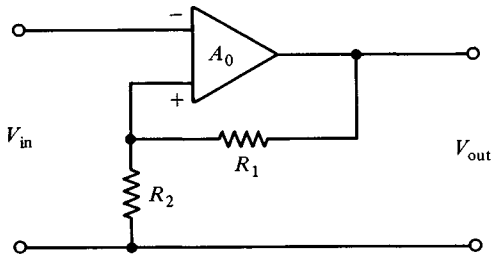

Fig. 4.6. Positive feedback applied across a simple operational amplifier can produce a transfer function of the double valued form shown in Fig. 4.7.

Because,

$$V_{in} = V_{BE1} - V_{BE2} \tag{4.3}$$

$$V_{out} = (I_{C1} - I_{C2})\, R_L \tag{4.4}$$

and

$$I_L = I_{C1} + I_{C2} \tag{4.5}$$

the identity,

$$\tanh(x) = [\exp(x) - \exp(-x)]/[\exp(x) + \exp(-x)] \tag{4.6}$$

may be used to obtain,

$$V_{out}/I_L R_L = \tanh(V_{in}/2V_T) \tag{4.7}$$

which is the function shown in Fig. 4.5.

Obviously, the simple circuit shown in Fig. 4.4 would need additional output stages to give it more gain and both to level shift the output and make it single ended. These additions would not radically change the form of the transfer function, shown in Fig. 4.5, and it is with reference to this function that some obvious problems can be identified.

4.5 The use of positive feedback

The most striking feature of Fig. 4.5 that needs some attention, if the circuit of Fig. 4.4 is to lead to a useful comparator circuit, is the absence of any clear threshold input voltage at which the output voltage changes rapidly from the low state to the high. An increase in the circuit gain would tend to produce a sharper threshold, and it is from this point of view that the idea of applying positive feedback to increase the gain seems a sensible direction for the circuit designer to choose [6].

For example, the circuit idea shown in Fig. 4.6 uses positive feedback across a standard operational amplifier. As the feedback fraction is

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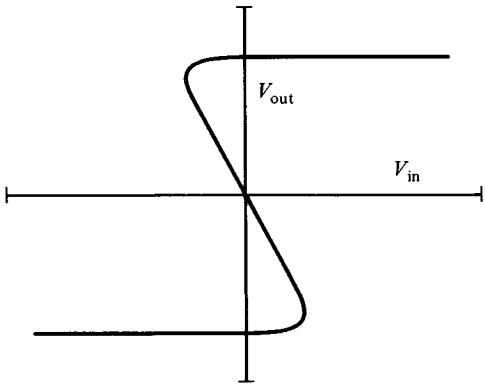

Fig. 4.7. *The transfer function of Fig.* 4.6 *when* $A_0 R_2/(R_1+R_2) > 1$.

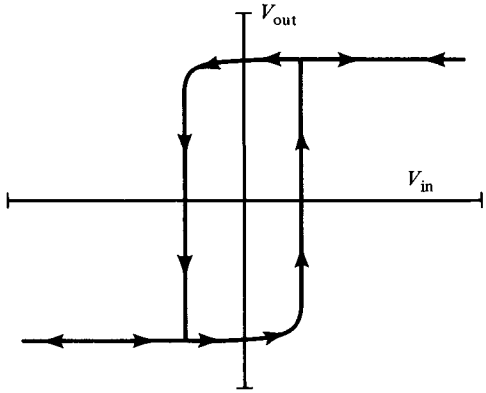

Fig. 4.8. *The double valued transfer function of Fig.* 4.7 *cannot be followed. The circuit of Fig.* 4.6 *exhibits a trigger action and hysteresis.*

increased, the transfer function changes from the form shown in Fig. 4.5 to give a higher and higher gain, passing though $+\infty$ to change, discontinuously, to $-\infty$ at the critical point where the overall loop gain, $A_0 R_2/(R_1+R_2)$, is unity. If the amount of positive feedback is increased still further, the transfer function takes on the interesting form shown in Fig. 4.7, a feature of electronic circuits with positive feedback that was first clearly explained by Williams [7].

A circuit cannot, of course, operate smoothly along a multivalued transfer function of the kind shown in Fig. 4.7. The circuit now has a trigger action and exhibits hysteresis, as shown in Fig. 4.8. In fact, Fig. 4.6 is often referred to as a 'Schmitt trigger circuit' as it is very similar, as a circuit shape, to a very early circuit idea published by O. H. Schmitt [8] in 1938.

So, it does appear that positive feedback is a good idea for comparator circuits. Positive feedback can provide some kind of trigger threshold for the circuit to operate on when the input voltage passes some predetermined reference level, and can also provide hysteresis which, as Fig. 4.8 shows, implies that there can be a small region around the critical threshold within which the circuit will ignore fluctuations and noise on the input signal. These are useful features but positive feedback along the lines of Fig. 4.6 does not lead to a good comparator circuit. A far more subtle approach is called for which maintains the balanced input of the circuit shown in Fig. 4.4, and also takes the system considerations, discussed at length in section 4.3, into account, particularly the fact that a clock signal could be introduced into the comparator circuit.

4.6 Positive feedback and symmetry

The trouble with Fig. 4.6, as a circuit idea, is that the symmetry of the operational amplifier's input circuit, illustrated by Fig. 4.4, has been lost. One input is used for the signal and the other is used for the positive feedback. Is it possible to apply positive feedback to both input terminals? Not directly, and not through potential dividers, because this would virtually destroy the possibility of using these input terminals for a signal input. For example, a direct connection of positive output terminal to negative input terminal, and also negative output to positive input, in Fig. 4.4, simply makes the input and output terminals one and the same.

What is needed is an extra pair of input terminals, which may be used to accept the positive feedback, while the original input terminals continue to accept the signal. This idea is shown in Fig. 4.9, where two long tailed pair circuits have been wired in parallel, as far as their collector loads are concerned. Both have independent tail currents, I_{L1} and I_{L2}, and one pair, Q_1 and Q_2, accepts the input signal, while the other pair, Q_3 and Q_4, has 100% positive feedback applied to it.

The circuit of Fig. 4.9 has some very remarkable properties. If I_{L2} is made zero, the circuit is identical to Fig. 4.4 and is a simple amplifier with the transfer function shown in Fig. 4.5. If I_{L2} is now increased gradually from zero, positive feedback is being applied and the gain of the circuit increases until, when $I_{L2} R_L = 2V_T$, using the symbolism of section 4.4, the gain becomes infinite. Further increase of I_{L2} causes the circuit to become a trigger circuit, with the kind of transfer function shown in Figs. 4.7 and 4.8.

A full analysis of this kind of circuit will be given later in this chapter when the final form, which will be the experimental circuit for this chapter,

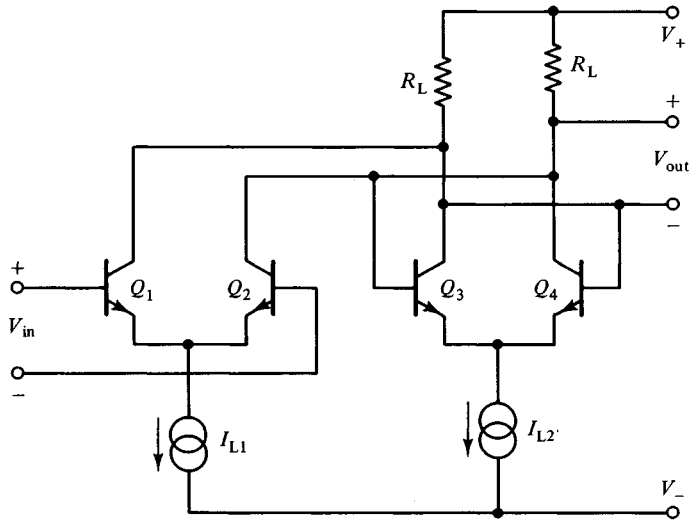

Fig. 4.9. *Applying positive feedback and yet maintaining a balanced circuit.*

has been reached. There are still a number of points to consider. What has been achieved so far is a circuit which can have radically different behaviour, illustrated by the contrast between the transfer functions shown in Figs. 4.5 and 4.8, simply by changing the value of a current, I_{L2}. This immediately suggests the possibility of using the clock signal to control I_{L2}. In fact, the key to an excellent comparator, which will really fit into a digital system, lies in the clock control of both I_{L1} and I_{L2}.

4.7 Introducing the clock signal

A circuit of the shape shown in Fig. 4.9 may have been first described by Lynes and Waaben [9] when it was applied to a sense amplifier problem. The use of the circuit as a comparator was presented by Slemmer [10] at about the same time. All these authors realised that a very important step forward in the technique of making very fast and very sensitive amplifying circuits, specifically within the environment of a digital system, could be taken if the clock signal was made to operate the circuit of Fig. 4.9 in two distinct states.

During what might be called the sense state, $I_{L1} = I_L$ and $I_{L2} = 0$. The circuit then operates as a straightforward amplifier, and a small output voltage, v_o, is developed. This will appear across the collector junction of Q_3 as $-v_o$, while across the collector junction of Q_4 it will appear as $+v_o$; Q_3 and Q_4 are off at the moment, and v_o is typically a few millivolts.

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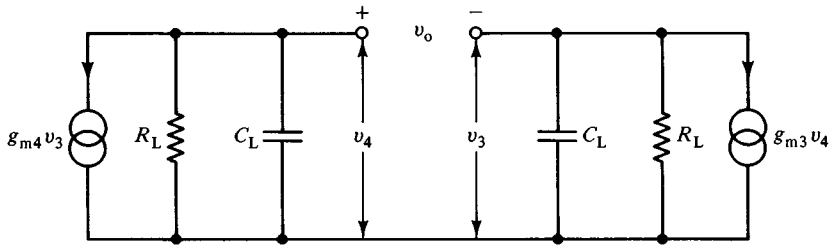

Fig. 4.10. *An equivalent circuit for Fig.* 4.9 *when* $I_{L1} = 0$ and $I_{L2} = I_L$.

During what might be called the latch state of the circuit shown in Fig. 4.9, $I_{L1} = 0$ and $I_{L2} = I_L$. Also $I_L R_L$ is made large enough to put Q_3 and Q_4 into regeneration, that is to have the behaviour shown in Fig. 4.8, and the final state which the circuit latches into will be decided entirely by the initial values of the collector junction voltages discussed in the previous paragraph. It is possible to take this discussion considerably further at this stage, because the equation of motion for this circuit is easily written.

Fig. 4.10 shows a very much simplified small signal equivalent circuit for the circuit shown in Fig. 4.9. It is assumed that $I_{L1} = 0$ and $I_{L2} = I_L$. The transistor Q_3 has v_3 across it, while the transistor Q_4 has v_4. The output voltage is then $v_o = v_4 - v_3$. The total capacitance from each output terminal to the common emitters of Q_3 and Q_4 is represented by C_L, and other capacitances are neglected. This is an accurate enough model to illustrate the important properties of this circuit. A full analysis has been given by Zojer, Petschacher and Luschnig [11].

The transistors Q_3 and Q_4 share the current $I_{L2} = I_L$ equally, so that their mutual conductances are

$$g_{m4} = g_{m3} = I_L/2V_T \tag{4.8}$$

where the symbolism of equation (4.2) is being used again. The nodal equations for Fig. 4.10 are

$$g_{m4}v_3 + v_4/R_L + C_L\,dv_4/dt = 0 \tag{4.9}$$

and

$$g_{m3}v_4 + v_3/R_L + C_L\,dv_3/dt = 0 \tag{4.10}$$

As $v_o = v_4 - v_3$ it follows, from subtracting equation (4.10) from equation (4.9), that

$$C_L R_L\,dv_o/dt + (1 - g_m R_L)v_o = 0 \tag{4.11}$$

where $g_m = g_{m3} = g_{m4}$, from equation (4.8).

Equation (4.11) may be solved by substituting $v_o = V\exp(at)$, where

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V is the initial value of v_o that has been set by the input signal during the sense state of the circuit which was described above. This shows that

$$a = (g_m R_L - 1)/C_L R_L \tag{4.12}$$

which shows that the circuit is regenerative once I_L is increased sufficiently to make $g_m R_L > 1$. From equation (4.8) this means that I_L must exceed $2V_T/R_L$, as stated above. The output voltage, v_o, would then increase exponentially, with the time constant $C_L R_L/(g_m R_L - 1)$ (see equation (4.12)) until the circuit ran into the non-linear regime and latched into a state where either Q_3 was on and Q_4 off, or *vice versa*.

Clearly, the circuit designer's goal would be to make the time constant $C_L R_L/(g_m R_L - 1)$ as small as possible. This can be done by increasing R_L, but once R_L exceeds $1/g_m$ by a factor of about 10, there is no point in any further increase because the time constant has fallen to a limit of C_L/g_m. In any case, R_L would not be made so large that the transistors Q_3 and Q_4 could saturate.

The circuit's time constant may, therefore, be taken to be C_L/g_m, and this could be well below 100 ps in an integrated circuit. It follows that Fig. 4.9 is a circuit shape of great potential, and should lead to an excellent design for a fast comparator circuit which will fit into a digital system environment. The final form of such a comparator circuit will now be given, and then experimental work can begin.

4.8 The final circuit shape

Fig. 4.11 shows the additional features that should be added to Fig. 4.9 in order to make the basis for an excellent fast comparator.

First, the load resistors, R_L in Fig. 4.9, have been split into two, R_1 and R_2 in Fig. 4.11. This idea is found in the work of Peetz, Hamilton and Kang [12], and is an excellent way of optimising the bandwidth of the sense amplifier state, which calls for a low value of R_L, and the speed of the latch state, which calls for a high value of R_L.

The second addition shown in Fig. 4.11 is that emitter followers, Q_5 and Q_6, have been added to reduce the capacitive loading, C_L in equation (4.11), and also to increase the reverse bias across the collector junctions of Q_3 and Q_4 by about 700 mV. This reduces C_L still further, and generally improves the gain-bandwidth of the circuit. The output from the circuit can then be taken from the emitters of Q_5 and Q_6.

Finally, Q_7 and Q_8 have been added to switch the I_L either into the sense amplifier, Q_1 and Q_2, or into the latch, Q_3, Q_4, Q_5 and Q_6, depending upon whether the clock signal is low or high.

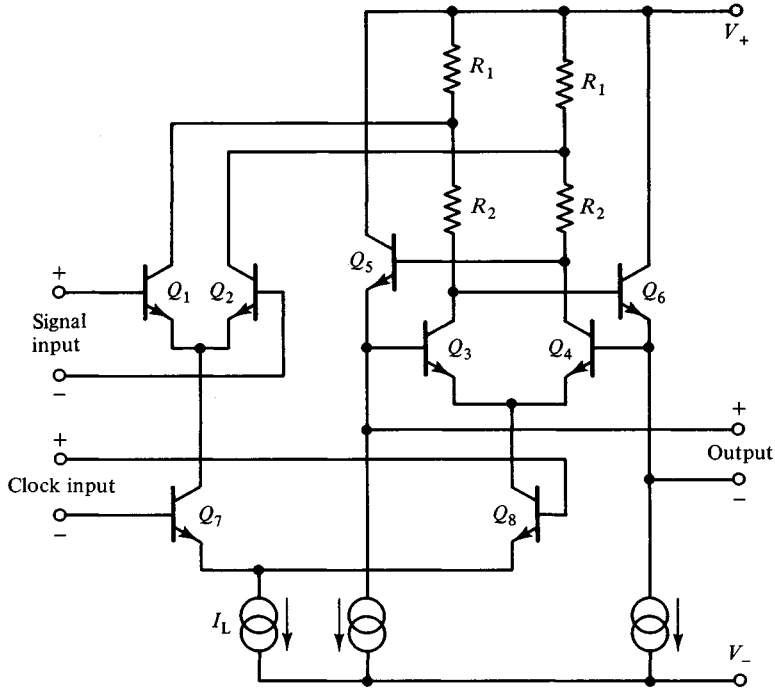

Fig. 4.11. *The final circuit shape for a high speed comparator circuit.*

Further additions would have to be made to the circuit in order to put the correct level shifts onto the inputs and outputs, and to make both the clock input accept, and the circuit output supply, signal levels compatible with the system's logic. All this would have to be done within the environment of one VLSI circuit, one which would include all the features shown in Fig. 4.2. Some examples of this kind of advanced design may be seen in the references that have already been given ([3], [4], [11] and [12]) and in the work of Inoue *et al.* [13], van de Grift and van de Plassche [14], and Yoshii, Asano, Nakamura, and Yamada [15]. A very interesting design using a new bipolar process has been published by Hotta *et al.* [16], and the circuit idea of Fig. 4.9 has been tried out in gallium arsenide [17] and in CMOS [18]. The problems of actually using these advanced circuits have been discussed in a very useful paper by Emmens and Lonsbourough [19].

4.9 An experimental circuit

The experimental circuits for this chapter will not be the advanced integrated circuits discussed above. In order to get an understanding of

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the interesting comparator idea shown in Fig. 4.11, it is only necessary to construct a minimum amount of hardware, and the need for reasonable device matching can be met by using transistor arrays.

The first experimental circuit is shown in Fig. 4.12 and may be used to investigate the quasi-static behaviour of the circuit: its critical signal levels and its hysteresis. This will illustrate some unexpected and important behaviour.

Fig. 4.12 is realised using two CA3046 transistor arrays. Q_1 and Q_2 belong to one array, while $Q_{1'}$ to $Q_{4'}$ belong to the other. The tail current for Q_1 and Q_2 has been made about 1 mA, and is kept constant during the experimental work. It is the tail current for the regenerative part of the circuit, that is I_{L2} in the previous Fig. 4.9, which can be varied by means of a variable supply, V_{L2} in Fig. 4.12, that is connected to R_8. This simulates the conditions under which the circuit would operate at high speed, because a constant tail current for Q_1 and Q_2 maintains the signal level across R_3 and R_5, which this sensing part of the circuit transfers to the latch part of the circuit. Such a situation would apply during fast clocking of the real circuit (Fig. 4.11) in which the signal level, referred to above, would remain stored on the collector junction capacitances of $Q_{1'}$ and $Q_{2'}$.

It was shown in section 4.7 that there was no point in increasing the load resistance for the latch part of the circuit above $10/g_m$. For the current levels chosen for Fig. 4.12, this means that (R_3+R_4), and (R_5+R_6), would be kept below 250 Ω. A value of 122 Ω has been chosen. This effects a sensible split in the load resistors, as discussed at the beginning of section 4.8, with $R_3 = R_5 = 22\ \Omega$ and $R_4 = R_6 = 100\ \Omega$.

4.10 Hysteresis measurements

For the first experimental measurements, the circuit of Fig. 4.12 should be connected to a d.c. signal source that will provide an input of ±50 mV. This can be done by using a variable power supply and a potential divider. A similar variable power supply should be used for V_{L2}. An oscilloscope on XY display should then be used to show the emitter voltage of $Q_{3'}$, or $Q_{4'}$, against V_{L2}.

Now set $V_{L2} = +5$ V and V_{in} to, say, +10 mV. This positive input signal would be expected to make the emitter of $Q_{4'}$ go low once the tail current of $Q_{1'}$ and $Q_{2'}$ is increased by reducing V_{L2}. It might be thought that this would happen discontinuously, at some critical level of V_{L2}, but this is not so. Referring to Figs. 4.5, 4.7 and 4.8, where the idea of circuit hysteresis was first introduced, it is clear that a positive input must produce a

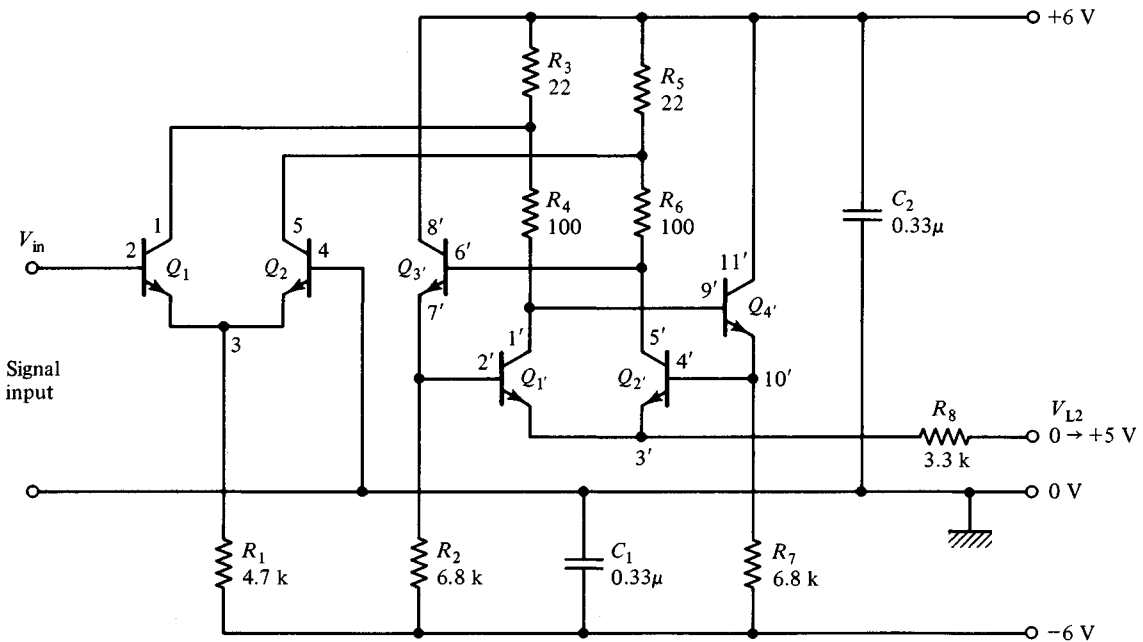

Fig. 4.12. *An experimental circuit for static measurements on the comparator.*

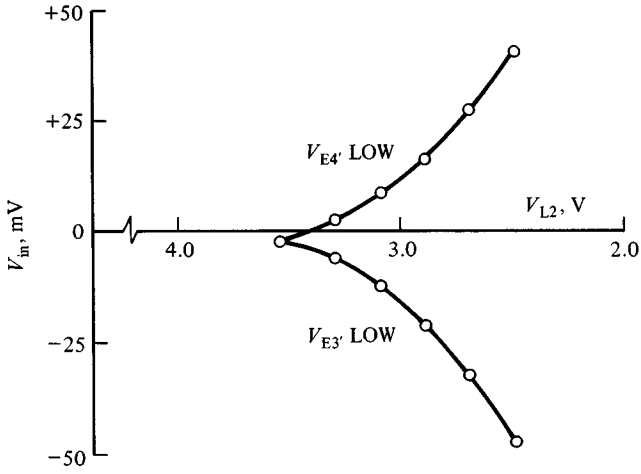

Fig. 4.13. *Experimental measurements of the hysteresis in the circuit shown in Fig.* 4.12. V_{L2} *is held constant and* V_{in} *varied over the range* ± 50 *mV. For* increasing V_{in}, *the discontinuous transition* $V_{E3'}$ *LOW to* $V_{E3'}$ *HIGH, and, of course,* $V_{E4'}$ *HIGH to* $V_{E4'}$ *LOW, occurs when the upper curve is crossed. The discontinuous transition,* $V_{E4'}$ *LOW to* $V_{E4'}$ *HIGH, and, of course,* $V_{E3'}$ *HIGH to* $V_{E3'}$ *LOW, occurs when the lower curve is crossed, during a* decrease *in* V_{in}. *The small negative offset input voltage, shown by these results, can be attributed to the particular CA*3046 *being used for* Q_1 *and* Q_2.

positive output when the *initial* state of the circuit has a transfer function of the kind shown in Fig. 4.5. Hysteresis only applies when the circuit has been put into the state represented by the transfer functions shown in Figs. 4.7 and 4.8, and will then only be observed if the input voltage is varied.

It follows that hysteresis may be observed if V_{L2} is reduced, step by step, and, at each step, V_{in} is varied slowly from, say, -50 mV to $+50$ mV, and then back again. As V_{in} is varied, a sudden discontinuous change in voltage level at the emitter of $Q_{3'}$ and $Q_{4'}$, should be observed. The values of V_{in} and V_{L2} at which these discontinuities occur lie on the two curves shown in Fig. 4.13. It is the space between these two curves which is equal to the width of the hysteresis loop, shown in Fig. 4.8. As the tail current of $Q_{1'}$ and $Q_{2'}$ increases, so increasing the loop gain of this regenerative circuit, the hysteresis loop gets wider and wider. When $V_{L2} = 0$, the loop is so wide that the circuit is really 'latched': no matter how large the input signal, the voltage across R_3 and R_5, due to Q_1 and Q_2 is not big enough to push the circuit into its other state.

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4.11 Hysteresis theory

Before asking what the implications of the circuit hysteresis might be, which, of course, brings up the dynamic performance, it is interesting to find out why the experimental results lie on two curves of the shape shown in Fig. 4.13.

Referring to Fig. 4.12, the difference between the currents in Q_1 and Q_2 is

$$I_{C1} - I_{C2} = I_{L1} \tanh (V_{in}/2V_T) \tag{4.13}$$

where I_{L1} is the current in R_1. This causes a voltage $I_{C1} R_3 - I_{C2} R_5$ to be transferred to $Q_{1'}$ and $Q_{2'}$. Because $R_5 = R_3$ this voltage may be written $(I_{C1} - I_{C2}) R_3$. When V_{L2} falls from $+5$ V to zero, and I_{L2} begins to flow, an additional voltage $(I_{C1'} - I_{C2'})(R_3 + R_4)$ will be added. This follows because $R_4 = R_6$. The action of the circuit may be concisely summed up by the single equation

$$y = x \tanh (y + z) \tag{4.14}$$

where

$$y = (I_{C1'} - I_{C2'})(R_3 + R_4)/2V_T \tag{4.15}$$

$$x = I_{L2}(R_3 + R_4)/2V_T \tag{4.16}$$

and

$$z = (I_{L1} R_3/2V_T) \tanh (V_{in}/2V_T). \tag{4.17}$$

Now the experimental results of Fig. 4.13 were presented as measurements made by fixing V_{L2}, that is I_{L2}, and varying V_{in}. For analysis, however, it is simpler to consider the alternative, but more tedious, experiment in which V_{in} is fixed, and I_{L2} is decreased to take the representative point, (V_{L2}, V_{in}) in Fig. 4.13, across the critical hysteresis boundary. From this point of view, z, given by equation (4.17), is a constant, and the hysteresis boundary is given by the values of I_{L2} at which dy/dx becomes infinite.

From equation (4.14)

$$dy/dx = \tanh (y + z) + [x/\cosh^2 (y + z)]\, dy/dx \tag{4.19}$$

which, using equation (4.14) to substitute for x and rearranging, may be written

$$dy/dx = [\tanh (y + z)]/[1 - 2y/\sinh 2(y + z)]. \tag{4.20}$$

It follows that $dy/dx = \infty$ at values of y given by the solution of the transcendental equation

$$\sinh 2(y + z) - 2y = 0. \tag{4.21}$$

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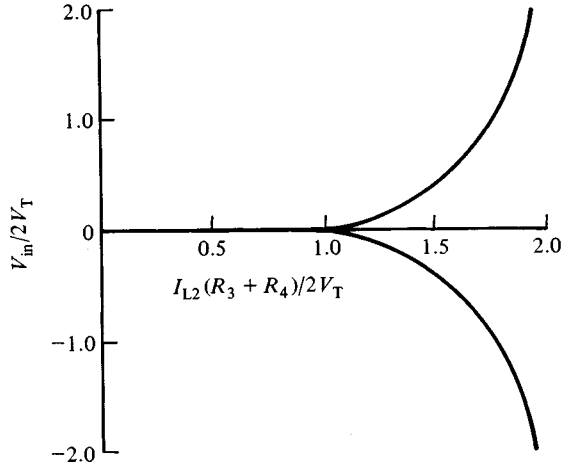

Fig. 4.14. *The theoretical hysteresis boundaries for the circuit shown in Fig.* 4.12, *calculated for* $I_{L1}R_3/2V_T = 0.5$.

These values of y may then be used in equation (4.14) to find the corresponding values of x. All this is easily done on a programmable calculator. The program takes in a value of $V_{in}/2V_T$, calculates z from equation (4.17), finds the root of equation (4.21) by using the Newton–Raphson method, and finally gives the value of x using equation (4.14).

The results are shown in Fig. 4.14 and, when these are scaled correctly using the component values given in Fig. 4.12, very close agreement is found between these theoretical curves and the experimental results shown in Fig. 4.13, for small values of V_{in}. The experimental circuit does not show a clear saturation for large positive values of V_{in} because a simple resistor, R_1 in Fig. 4.12, has been used to define I_{L1}, instead of a constant current sink. This means that Q_1 has a gain of R_3/R_1 to large positive inputs, instead of giving the zero gain shown in Fig. 4.5.

4.12 The implications of hysteresis

Hysteresis, of the kind considered in the previous two sections, can give rise to interesting time dependent errors in digital systems which dispense with a sample and hold circuit in advance of the ADC, and call for the ADC to implement its own sample and hold function under the control of the clock signal. This problem has been discussed very clearly by Peetz *et al.* [12]. The clock signal will be arranged to switch the circuit from the sense state to the latch state, as described in section 4.7, as rapidly as

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possible. The effect of this may be imagined by considering the transfer functions shown in Figs. 4.5, 4.7 and 4.8. In a matter of a few nanoseconds the transfer function becomes a hysteresis loop, and then the width of this hysteresis loop begins to expand, starting with negligible width. The actual value of the width, in terms of input voltage variation, is given by the distance between the two curves shown in Fig. 4.14.

Once inside the hysteresis loop, the representative point is captured unless it is moving so fast that it can catch up and overtake the other side of the expanding loop. This can clearly happen with very fast signals that enter the loop when it has only just started to expand. As Fig. 4.14 shows, once I_{L2} is really established, the velocity of hysteresis loop expansion becomes very large indeed.

If the representative point does succeed in crossing the hysteresis loop before it fully expands, then the circuit will latch high for the signal coming from the $V_{in} < 0$ side, and low for one entering from the $V_{in} > 0$ side. This is the opposite way around when compared to slow signals, despite the fact that the actual value of both fast and slow signals was the same at the instant the clock signal initiated the latch state of the circuit.

It is for these reasons that a sample and hold circuit must precede the ADC in a very fast digitising oscilloscope. When lower frequencies are being handled, it is possible to make the ADC operate as its own sample and hold [12].

4.13 Dynamic measurements

Fig. 4.15 shows a second experimental circuit. This can be used to make dynamic measurements on the high speed comparator circuit idea that was first shown in Fig. 4.11.

The circuit shown in Fig. 4.15 is easily constructed by adding some more work to the first experimental circuit, the one shown in Fig. 4.12. The transistors Q_3 and Q_4, in Fig. 4.15, are already available on the CA3046 which contains Q_1 and Q_2. Other components have been added to make Q_3 and Q_4 perform the same function that Q_7 and Q_8 perform in Fig. 4.11: a constant tail current is switched repetitively either to Q_1 and Q_2, for the sense state of the circuit, or to $Q_{1'}$ and $Q_{2'}$, for the latch state.

The clock signal for the circuit shown in Fig. 4.15 is provided by a simple square wave generator which is RC coupled to the base of Q_4. This makes for a very simple experimental circuit, but care must be taken not to overdrive Q_4. To set the correct square wave input level, which will be less than 150 mV peak to peak, the signal at the top of R_1, in Fig. 4.15, should be viewed on a d.c. oscilloscope. A square wave, centred on a d.c.

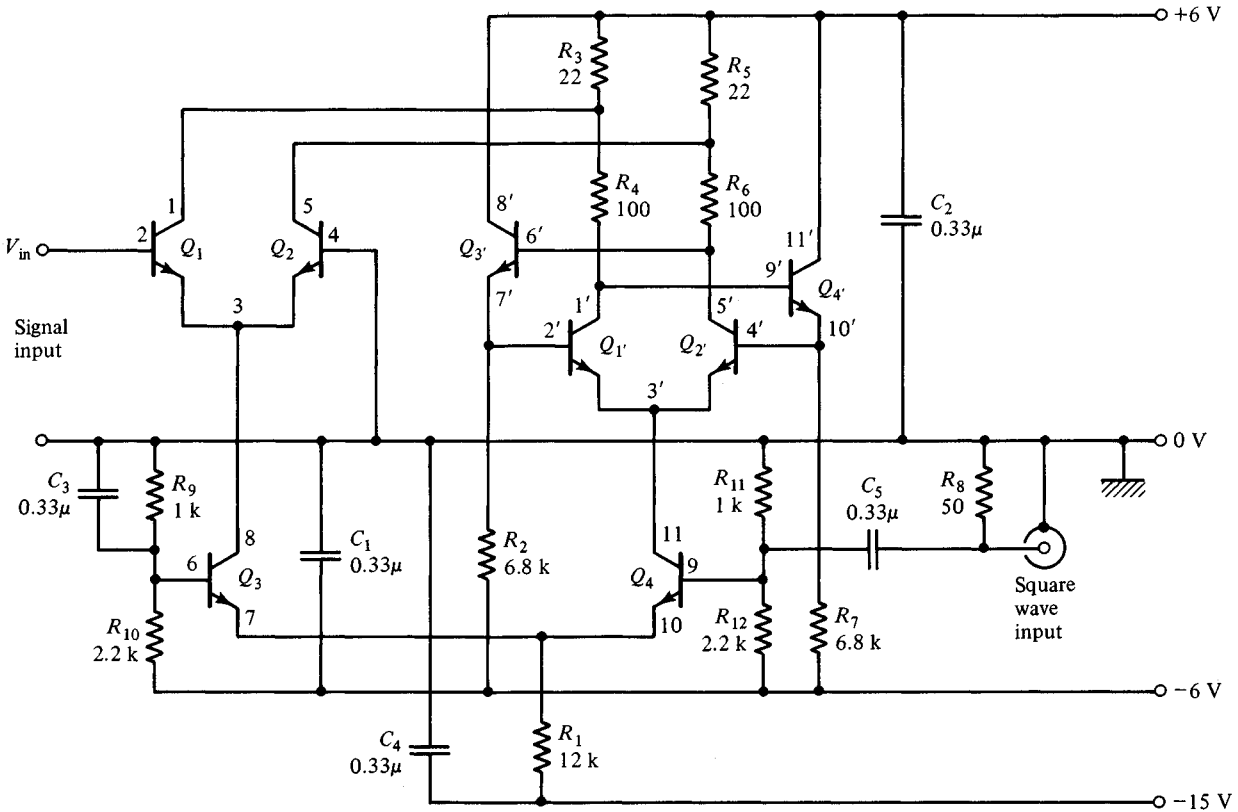

Fig. 4.15. *An experimental circuit for dynamic measurements on the comparator.*

level between -2.5 V and -3.0 V, should be seen, and the correct input level will have been reached just before the negative amplitude of this square wave stops increasing as the input level is increased.

The dynamic performance of the circuit may now be observed by connecting two high impedance probes to the emitters of $Q_{3'}$ and $Q_{4'}$ and viewing the waveforms on a dual beam oscilloscope, using a.c. coupling and 50 mV/div sensitivity. A small d.c. input signal is then applied to the circuit, in just the same way as was done in the hysteresis measurements described in section 4.10, and this d.c. input signal is varied from, say, -25 mV to $+25$ mV. A square wave of about 100 mV peak to peak should then be observed on the emitter of $Q_{3'}$, for negative inputs, changing over to be on the emitter of $Q_{4'}$, for positive inputs. The change over should be very abrupt, and should occur close to the same small offset voltage that was found when the measurements of hysteresis were made. This is the offset shown in Fig. 4.13, but note that exact agreement should not be expected, for an important reason that will be discussed later.

At this stage, the dynamic behaviour of the circuit is much more complicated than that predicted by the simple model outlined in section 4.7. This model led to the first order differential equation (4.11) which involved the time constant C_L/g_m. In the experimental circuit, Fig. 4.15, C_L/g_m is only a few nanoseconds at the moment, and the dynamic behaviour is determined by a number of factors, because the experimental circuit is a discrete component circuit which has been laid out on quite a large scale. To make contact with the kind of dynamic performance that an integrated circuit would have, the experimental circuit must be made to work on a much slower time scale, as with the experimental circuits of previous chapters.

This can be done by deliberately increasing the capacitance, C_L, that was introduced into the dynamic analysis of section 4.7. C_L is shown in Fig. 4.10 as the capacitance which is across Q_3 and Q_4 in Fig. 4.9. The equivalent capacitance to C_L in Fig. 4.15 is the capacitance from collector to emitter for $Q_{1'}$ and $Q_{2'}$. As things stand at the moment, this capacitance is only a few picofarads.

If C_L is made really large, say 470 pF, by connecting two capacitors across $Q_{1'}$ and $Q_{2'}$, in Fig. 4.15, from their collectors down to their common emitters, the most interesting dynamic behaviour will be observed that corresponds to the kind of behaviour, and the waveforms, published by Zojer *et al.* [11] for an advanced integrated circuit. The time scale of the experimental circuit is, of course, much slower.

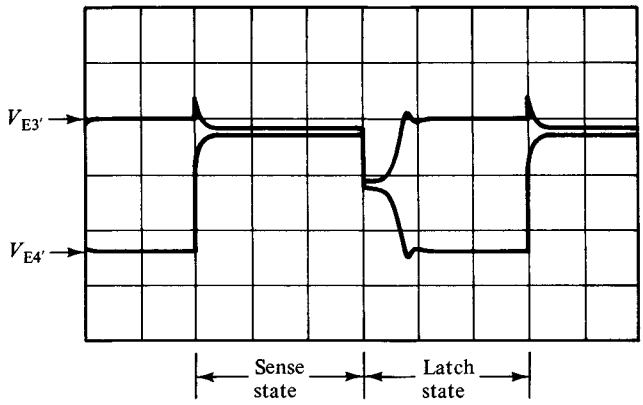

Fig. 4.16. *The waveforms observed at the emitters of* $Q_{3'}$ *and* $Q_{4'}$, *in Fig.* 4.15, *when there is a positive input voltage, and when both* $Q_{1'}$ *and* $Q_{2'}$ *have* 470 *pF capacitors connected from their collectors down to their common emitters. The display is a.c. coupled,* 50 *mV/div and* 1 *μs/div. The two waveforms are shown with their correct relative d.c. levels.*

Fig. 4.16 shows the waveforms which should be observed at the emitters of $Q_{3'}$ and $Q_{4'}$, in Fig. 4.15, when V_{in} is just above the critical threshold level, that is for a small positive value of V_{in}. The two waveforms have been adjusted to lie at the correct relative d.c. levels.

During the sense state, Fig. 4.16 shows that the emitters of $Q_{3'}$ and $Q_{4'}$ each have a small signal level on them, $V_{E4'}$ being slightly more negative, relative to $V_{E3'}$, because of the small positive input signal to Q_1 and Q_2. This difference in level between $V_{E4'}$ and $V_{E3'}$ has been exaggerated slightly in Fig. 4.16, for clarity, but the difference will be seen very clearly if V_{in} is increased to, say, +25 mV.

The latch state begins when the square wave input turns Q_4 on and Q_3 off. The first thing that happens is that the emitters of $Q_{3'}$ and $Q_{4'}$ both fall together by an amount $I_{L2}(R_3+R_4)/2$. This follows because half of the current in Q_4 now flows in (R_3+R_4) and the other half in (R_5+R_6). The drop is, therefore, about 50 mV.

The circuit is now regenerative, in the sense of equation (4.11) with $g_m R_L > 1$. The *difference* between the two voltages displayed in Fig. 4.16 now grows exponentially until the circuit leaves the simple linear regime, used in the analysis leading to equation (4.11), and takes on the levels determined by the state in which $Q_{1'}$ is on and $Q_{2'}$ is completely switched off.

4.14 The dynamic offset voltage

A very important point about the dynamics of this circuit should have been revealed by these experiments. When the two 470 pF capacitors were connected across $Q_{1'}$ and $Q_{2'}$, in Fig. 4.15, a large change in the offset voltage, the critical input level at which $V_{E3'}$, or $V_{E4'}$, changes from a large square wave to a small one, should have been observed. The offset voltage should now be quite large, and may be positive or negative. The reason for this is the tolerance on the two capacitors used, and this may be confirmed very easily by simply interchanging them: the large offset voltage will change sign. This observation is important because it explains why the offset voltage observed in the earlier static hysteresis measurements, the offset shown in Fig. 4.13, differs from the offset observed in the dynamic tests, described in section 4.13: the difference is due to the different stray capacitances associated with the layout of this discrete component circuit.

Why should a difference in the capacitance across $Q_{1'}$ and $Q_{2'}$, in Fig. 4.15, cause a change in d.c. offset voltage, which is surely due to the simple d.c. offset voltage of the input pair, Q_1 and Q_2? The answer to this may be seen in the waveforms shown in Fig. 4.16. At the beginning of the latch state, Q_4 turns on and the current in Q_4 should be shared equally by $Q_{1'}$ and $Q_{2'}$. That is why the collector voltages of both $Q_{1'}$ and $Q_{2'}$ should drop together, as shown in Fig. 4.16, and why the small difference between these two voltages, initially set by the signal input, should be maintained. Q_4 takes a finite time to turn on, however, and if the stray capacitances in parallel with $Q_{1'}$ and $Q_{2'}$ are not identical, these capacitances will charge up a small amount, during the finite turn-on time, but they will not charge up equally, even if the current in Q_4 is shared equally between them.

But this brings out a further question. Why should the current in Q_4 be shared equally between $Q_{1'}$ and $Q_{2'}$? For this to happen, $Q_{1'}$ and $Q_{2'}$ must not only have identical d.c. characteristics, they must also be identical dynamically. This calls for identical capacitance to be associated with the emitter and collector junctions of both transistors, which implies perfect symmetry in the layout of all parts of the circuit shown in Fig. 4.15 that are associated with $Q_{1'}$ and $Q_{2'}$. This is, of course, impossible with a discrete component circuit, but it is almost possible with the layout of an integrated circuit, although this may not be as easy as one might think. For example, it is obvious that the connections which must be made to the collectors of Q_1 and Q_2, the input sense amplifier, will involve crossovers which are asymmetric if the circuit is laid out as it is drawn in Fig. 4.15. If this is avoided by placing Q_1 and Q_2 in between R_4 and R_6, it is now the connections to the bases of Q_1 and Q_2 that will cause problems, to say

nothing of the connection to their emitters. When all these problems have been solved, the designer still has to deal with the layout of 255 such circuits, all on one die, and their associated logic, as shown in Fig. 4.2. It is, in fact, the problems associated with relative propagation delays [12], between various parts of such a large scale integrated circuit, that cause the greatest difficulty. Because the devices used are so fast, and the capacitances associated with individual devices are so small, the problem of unequal stray capacitance, which has been illustrated by the experimental circuit used here, is not the most difficult problem the designer has to solve.

4.15 Conclusions

This chapter began by considering the ADC problem in general and its importance in the fields of instrumentation, measurement, and communications. The comparator circuit was then isolated as a key circuit problem in ADC design, particularly for the flash ADC which is the fastest of all ADCs and the one used in the fastest digitizing oscilloscopes.

System considerations were then brought in to show how the idea for a new circuit shape could come from an understanding of what an entire system, of which the new circuit was to be only a minor, but essential, part, was intended to do. This led to a comparison between a simple operational amplifier kind of comparator and a comparator using positive feedback.

Positive feedback makes a comparator circuit have a critical input voltage, a threshold level, at which the output changes state. Positive feedback also introduces hysteresis into the transfer function of the comparator, which can be a very useful feature if it is properly controlled.

The idea of control led to a discussion of how the clock signal of the digital system would be used to control the transfer function of the comparator circuit so that this transfer function could take on quite distinct forms, the different forms that are required during different times in the data processing cycle. It is interesting to note that this idea, which led to the circuit shape shown in Fig. 4.11, did not appear until 1969 [9], and was not widely adopted until Peterson took it up in 1979 [4]. Digital systems using comparators have been around since the 1940s, however [2].

The experimental circuit for this chapter made it possible to measure the hysteresis boundaries of the circuit, under really static conditions, and to compare these measurements with theory. Hysteresis, in the fast comparator/latch circuit, has interesting implications when the circuit must handle signals that are changing very rapidly with time. This is very

important in systems which dispense with a true sample and hold circuit, the kind of circuit discussed in chapter 3, and make direct use of the comparator/latch to measure the input signal amplitude [12] at some instant in time.

Hysteresis is only one of the problems facing the circuit designer when the dynamics of the comparator/latch circuit are considered, and this chapter closed with a description of some dynamic experimental work that may be done by adding some more hardware to the first experimental circuit. There is much that may be done with this final circuit, Fig. 4.15, both with and without the additional capacitors that should be added in order to slow the circuit down so that it behaves in a fairly simple way. A very clear demonstration of the statistical nature of the circuit's response to d.c. signals very close to the threshold input voltage may be made, and it is also interesting to examine the circuit's response to a small sinusoidal input. Another possibility is to increase the values of R_4 and R_6 so that the circuit may be studied under conditions which allow $Q_{1'}$ and $Q_{2'}$ to saturate.

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