3
Sample and hold circuits

3.1 Introduction

In its simplest form [1], a sample and hold circuit has the circuit shape shown in Fig. 3.1. The signal input arrives through a 50 Ω co-axial line, to find a 50 Ω termination, and is then sampled periodically by means of the sampling gate. This gate is shown as a simple switch in Fig. 3.1.

The switch closes for a very short time, τ, short enough for it to be assumed that any change in the input signal over that time may be neglected. During this short time, the sampling capacitor, C_s, will begin to charge up towards the value that the input signal has at the instant of sampling. The time constant, T_{in}, associated with this charging process will be $25C_s$, because C_s will see a source impedance of 25 Ω when the switch is closed: the 50 Ω resistor in parallel with the 50 Ω input line.

When the switch is open, C_s is left providing an input to the voltage follower, A in Fig. 3.1. The output from the circuit is thus 'held' in between samples, provided the voltage follower can be made to have a high enough input impedance.

How the circuit actually behaves is mainly determined by the relative values of the input time constant, T_{in}, and the sampling time, τ. Three cases will be considered in the following three sections: $T_{in} \gg \tau$, $T_{in} \ll \tau$, and the particularly interesting case where C_s is replaced by an open circuited length of transmission line.

3.2 Performance when $T_{in} \gg \tau$

The sampling oscilloscope, the instrument discussed briefly in chapter 1, provides an example of a sample and hold circuit which operates with $T_{in} \gg \tau$. The signal input, in this case, is periodic and the time at which

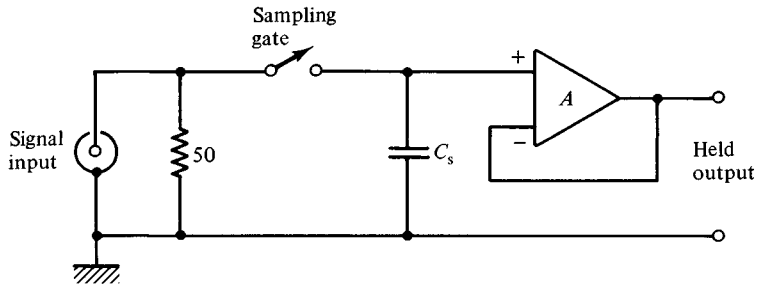

Fig. 3.1. *A sample and hold circuit.*

the sample is actually taken, t', is advanced, very slowly, step by step, so that the held output of the circuit shown in Fig. 3.1 is the integrated average of the input signal, $f(t)$, taken over time τ, that is

$$V_{\text{out}} = (1/\tau)\int_{t'}^{t'+\tau} f(t)\,\mathrm{d}t. \tag{3.1}$$

An estimate of the effective bandwidth of the sample and hold circuit can be made by setting $f(t) = A\sin(\omega t)$ in equation (3.1). Completing the integration gives

$$V_{\text{out}} = -(A/\omega\tau)\{\cos[\omega(t'+\tau)] - \cos(\omega t')\} \tag{3.2}$$

which may be simplified by using the well-known identity,

$$\cos(\alpha) - \cos(\beta) = 2\sin[(\alpha+\beta)/2]\sin[(\beta-\alpha)/2] \tag{3.3}$$

to give,

$$V_{\text{out}} = (2A/\omega\tau)\sin[\omega(t'+\tau/2)]\sin(\omega\tau/2). \tag{3.4}$$

Equation (3.4) shows that V_{out} is, as expected, a sine wave with the same frequency, ω, as the input sine wave, but transformed to the much slower time scale, t'. What is of primary interest, however, is the amplitude of this V_{out}. This amplitude is not A but, from equation (3.4),

$$|V_{\text{out}}| = (A/\pi f\tau)\sin(\pi f\tau) \tag{3.5}$$

where $f = \omega/2\pi$ has been substituted for convenience.

Equation (3.5) shows that the sample and hold circuit, shown in Fig. 3.1, has the frequency response shown in Fig. 3.2, when it is operating with $T_{\text{in}} \gg \tau$, and t' is changing very slowly. There will be an opportunity, later in this chapter, to check this experimentally. Fig. 3.2 has been drawn for the case where $\tau = 1$ ns. As would be expected, there is no response at all to a sinusoidal input which has a period equal to the sampling pulse width: the integral given as equation (3.1) is then zero. Similarly, there is no output for sinusoidal inputs having period τ/n, where n is any integer.

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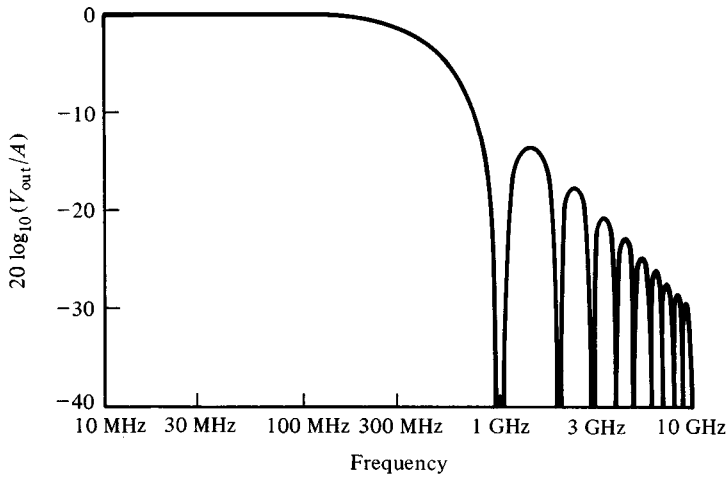

Fig. 3.2. *The response of the sample and hold circuit to sinusoidal inputs when* $T_{in} \gg \tau$, *the sampling time is advancing very slowly, and the sampling width,* τ, *is* 1 *ns.*

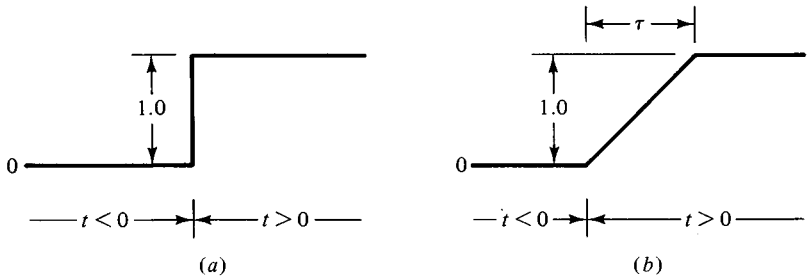

Fig. 3.3. *A Heaviside unit step function,* (*a*), *produces the output shown as* (*b*) *on the display of the sampling oscilloscope.*

As $[\sin(x)]/x = 0.707$ when $x = 1.39$, it is often stated [2] that the 3 db bandwidth of a sampling oscilloscope is, from equation (3.5)

$$B = 1.39/\pi\tau = 0.442/\tau \tag{3.6}$$

which would mean that a sampling pulse width of 1 ns would give a bandwidth of 442 MHz, as shown in Fig. 3.2. This can be a misleading point of view, however, because the frequency response shown in Fig. 3.2 does not belong to the simple world of linear network analysis, where everything has a slope of zero, 6 db/octave, 12 db/octave, and so on.

Just how different the sampling oscilloscope is, can be seen by considering equation (3.1) for another simple input function: the unit step function shown in Fig. 3.3(*a*). In this case the integration of equation (3.1) is so simple that it may be seen at once that the sampling oscilloscope

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display will be as shown in Fig. 3.3(*b*), where *attributed* time, t, has been used.

The result is that a perfect step input to the sampling oscilloscope is displayed as a linear rise, from zero to unity, duration τ. It might then be argued that the rise time, τ_r, of the sampling oscilloscope, taken from the 10% to the 90% points, is 0.8τ. Now using the often quoted [3] idea that bandwidth, B, and rise time, τ_r, are related by,

$$B = 0.35/\tau_r \tag{3.7}$$

for a well-designed direct coupled amplifier, it would seem to follow that the bandwidth of a sampling oscilloscope is given by,

$$B = 0.35/0.8\tau = 0.468/\tau \tag{3.8}$$

which is not all that different from equation (3.6). However, no linear amplifier can have a step response of the kind shown in Fig. 3.3(*b*), anymore than it can have a frequency response of the kind shown in Fig. 3.2. These are results which are specific to sampled data systems.

3.3 Performance when $T_{in} \ll \tau$

When the time constant, T_{in}, formed by the sampling capacitor, C_s, and the signal source impedance, in Fig. 3.1, is very much shorter than the sampling pulse width, τ, C_s has time to charge up to the signal level, always provided that the signal input frequency is well below $1/2\pi T_{in}$.

Operating with $T_{in} \ll \tau$ is the mode used in the sample and hold circuit at the input of a digitising oscilloscope. The input signal may now change dramatically from sample to sample, and the sample and hold circuit will still follow. In fact, the circuit is really operating in the track and hold mode, which, as Naegeli and Grau argue [4], has better noise and distortion performance than the sample and hold mode.

The frequency response of the circuit shown in Fig. 3.1, when $T_{in} \ll \tau$, is no longer that shown in Fig. 3.2, but a simple flat response out to a -3 db point at $f = 1/2\pi T_{in}$, followed by a -6 db/octave slope. Again, the experimental circuit, described towards the end of this chapter, will give an opportunity to demonstrate this.

In the digitising oscilloscope, the sample and hold circuit is not followed by a deflection amplifier of modest bandwidth, as it is in the sampling oscilloscope, but by a very fast ADC which must digitise the sample in, what may be, the very short time between samples. These very fast ADC circuits will be discussed in chapter 4.

When a very wide bandwidth is called for in a digitising oscilloscope, it

is necessary to make the sampling pulse width, τ, very small indeed. To then make $T_{in} \ll \tau$ may be quite impossible if a simple capacitor is to be used in the circuit, as shown in Fig. 3.1. A very interesting way of getting around this problem is described in the next section.

3.4 An open circuit transmission line for C_s

Rush and Oldfield [5] have described a sample and hold circuit in which a length of transmission line, with both ends open circuited, is used in place of the capacitor, C_s, shown in Fig. 3.1.

Fig. 3.4 shows the essential details of this circuit. When the sampling gate, the simple switch shown in Fig. 3.4, closes, the signal is presented with a 25 Ω load. This is a perfect match to the signal source impedance, which is made up from the 50 Ω termination, shown in Fig. 3.4, in parallel with the 50 Ω cable that would be connected to the signal input socket.

It follows that, for the very first sample, a voltage equal to one half of the signal input will be developed across the input end of the 25 Ω line, shown in Fig. 3.4. This voltage step will propagate along the 25 Ω line, be reflected without change of sign at the open circuit, and return to the input end, charging the line up to the full signal voltage as it does so. If the switch in Fig. 3.4 is then opened, at exactly the instant that this reflection reaches the input end of the 25 Ω line, the line will be left charged to exactly the level of the signal input.

Subsequent samples will increase, or decrease, the voltage level held in the 25 Ω line by just the amount that the signal input changes between samples. This, of course, is only true when the variation in the signal level during the sampling time, τ, may be ignored.

The above argument implies that the sampling pulse width must be made exactly equal to the time taken for a signal to travel a distance $2L$ in the 25 Ω line, that is $\tau = 2L/v_p$. This is the same relationship that applied for the pulse generator circuits, Figs. 2.2(*b*), 2.9 and 2.11, discussed in the previous chapter. The pulse generator and sampling gate circuits now involve very similar transmission lines, and may be built together as one hybrid circuit. This is clear from the interesting photographs in Toeppen's paper [6] where both transmission lines can be seen in the hybrid circuit, these being only a few millimetres in length because a sampling pulse width of only 100 ps is being used in this case.

What kind of frequency response does the sample and hold circuit shown in Fig. 3.4 have? The answer to this question may be seen by considering a sinusoidal signal input with a period exactly equal to τ, and thus also equal to $2L/v_p$. This means that the 25 Ω line is one half

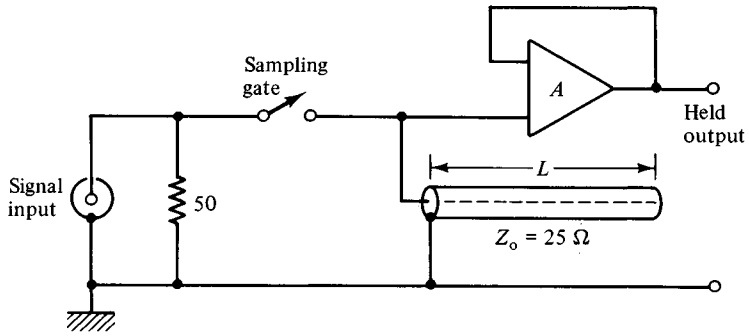

Fig. 3.4. A sample and hold circuit using a length of open circuited line instead of a sampling capacitor.

wavelength long. No matter at what points on the sinusoidal input signal the sampling gate closed and opened, the result would always be the same: the 25 Ω line behaves as a high Q parallel resonant circuit and there would be no constant voltage level component to act as an input signal for the low frequency voltage follower amplifier, A in Fig. 3.4. This means that the circuit of Fig. 3.4 has a frequency response of the same form as that shown in Fig. 3.2. The effective bandwidth will be of the order of that given by equation (3.6), that is $0.442/\tau$. However, there is a very important improvement in the performance in that the restriction on the change in input signal level from sample to sample, which was required in order to obtain equation (3.6), no longer applies for the new circuit, Fig. 3.4. No matter how great the change in signal input, the 25 Ω line shown in Fig. 3.4 will be left charged up to the correct level. The problem now is to digitise this analog information before it changes again, but that is the problem considered in the next chapter. This chapter continues with a look at the hardware realisation of sample and hold circuits.

3.5 The realisation of a sampling gate

So far, the sampling gate has been shown, in Figs. 3.1 and 3.4, as a simple switch. In practice, a very fast electronic switch is needed, and one which can be operated by the sampling pulse.

As an example, consider the idea of using a single n-channel enhancement MOST as a sampling gate. This idea is shown in Fig. 3.5. Three obvious problems can be seen at once.

1 The resistance of the device, when it is on, should be negligible compared to the signal source impedance, which in this case is 25 Ω. No fast MOST will satisfy this condition.

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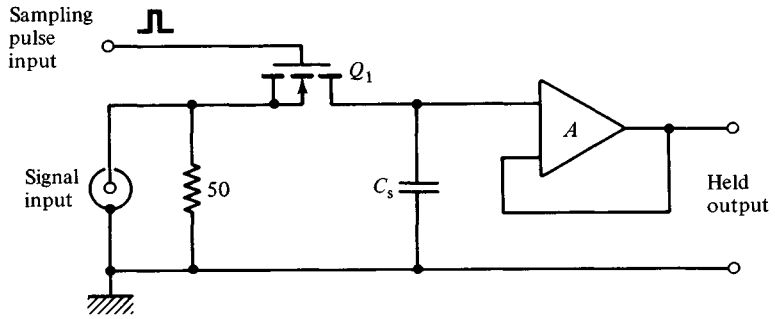

Fig. 3.5. *A single MOST does not make a good sampling gate.*

2 The impedance of the device must be very high indeed when it is off, particularly when C_s is small. An MOST will have a finite drain to source capacitance.
3 There will be considerable breakthrough of the sampling pulse into the signal input circuit, and across C_s, because of the finite gate to source and gate to drain capacitances.

These three problems are the main concern with all very high frequency sampling gate circuits. A review by Akers and Vilar [7] suggests that fast response diodes may be the most useful devices, at present, for the realisation of sampling gates, because these can have a very low on-resistance, very high off-impedance, and several matched diodes may be arranged in various configurations to provide good isolation between sampling pulse input and signal input. For this reason, the remainder of this chapter will concentrate upon these sampling gate circuits which use diodes, but it must always be borne in mind that this is only a fraction of a large and rapidly developing field in electronic circuit design. Among the many devices reviewed by Akers and Vilar [7], an obviously strong candidate for the future is the opto-electronically controlled switch. This idea comes from some early work by Auston [8], using the photo-conductivity of silicon. Indium phosphide opto-electronic switches have been used as sampling gates, at picosecond speeds, for the direct digital processing of radar signals [9].

3.6 Diode sampling gates

In the previous section, low on-resistance was listed as the first requirement for a sampling gate device. The solid state diode has good possibilities from this point of view, because it has a small signal resistance

$$\mathrm{d}V_F/\mathrm{d}I_F = (kT/e)/I_F \tag{3.9}$$

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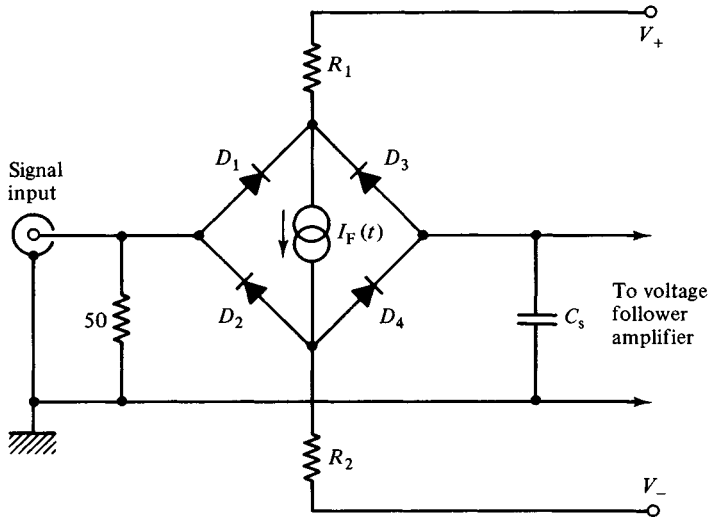

Fig. 3.6. A balanced diode bridge sampling gate. This should show negligible breakthrough of the sampling pulse, $I_F(t)$, into the signal circuit.

when it is forward biassed with a current I_F. As kT/e is 25 mV at room temperature, this means that a forward resistance of a few ohms may be obtained with a forward current of only a few milliamps.

The diode impedance can be very high when the diode is reverse biassed, so the second point listed in the previous section is also well satisfied.

It is the third point which influences the circuit shape of diode sampling gates more than anything else: the isolation which is needed between the sampling pulse input to the gate and the low level signal circuit.

Fig. 3.6 shows a first suggestion for a diode sampling gate. This uses four diodes connected in a bridge arrangement. The diodes are normally all reverse biassed by the connection to positive and negative supplies *via* R_1 and R_2, which are both made high and equal in value. This is the state when the sampling gate is off and the isolation between the signal input and the sampling capacitor, C_s, is provided by the high impedance and small capacitance of the reverse biassed diodes.

The gate is turned on by means of a sampling current pulse, $I_F(t)$. Because of the symmetrical bridge connection of the four diodes, this current is contained within the diode bridge, except for a small fraction which must flow in the resistors R_1 and R_2, and there should be no fraction of $I_F(t)$ flowing into C_s or into the signal input circuit. To obtain this result, excellent matching must be achieved between the four diodes. The

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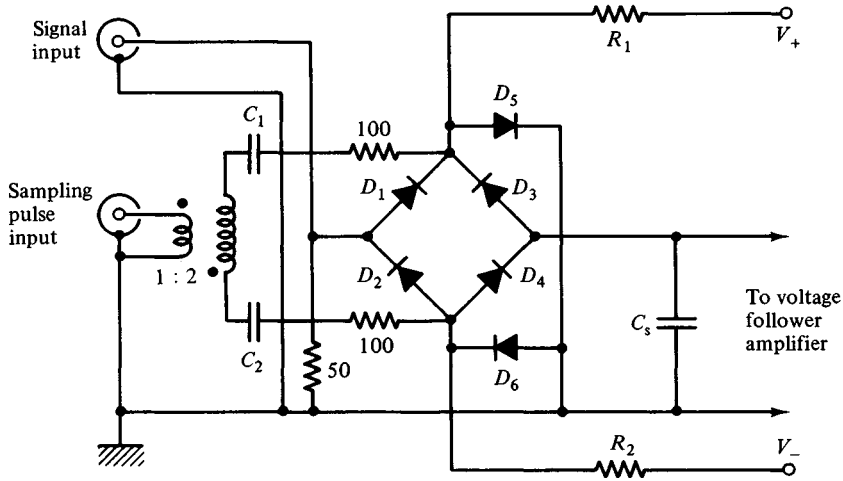

Fig. 3.7. A balanced series/shunt gate using six diodes. Some details are now shown for the sampling pulse input to this circuit.

stray capacitances associated with top and bottom nodes of the diode bridge, as it is shown in Fig. 3.6, must also be matched as closely as possible.

3.7 A series/shunt gate

A considerable improvement in the performance of the gate shown in Fig. 3.6 is obtained if two more diodes are added. These are shown in Fig. 3.7 as D_5 and D_6. The aim is to improve the isolation between the signal input and the sampling capacitor, C_s, when the gate is off. This is done by having D_5 and D_6 forward biassed when the gate is off, so that they present a very low impedance at the upper and lower nodes of the diode bridge, which previously had only high impedances, R_1 and R_2, connected to them. In Fig. 3.7, the signal input is now isolated from the sampling capacitor by the large attenuation that is effected through the very high impedances of D_1 and D_2, followed by the very low impedances of D_5 and D_6.

But the addition of D_5 and D_6 has the further advantage of clamping the upper and lower nodes of the diode bridge to approximately ± 0.7 V, in the case of silicon diodes, so that R_1 and R_2 can now be made really high values without involving large voltage excursions across the diodes themselves. The first task of the sampling pulse input is to turn D_5 and D_6 off, forcing the upper and lower nodes of the diode bridge to go from the ± 0.7 V state to the ∓ 0.7 V state, where D_1, D_2, D_3, D_4 are all on.

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3.8 Connecting the sampling pulse generator

Fig. 3.7 also begins to show some details of the way in which the sampling pulse generator might be connected to the sampling gate. Ideally, a balanced, and truly floating, pulsed current source is needed, as shown in Fig. 3.6. This was discussed briefly in the last section of chapter 2, where Fig. 2.11 was presented as a circuit shape for such a balanced sampling pulse generator.

Experimentally, it is most convenient if a simple sampling pulse generator may be used, and this will have an unbalanced 50 Ω co-axial output. This is true of any simple laboratory pulse generator, and also true of the experimental circuit described in the previous chapter: Fig. 2.9.

To use such an unbalanced pulse source as a sampling pulse generator for the balanced diode gate, a pulse transformer has been used in Fig. 3.7, which transfers the pulse from the 50 Ω co-axial system into a balanced 200 Ω transmission line system. Use is then made of the very low forward resistance of the diodes, when compared to the higher impedance of the balanced transmission line system, to make a fair approximation to a current source for switching the diodes on and off.

Such a balanced to unbalanced transformer is usually termed a 'balun'. This is not a simple transformer but a very wide bandwidth, high frequency device, and its construction will be dealt with in the next section. In circuit representation, however, a balun is usually shown by the normal transformer symbol.

A transformation ratio of 1:2 is the most simple one to obtain, and this means an impedance ratio of 1:4, so that the secondary of the balun shown in Fig. 3.7 is terminated with 200 Ω. This is done using two separate 100 Ω resistors so that there is a balance in the unavoidable stray capacitance to ground.

It is very important to understand the reason for the capacitors C_1 and C_2 in Fig. 3.7. These are essential because there can be no d.c. level across the secondary of a transformer. The fact that some balun designs are isolating transformers, like the one symbolised in Fig. 3.7, and others involve a d.c. path between primary and secondary, has nothing at all to do with this point. C_1 and C_2 are needed because D_5 and D_6 clamp the upper and lower nodes of the diode bridge at ± 0.7 V for most of the time. Just how much of the time depends upon the mark to space ratio of the sampling pulse generator. C_1 and C_2 charge up to accommodate this change in mean d.c. level between the secondary of the balun and the upper and lower nodes of the diode bridge. Two capacitors are used for the same reason, discussed above, that two 100 Ω resistors are used

instead of a single 200 Ω one. These capacitors would be made quite large, and, of course, equal, so that the time constant, $100\,\Omega \times C_1$, would be greater than the longest time expected between samples.

3.9 A design for a balun

The first step towards the construction of an experimental diode sampling gate circuit is to construct the balun that will be needed between this circuit and the sampling pulse generator. This balun will be a pulse transformer, that is a device with a very wide bandwidth, and must be constructed from transmission line.

As an introduction to this method of pulse transformer construction it is useful to consider the simple inverting pulse transformer that consists of a length of co-axial transmission line wound upon a ferrite toroid. At one end of this line, the outer sheath is grounded and the inner conductor is connected to the pulse source, in the usual way. At the other end of the line, because of the large inductance of the winding, which is common to both inner and outer conductors, the connections may be *reversed*: the inner conductor may be grounded while the outer conductor used as the source of a pulse, identical to the input pulse but of opposite sign. This kind of transformer has been known for a very long time [10].

The simplest way to make a balun transmission line transformer is to take two of the inverting transformers, that have been described above, and connect their inputs in parallel on one side and in series on the other. For example, 100 Ω co-axial cable could be used to provide a 50 Ω to 200 Ω balun transformer of this kind. Using 100 Ω twisted pair, or balanced line, would be even better. This method of constructing a balun may have been first described by Talkin and Cuneo in 1957 [11] and a paper [12] has reviewed developments in technique, although it does not mention an important contribution by Hilberg [13], who deals with the problems that can arise when transformers are made to operate in both the transmission line mode and the conventional coil mode, simultaneously.

The balun transformer which is recommended for the experimental circuit of this chapter, is shown in Fig. 3.8. This uses four of the inverting transformers that were described above, using four equal lengths of 50 Ω twisted pair transmission line wound on four ferrite toroids. For simplicity, only a single turn, and a single twist, are shown on each toroid in Fig. 3.8. In practice, 500 mm of twisted pair line is used on each core, these being 25 mm diameter, high permeability, high frequency, ferrite [14]. The winding is widely spaced. A 50 Ω twisted pair line is easily made

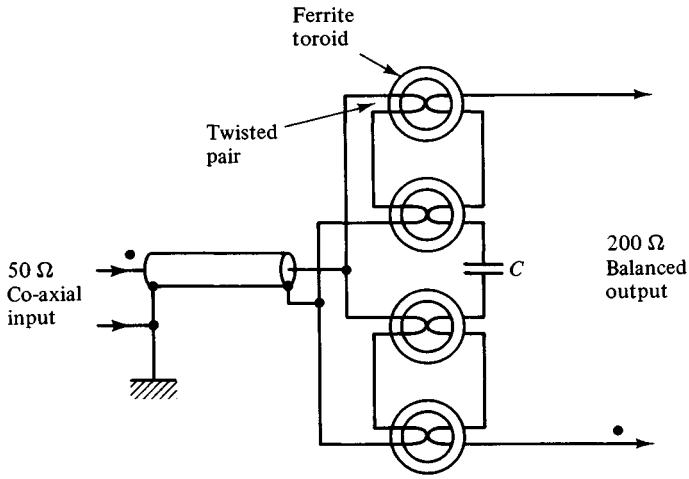

Fig. 3.8. One possible way of realising the balun, shown in Fig. 3.7, using four ferrite toroids and four lengths of 50 Ω line made from twisted pairs. Capacitors C_1 and C_2, in Fig. 3.7, are now replaced by a single one, C.

from two 0.4 mm polyurethane coated wires, twisted to a 5 mm pitch. As Fig. 3.8 shows, the four 50 Ω lines are connected in series/parallel on the 50 Ω side, to give a 50 Ω input impedance, while they are all four connected in series, on the output side, to give the 200 Ω balanced output. This configuration has a very great advantage over the simpler one, using just two 100 Ω lines, in that the balun shown in Fig. 3.8 is an isolating transformer: there is no d.c. path between input and output.

A more expensive way of making the balun shown in Fig. 3.8, that certainly gives better very high frequency performance, is to use four lengths of miniature 50 Ω co-axial cable, instead of the twisted pairs, and thread ferrite beads on each length [15]. This gives a linear layout to the balun and reduces the shunt capacitance that must be associated with the toroidal windings of the previous version.

3.10 An experimental sample and hold circuit

The experimental circuit for this chapter is shown in Fig. 3.9. This uses the six diode configuration, previously shown in Fig. 3.7. The CA3019 device is used for this: an array of six diodes, in monolithic silicon, in which four diodes are internally connected as a bridge, and the other two are left free. The diodes are numbered in Fig. 3.9 so that they correspond to the data sheet numbering [16]. The sampling pulse input comes directly from the

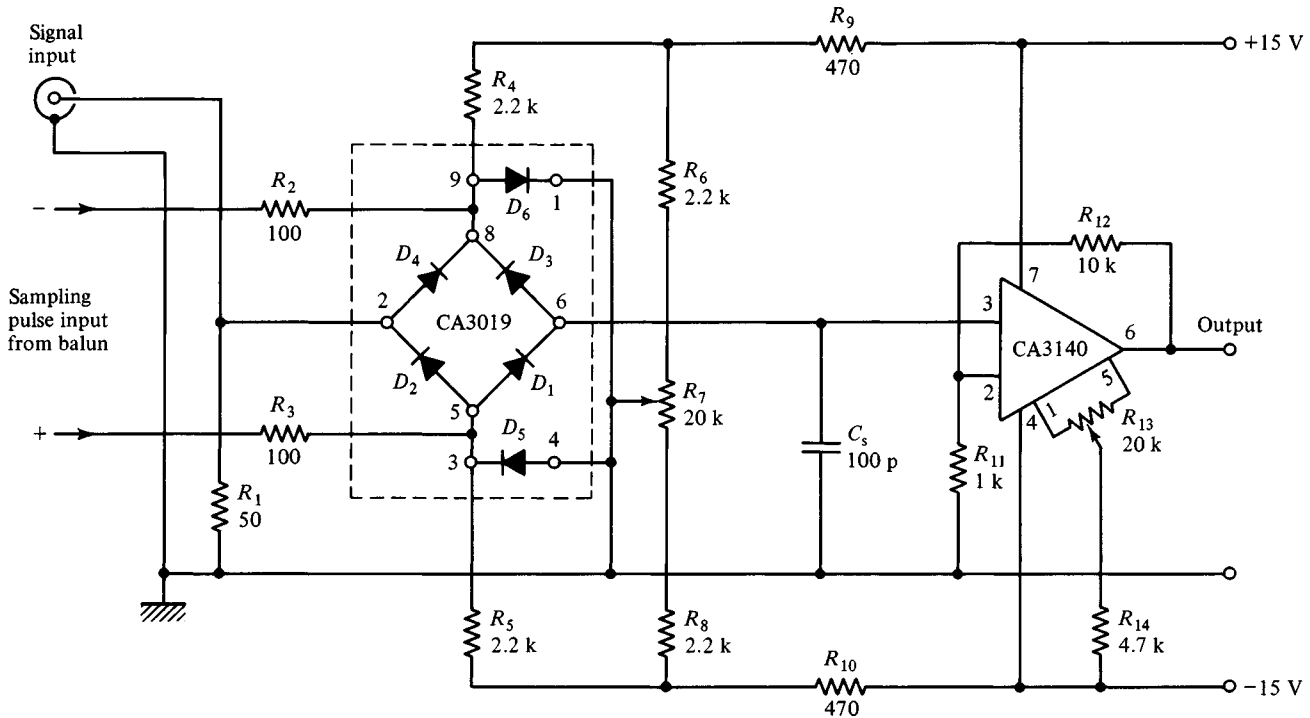

Fig. 3.9. The experimental sample and hold circuit. Note that pin 7 of the CA3019 must be connected to −7.5 V and, as with pins 4 and 7 on the CA3140, decoupled to ground.

200 Ω balanced output of the balun, shown in Fig. 3.8. The capacitor C, shown in Fig. 3.8, should be a ceramic 0.33 μF, 50 V, or a larger value if this is available in a small size with low inductance.

The amplifier which is needed to produce a useful output from the voltage that is held on the sampling capacitor, C_s, is provided by the CA3140 in Fig. 3.9. This is connected to have a gain of 11 by means of the feedback network R_{12} into R_{11}. The CA3140 is a very well-established operational amplifier [17] that has MOS input transistors, and thus draws negligible current from the small capacitor, C_s. Attention must be given to the layout of the circuit board around the top end of C_s, and all the connections to this, to ensure that there is negligible leakage current from any source into this sensitive area. This point can be easily checked, when the circuit is operating, by removing the sampling pulse input to the primary of the balun and watching how rapidly the d.c. level, at the output of the CA3140, drifts away from the zero level previously set by the nulling operation. Even when C_s is as small as 100 pF, this drift, which can be positive or negative, should be only of the order of ± 1 V/s.

3.11 Experimental work

Because the MOS input devices in the CA3140 cause this to have a fairly large input offset voltage, it is necessary to null the output of the circuit shown in Fig. 3.9, with C_s temporarily short circuited, before starting work. This is done by adjusting R_{13}.

A sampling pulse of +4 V amplitude, at least 10 kHz repetition rate, and between 20 ns and 100 ns duration, should then be supplied to the input side of the balun, shown in Fig. 3.8. This pulse may be provided by the experimental circuit of the previous chapter, Fig. 2.9, or from a laboratory pulse generator. The short circuit should be removed from C_s and a 50 Ω termination connected to the signal input socket, shown in Fig. 3.9.

First, view the d.c. level at the output with an oscilloscope. This will no longer be zero, as it was after the null was effected with R_{13}, but offset by some small amount which will be found to depend upon the sampling pulse width. The reason for this is the unbalanced dynamic behaviour of the diodes. Even if all six diodes were perfectly matched from a d.c. point of view, the stray capacitance, intrinsic to their monolithic structure, is unbalanced, and the switching characteristics must differ. This means that a small amount of charge will be transferred into or out of C_s during the rise time of the sampling pulse. The opposite occurs during the fall time. It is impossible for these two dynamic events to cancel one another out,

and a small positive or negative charge will be transferred to C_s even when the signal input is zero. This can be corrected by a very small adjustment of the forward bias on D_6 and D_5, and thus the reverse bias on the other four diodes. This adjustment is made by means of R_7, for each particular value of sampling pulse width.

Why does the sampling pulse width influence the output offset corresponding to zero input signal? The answer to this may be found by observing how the various ground connections and lengths of cable used in the experiment influence this offset. The rising edge of the sampling pulse, and the falling edge, set up disturbances that persist for some microseconds as they are reflected and transmitted around the various transmission paths within the system. Changing the relative time position of these two events, rise and fall, by changing the pulse width, changes the way in which these spurious signals interfere with one another, and this, in turn, must have a slight effect upon the way in which the diode gate turns off at the end of the sampling pulse. These problems do not, of course, arise in the final form of a manufactured digitising or sampling oscilloscope, because the sampling pulse width is fixed, and so are the relative positions of the various parts of the system.

3.12 Measuring the frequency response

Once the experimental circuit has been nulled correctly under zero signal input conditions, the input termination may be replaced with a simple radio frequency signal generator, and the behaviour of the sample and hold circuit checked for a sine wave input.

At present, the value of C_s is 100 pF, so that T_{in} is 2.5 ns: very much smaller than the sampling pulse width, which will be around 50 ns. This means that the circuit is operating in the $T_{in} \ll \tau$ regime, discussed in section 3.3, and should have a frequency response out to $1/(2\pi \times 2.5 \times 10^{-9})$ Hz, or 63.6 MHz. This can be checked using very simple equipment, because the actual output from the CA3140, in Fig. 3.9, is of very limited bandwidth: only about 300 kHz. If a simple analog oscilloscope is connected to the output of the CA3140, and its timebase is triggered at the repetition rate of the sampling pulse generator, which is around 10 kHz, the envelope of the sampled data will be observed on the analog oscilloscope, and this will, in fact, look like a sine wave whenever the input frequency is close to a harmonic of 10 kHz. Naturally, it is not easy to hold the frequency of a simple signal generator close to, for example, exactly 300×10 kHz, or 30 MHz. The repetition rate of the pulse generator will also be subject to drift. In practice a sinusoidal

looking output will be observed only every now and again, as the input frequency is varied, but the *envelope*, or *amplitude*, of this sampled output may easily be measured so that the bandwidth of 63.6 MHz can be checked. The value of C_s may then be changed to 200 pF, or 50 pF, and the check repeated.

The other important point to check is the overall gain of this sample and hold system, and its noise level. An RF input of 10 mV peak to peak should give an output with an envelope of 110 mV peak to peak, because there should be negligible loss across the diode gate followed by a gain of 11 in the CA3140. It is this overall gain of 11 that should drop by 3 db at 63.6 MHz.

The noise level at the output of the CA3140 depends very much upon the laboratory environment: this is a very wide bandwidth system of high sensitivity, and is laid out in a rather open way. However, on a timebase of, say, 1 ms/div., the noise should appear to be only a few millivolts. The breakthrough of the sampling pulse is discussed in section 3.13.

It is now interesting to examine the other mode of behaviour that was discussed in section 3.2: the case when $T_{in} \gg \tau$. To do this the value of C_s is simply increased several orders of magnitude. For example, making $C_s = 10$ nF will increase T_{in} to 250 ns. Working with a sampling pulse of 50 ns, a frequency response like the one shown in Fig. 3.2 should be obtained with the experimental circuit, but the first null in the response should be at 20 MHz and, from equation (3.6), the 3 db bandwidth should be at 8.84 MHz.

When this is checked, using the same technique that was described at the beginning of this section, something, perhaps, unexpected will be observed. Although the frequency response will be found to follow the interesting form shown in Fig. 3.2, and the complicated periodic responses and nulls out to the higher frequencies will be clearly observed, the entire response will appear to show a rapidly fluctuating overall gain as the input frequency is increased slowly over the expected pass bands.

This behaviour is a demonstration of the constraint that was put upon the rate at which t', the sampling time, could change when equation (3.1) was used to derive equation (3.4). The behaviour shown in Fig. 3.2 will only be found in the experimental circuit when the signal input frequency is very close indeed to a harmonic of the sampling pulse generator repetition rate. The experimental circuit is then behaving in exactly the same mode as a classical sampling oscilloscope: the sampled output is equivalent to a stroboscopic view of the high frequency input.

Finally, it is interesting to attempt to model the idea of using an open circuited length of transmission line for C_s. This idea was discussed above

in section 3.4. The 25 Ω line which is needed is easily made by using two 50 Ω co-axial cables in parallel, with both inner conductors connected to pin 3 of the CA3140, in Fig. 3.9, and both outer conductors taken to ground. C_s is, of course, removed entirely. For a 50 ns sampling pulse, the two lines will have to be about 5 m in length. The same frequency response seen in the previous test, with $C_s = 10$ nF, should then be observed but, this time, the restriction on the rate of change of t', and the rapid fluctuations in overall gain, observed previously as the input frequency was changed, should disappear.

3.13 Dynamic range

Up to now, all the tests on the experimental sample and hold circuit have been made with an RF input of only a few millivolts. Looking at Fig. 3.9, it is clear that there must be some upper limit to the signal input level because once this begins to approach the forward drop across any of the diodes the gate can no longer be operating in a simple way.

It is useful to combine a test of the d.c. input level handling capabilities of the circuit with an observation of the breakthrough of the sampling pulse into the input circuit and the output circuit. To do this, a simple analog oscilloscope should be used to view the d.c. level at both the input and the output of the circuit shown in Fig. 3.9, and the timebase of this oscilloscope triggered from the trigger output of the pulse generator being used to provide the sampling pulse. If the timebase speed is then set to, say, 1 μs/div, the breakthrough of the sampling pulse into the input circuit, and at the output of the CA3140, will be seen as spikes. These spikes should be only about 100 mV on either channel, and are, of course, a distortion of the sampling pulse by the limited bandwidth of the oscilloscope, and the CA3140. Nevertheless, a relative measure of the sampling pulse breakthrough, and how it changes, can be made.

A d.c. level may now be established at the input by connecting the input termination to a variable voltage power supply, say ±30 V *via* a 500 Ω resistor. This should make an input voltage of up to ±1.5 V possible. As the d.c. input is increased, the output should also increase, 11 times faster because of the gain of the CA3140, and the sampling pulse breakthrough will change because the balance of the diode bridge is being spoilt as the input voltage level departs from zero. Apart from this, the gate will appear to continue working until the input level reaches two forward diode voltages in magnitude, that is 1.2 V or more. Real confirmation that the gate is still turning off properly may be obtained by disconnecting the sampling pulse and checking that the output level of the CA3140 still

drifts slowly, one way or the other, despite the high d.c. level at the gate input. Note that this result means that a larger dynamic range may be obtained by using gallium arsenide diodes [18], while Schottky barrier diodes give less dynamic range than silicon.

3.14 Conclusions

After a general discussion of sampling gates and the kind of overall frequency response that can be expected from sampling systems, this chapter took the six diode series/shunt gate as an experimental project for circuit design work.

This involved a short digression, in section 3.9, to consider the construction of the balun that was needed to connect the sampling pulse generator to the diode gate. In a real digitising oscilloscope, this balun would not be needed because the combination of sampling pulse generator and sampling gate becomes one single hybrid circuit. However, it is much easier to observe what is really happening, and to vary the circuit parameters experimentally, when the system is split up into convenient parts and connected up with co-axial cable. The earth-loop problems and matching problems that then come up all add to the interest and value of the experimental work.

Another radical difference between the experimental circuit described here, Fig. 3.9, and a real digitising oscilloscope, is the use of a much longer sampling pulse. This is essential if experimental work is to be done using fairly simple methods of construction and test equipment. The system described here is a scaled-up version of the real thing: lengths of transmission line are several metres in length, instead of several millimetres. The principles involved are just the same, however.

The message coming from the experimental work of this chapter should be about *time*. The experimental circuit accepts signals with frequencies approaching 100 MHz at its input, and then reproduces these signals, accurately, on a much slower time scale. Once the sampling gate has been passed, the hardware involved is all low frequency: a simple operational amplifier and a general purpose laboratory oscilloscope.

The same message is found inside the case of a digitising oscilloscope. The input circuits belong to the world of microwave electronics and occupy, perhaps, 5% of the volume. There is then a very fast ADC, the subject of the next chapter. After that, all the electronics is rather slow and very cheap: digital data processing, memory and display.

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