6
Wide-band amplifier circuits

6.1 Introduction

Wide-band amplifier circuit design is one of the most difficult and varied areas in the whole subject of electronic circuit design. There are the wide-band intermediate frequency amplifiers associated with radio, television and radar receivers, there are the wide-band pulse amplifiers of radar and nuclear instrumentation systems, there are the direct-coupled wide-band amplifiers found in oscilloscopes, and many other electronic systems, and there are the wide-band repeater amplifiers found in cable communication systems.

A number of excellent texts consider many of the areas listed above. Maclean's book [1] deals mainly with the repeater kind of amplifier, and is particularly strong on the computer aided optimisation of a design for the best noise performance and low sensitivity to component tolerance. Kovács' book [2] covers a much wider field and attempts to answer the question which will be central to this chapter: how is the first step in design, the choice of the *circuit shape*, the initial circuit idea, to be made? This is, perhaps, in contrast to Carson's well-known book [3], which contains no practical circuits but is excellent on theory.

This chapter will concentrate on one small area in the field of wide-band amplifier circuit design: wide-band direct-coupled amplifiers. These are needed for the deflection amplifiers of the conventional analog oscilloscope and, of course, for the digitising oscilloscope when this kind of instrument is to be designed for use with very low level signals. In both cases, the input stages of the deflection amplifier call for high input impedance, wide bandwidth and well-defined gain.

The output stage of an analog oscilloscope deflection amplifier is also of particular interest, when the CRT is of the conventional kind, because

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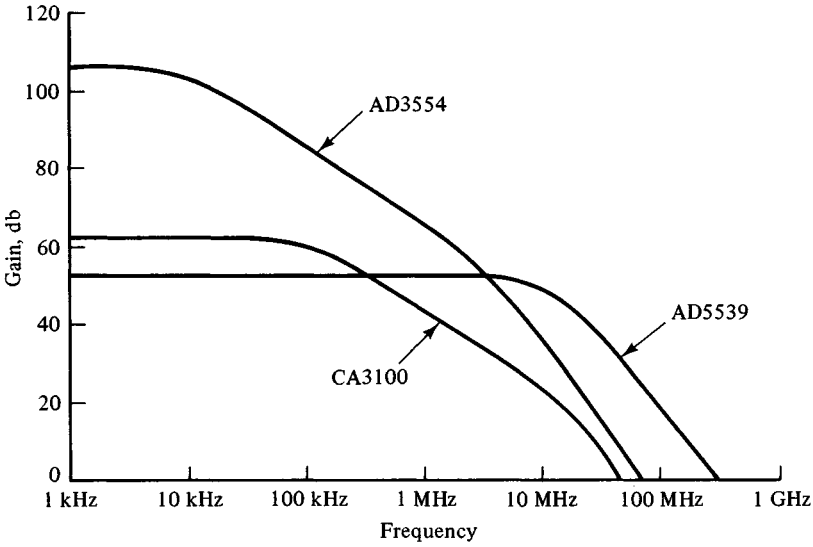

Fig. 6.1. *The open-loop gain characteristics of three wide-band operational amplifiers: the hybrid AD*3554, *the monolithic BiMOS CA*3100, *and the pure npn monolithic AD*5539.

the load will be a pure capacitance which must be driven at high frequency and at quite high voltage. The output stage problem is considered at the end of this chapter.

6.2 Direct-coupled amplifiers

A direct-coupled amplifier, or d-c amplifier, is one which has a constant gain from zero frequency up to some high frequency at which the gain begins to fall. This is illustrated in Fig. 6.1 where the open loop gain characteristics of three well-known wide-band operational amplifiers are shown [4]. The contrast between these amplifiers and the more common kind of internally compensated operational amplifier, which has a constant gain only up to about 10 Hz, should be noted.

Wide-band d-c amplifiers are a relatively recent kind of circuit in electronics. The first analog oscilloscopes used amplifiers with *RC* coupling, and could therefore only display time varying signals. There was no possibility of using the oscilloscope to display relative d.c. levels in a circuit. These early oscilloscopes used several stages of amplification, without any negative feedback, and had inductive loads for the active devices in order to compensate for the fall off in gain at high frequencies [5]. The first video amplifiers of early television followed the same lines.

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6.3 Wide-band d-c amplifiers for oscilloscopes

The simplest analog oscilloscope must have a bandwidth of well over 10 MHz if it is to be of any use to the electronic engineer of today. The sensitivity of the instrument should be such that signals of a few millivolts are sufficient to give a vertical deflection of about one screen diameter. This will call for an overall gain of at least 80 db.

It is thus clear that the operational amplifiers which have the kind of open-loop gain characteristics shown in Fig. 6.1 are not going to be the building blocks of a modern analog oscilloscope amplifier. Even the AD5539 would only be useful at the front end of an oscilloscope with a modest bandwidth of about 20 MHz, and then something would have to be done about its high input bias current. A very important feature which any oscilloscope must have is that the apparent d.c. level displayed is quite independent of the signal source impedance. When the input socket to the oscilloscope is short circuited, open circuited, or connected to some finite impedance, there must be no observable shift in the display. This clearly rules out any kind of amplifier which has a significant input bias current.

6.4 The problem of the input circuit

The input attenuator circuits for a typical analog oscilloscope were discussed in chapter 5, section 5.6. These were designed to work into an amplifier having a 1 MΩ input impedance. On the most sensitive range of the instrument, the input signal is taken directly to this 1 MΩ input impedance circuit.

As stated in the previous section, the input circuit should have negligible input bias current. It must also be protected in some way from the possibility that the user will connect the input of the oscilloscope to some very high voltage.

Both these essential requirements are satisfied by means of the circuit shown in Fig. 6.2. In this typical analog oscilloscope circuit, a dual JFET, a 2N5911, is used. This kind of device has a very small input bias current, typically 100 pA at 25 °C. This will produce a change in apparent input voltage of less than 100 μV when the input socket is short circuited. Unfortunately the input bias current of a JFET increases very rapidly with temperature and, from this point of view, a MOSFET would be better. However, the MOSFET suffers from greater flicker noise, a point which will be discussed in chapter 10, and it is more difficult to get a matched pair of devices.

The 2N5911 is protected by means of the two 1N914 diodes in Fig. 6.2.

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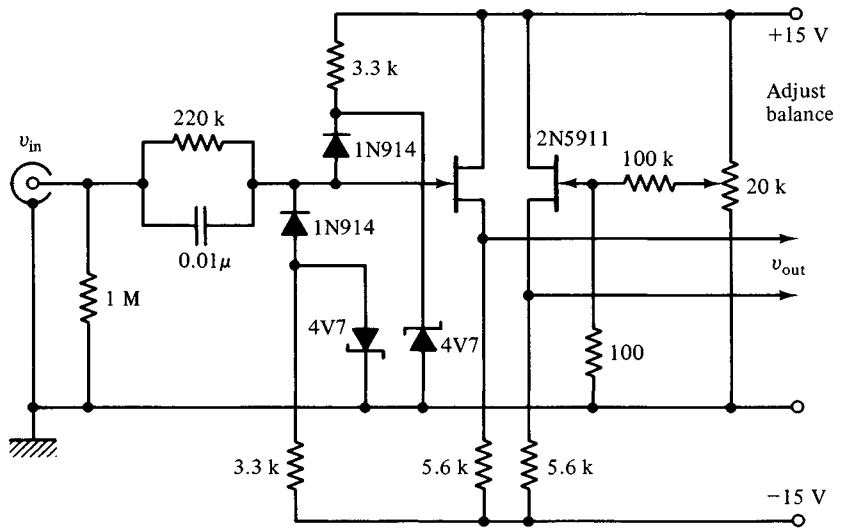

Fig. 6.2. A typical input stage for an analog oscilloscope using a dual JFET which is protected against excessive input voltages.

If the oscilloscope input, on its most sensitive range, which would be typically a few millivolts per division, were connected to a voltage in excess of ± 4.7 V, one or the other of the 1N914 diodes would begin to conduct and limit the gate to source voltage of the 2N5911 to a value well below breakdown. In fact some ± 600 V could be applied to the input before the protection circuit would be rendered ineffective, because of the 220 kΩ resistor which has been put in series with the input lead. This 220 kΩ resistor is shunted with a 0.01 μF capacitor to eliminate the attenuation that it would present to high frequency input signals because of the capacitance at the gate of the 2N5911. This capacitance can total about 10 pF: the input capacitance of the 2N5911 plus the capacitance of the two reverse biassed 1N914 diodes. Typically, the total input capacitance of a simple analog oscilloscope will total about 20 pF because of additional wiring and because of the problems discussed in chapter 5, section 5.6.

6.5 Feedback

The gain of the input stage shown in Fig. 6.2, $\Delta v_{out}/\Delta v_{in}$, is very close to unity. If R_s is the 5.6 kΩ resistor connected to the source of the left-hand side of the 2N5911, it is clear that

$$g_m(\Delta v_{in} - \Delta v_{out}) = \Delta v_{out}/R_s \tag{6.1}$$

where g_m is the forward transconductance of the 2N5911.

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Equation (6.1) leads to the well-known result for the gain of a source follower circuit,

$$\Delta v_{out}/\Delta v_{in} = g_m R_s/(1+g_m R_s) \qquad (6.2).$$

This is, of course, evidence that the source follower is really an amplifier with an open-loop gain of $g_m R_s$ which has 100% negative feedback. The 100% negative feedback arises because of the *circuit shape*: the output terminal and the negative going input terminal are one and the same thing, the source of the JFET.

Feedback of this very local kind is a feature of the circuits which will be considered in the next few sections as a typical analog oscilloscope vertical deflection amplifier is dealt with stage by stage. Fig. 6.2 shows another feature which will be common to all these circuits: balance. The right-hand side of Fig. 6.2 provides a second output terminal which should be at the same mean voltage level as the left-hand output terminal, regardless of changes in temperature. The stages which follow should then take this balanced output signal and amplify it up to the level required for the vertical deflection plates, which present a balanced load.

Local feedback, that is negative feedback across each stage of the vertical deflection amplifier, is essential if the full gain-bandwidth of the active devices is to be reflected in the overall bandwidth of the amplifier. This is clear if Fig. 6.1 is considered again. The AD3554 and AD5539 operational amplifiers have gain-bandwidth products well over 1 GHz, as would be expected from a bipolar monolithic or hybrid technology, but, because these are both multistage amplifiers, only a modest amount of feedback may be applied overall, otherwise the resulting feedback amplifier will be unstable. This is particularly evident for the AD3554: despite its 1.7 GHz gain-bandwidth product, inferred from an extrapolation of the 6 db/octave part of its open-loop gain characteristic, it cannot be used with a feedback fraction of more than -60 db, giving a gain of 60 db but a bandwidth of only about 1 MHz.

6.6 Local series and shunt feedback

Very wide bandwidth and well-defined gain can be obtained from circuits which are built up from the two elementary circuit shapes shown in Figs. 6.3(*a*) and (*b*). These are often called 'series feedback' and 'shunt feedback' circuits, respectively [6].

In the series feedback circuit the transistor is being used as a transconductance amplifier, which means that its output current is considered to depend upon its base to emitter voltage. This voltage is formed by subtracting a voltage proportional to the output current from

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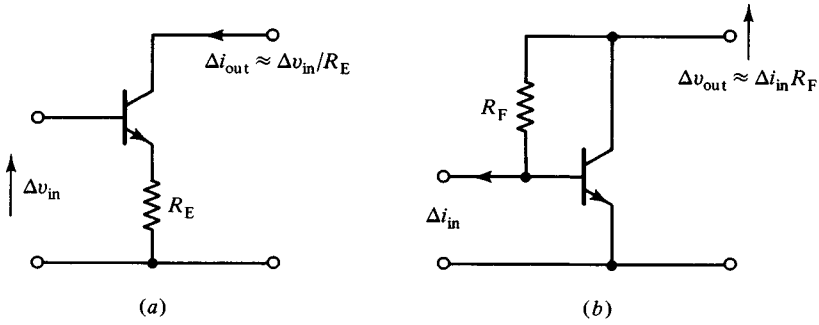

Fig. 6.3. The series feedback circuit, (a), and the shunt feedback circuit, (b).

the true input voltage, v_{in}. In other words, this is an example of negative feedback of a *voltage* proportional to *output current*. It results, as shown in Fig. 6.3(*a*), in a circuit which converts a change in input voltage into a well-defined change in output current: $\Delta i_{out} \approx \Delta v_{in}/R_E$. An accurate expression will be given below, when the final circuit shape is discussed.

In the shunt feedback circuit, Fig. 6.3(*b*), the transistor is being used as a current amplifier, which means that its output current is considered to depend upon its base current. This base current is formed by subtracting a current proportional to output voltage from the true input current, i_{in}. In other words, this is an example of negative feedback of a *current* proportional to *output voltage*. It results, as shown in Fig. 6.3(*b*), in a circuit which converts a change in input current into a well-defined change in output voltage: $\Delta v_{out} \approx \Delta i_{in} R_F$. Again, an accurate expression is given below.

6.7 Combining the shunt and series feedback circuits

The simple way in which Figs 6.3(*a*) and (*b*) have been drawn suggests, almost at once, that these two circuits can be combined to form a new circuit shape for a voltage amplifier with a gain R_F/R_E. This idea may have been first put forward in an important paper by Cherry and Hooper [7] and is shown in Fig. 6.4, but Fig. 6.4 is a long way from being any kind of useful circuit. In the first place, a balanced amplifier is needed for the analog oscilloscope deflection amplifier, for the reasons given in section 6.5. Secondly, a practical circuit based upon Fig. 6.4 would introduce a considerable level shift because the output terminal must be positive, with respect to the input terminal, by $2V_{CE}$, where V_{CE} will be at least 5 V if good high frequency performance is to be obtained. This level shift may not matter in an analog oscilloscope deflection amplifier because the CRT

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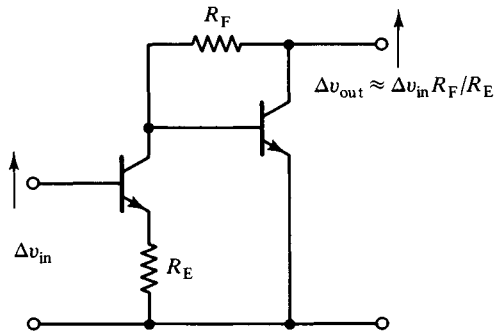

Fig. 6.4. An academic series/shunt feedback pair.

deflection plates could both be at quite a high d.c. level. It is unlikely, however, that the designer would consider this way of accommodating a large level shift a good idea, because it would involve quite complicated power supply arrangements for the amplifier circuits.

6.8 An experimental circuit

Fig. 6.5 shows the first experimental circuit for this chapter and illustrates one of the many possible ways of providing balanced amplification with negligible level shift by combining the series feedback and shunt feedback circuits.

In Fig. 6.5, series feedback is applied to the long tailed pair Q_5 and Q_4 by means of two equal resistors, R_3 and R_4. The current output from this long tailed pair drives a second long tailed pair, Q_2 and Q_1, which has shunt feedback applied by means of two equal resistors, R_{11} and R_{15}. The circuit is built around a CA3096A transistor array, and the numbering of the devices corresponds to the numbering on the data sheet.

By using pnp transistors for the first stage, Q_5 and Q_4, and then npn transistors for the second stage, Q_2 and Q_1, a negligible level shift is involved in going from input to output when the component values are chosen correctly. There are, of course, a number of ways of doing this when an amplifier involves several stages, instead of simply two stages like the circuit shown in Fig. 6.5. The first stage may be npn, the second stage pnp: Fig. 6.5 uses the alternative simply because the pnp devices in the CA3096A are designed to work at a lower current than the npn devices, so that it is sensible to use pnp at the input end and npn at the output. Another possible mix of device polarity is to use npn, or pnp, for the first two stages, and then restore the level by using the opposite polarity in the third and fourth stages, and so on.

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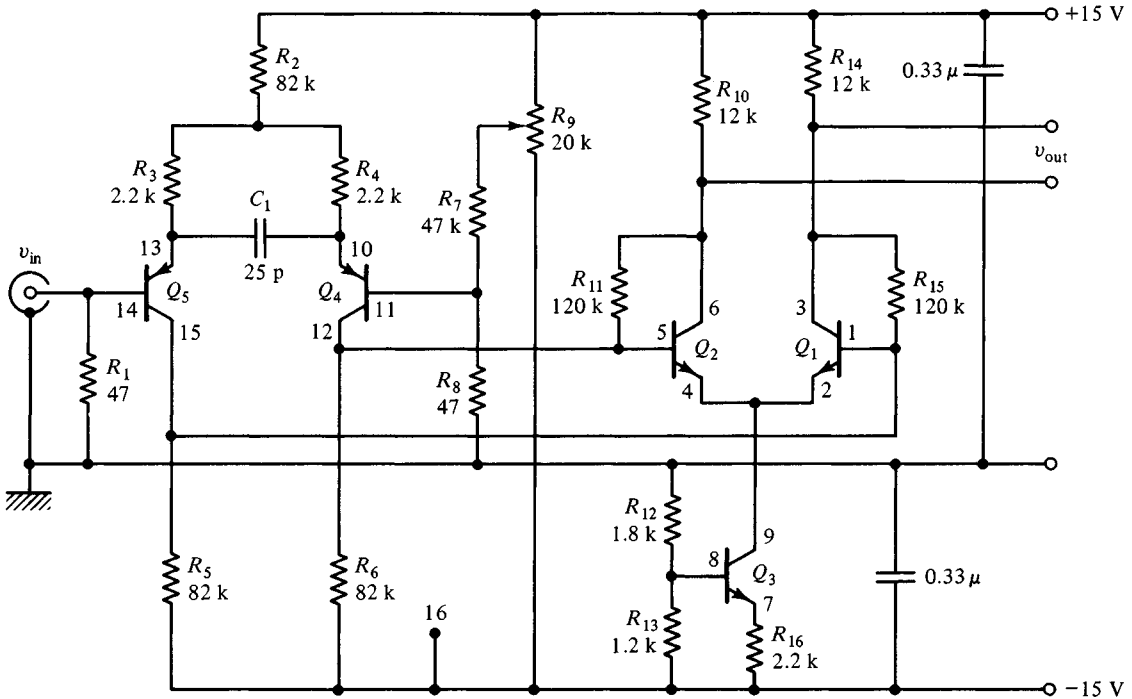

Fig. 6.5. An experimental wide-band amplifier circuit built around a CA3096 transistor array.

This idea of mixing device polarity to give zero d.c. level shift between the input and output terminals of a d-c amplifier is very old. A circuit published in 1955 by Slaughter [8] uses the idea, with transistors of the very earliest kind. The wide adoption of this idea had to wait for really good dual high frequency devices, of both pnp and npn polarity, to become available. A monolithic process which can provide good transistors of both polarities still presents problems. This is why many analog oscilloscope vertical amplifiers are made with discrete components, albeit using the most advanced surface mounting techniques with components on both sides of the circuit board [9]. The operational amplifiers which are the subject of Fig. 6.1 solve the level shifting problem as follows: the AD3554 is a hybrid circuit using npn and pnp devices; the CA3100 uses npn devices and p-channel MOSTs; the AD5539 has only npn devices and makes use of several base-emitter voltage drops to give the required level shift.

The resistors R_5 and R_6 play an important role in the circuit shown in Fig. 6.5 because they must carry the mean collector currents of Q_5 and Q_4 as well as the mean currents flowing in the shunt feedback resistors, R_{11} and R_{15}. In most designs these two currents are about the same order of magnitude. The currents in R_5 and R_6 are almost constant because changes in the collector currents of Q_5 and Q_4 should be transferred directly into the shunt feedback stage, Q_2 and Q_1. Writing $R_3 = R_4 = R_E$, these changes in collector current for Q_5 and Q_4 may be written,

$$\Delta i_{c5} = -g_{m5}(\Delta v_{in}/2)/(1 + g_{m5} R_E) \tag{6.3}$$

and

$$\Delta i_{c4} = +g_{m4}(\Delta v_{in}/2)/(1 + g_{m4} R_E) \tag{6.4}$$

Writing $g_{m5} = g_{m4} = g_m$, it follows that a fairly accurate expression for the input current from Q_2 and Q_1 would be,

$$\Delta i_{c4} - \Delta i_{c5} = \Delta v_{in}/(g_m^{-1} + R_E) \tag{6.5}$$

and this will only be equal to $\Delta v_{in}/R_E$ when the term g_m^{-1} is small compared to R_E. For this reason it is important to keep the full expression, equation (6.5), in the analysis.

Passing on to the second stage, it is easy to show, using equation (6.5), that

$$\Delta v_{out}(1/R_F + 1/R_L h_{fe} + 1/R_F h_{fe}) = \Delta v_{in}/(g_m^{-1} + R_E) \tag{6.6}$$

where $R_F = R_{11} = R_{15}$, $R_L = R_{10} = R_{14}$ and $h_{fe} = h_{fe1} = h_{fe2}$.

The term $1/R_F h_{fe}$ can be neglected, but if R_L is made much lower than R_F the feedback resistor should be thought of as being shunted by a

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resistor $R_L h_{fe}$. A fairly accurate expression for the overall low frequency gain of the circuit shown in Fig. 6.5 is thus

$$\Delta v_{out}/\Delta v_{in} = R'_F/R'_E \tag{6.7}$$

where R'_F is the parallel combination of R_F and $R_L h_{fe}$, and R'_E is the series combination of R_E and g_m^{-1}.

6.9 Component values

All the component values are marked on Fig. 6.5. A single ended input is provided, acting as a termination for the pulse generator that will be used as a signal source. This means that the 'adjust balance' potentiometer, shown first in Fig. 6.2, is now transferred to the experimental circuit as R_9.

R_2 is chosen to make the collector currents in Q_5 and Q_4 about 100 μA each, because this is the optimum for the pnp devices in the CA3096 array. This makes g_m^{-1}, in equation (6.7), about 300 Ω so that R_E is chosen to be well above this, but not so great as to allow g_m^{-1} to be neglected.

Q_3 is being used as the current sink for Q_2 and Q_1 and, as these npn devices in the CA3096A have optimum h_{FE} at a collector current of about 1 mA, R_{12}, R_{13} and R_{16} are chosen to make Q_3 sink just over 2 mA.

The shunt feedback resistors are chosen to give an overall low frequency gain of about 50, giving $R_{11} = R_{15} = 120$ kΩ. The V_{CE} of Q_5, Q_4, Q_2 and Q_1 is then chosen to be 5 V in magnitude and this enables R_5 and R_6 to be determined because the d.c. current in R_{11} and R_{15} is then known. The values of R_{10} and R_{11} then follow, and as these can be made 12 kΩ it is clear that $h_{fe} R_L$ is much greater than R_F, in equation (6.7), at least at low frequency, and the low frequency gain of the experimental circuit should be given by

$$G_0 = R_F/(g_m^{-1} + R_E) \tag{6.8}$$

which comes out to be 48.

6.10 Experimental measurements

Initially, measurements should be made without C_1 connected. Check the d.c. levels in the circuit and then connect an oscilloscope to the output points, pins 3 and 6 of the CA3096A, using two $\times 10$ high impedance probes. The oscilloscope sensitivity should be at least 100 mV/div and bandwidth at least 10 MHz.

Apply a 10 μs positive going pulse of a few millivolts and check that the low frequency gain is close to the value of 48 predicted by equation (6.8).

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The full gain is, of course, given by the true differential output voltage, observed between pins 3 and 6 on the CA3096A, divided by the input pulse amplitude. A positive pulse should be seen on pin 3, and an equal, but opposite polarity, pulse on pin 6. The experimentalist should resist the temptation at this stage of using the oscilloscope in the 'channel A plus inverted channel B', or differential, mode, because some interesting things may be seen which need explaining. For example, when the output pulses are observed separately, removing one of the high impedance probes causes the pulse which is left under observation to have a much longer rise time. In other words, adding capacitance to pin 3 slows down the response of pin 3, as would be expected, but appears to speed up the response on pin 6, the explanation of which may need some thought. The circuit is quite symmetrical in this respect: a few picofarads added between pin 6 and ground, when both pin 3 and pin 6 are under observation, will be seen to slow the response at pin 6 while speeding the response at pin 3.

These remarks lead to a discussion of the high frequency performance of the experimental circuit shown in Fig. 6.5. It is obvious that the shunt feedback stage, Q_2 and Q_1, will be very sensitive to any capacitance which may be in parallel with the feedback resistors, R_{11} and R_{15}. The R_F, which occurs in equation (6.6), should be replaced by Z_F, to represent the parallel combination of R_F and C_{cb}, where C_{cb} is the collector junction capacitance of Q_1 and Q_2, plus any stray capacitance due to the circuit hardware. As it stands, this output stage should have a rise time of the order of $C_{cb} R_F$, which could be as long as 200 ns.

However, it will be observed that the experimental circuit shown in Fig. 6.5 is not very sensitive to capacitive loading across its true output: that is from pin 3 to pin 6. The reason for this is the quite low differential output impedance. The experimentalist should obtain an expression for this impedance, which should simplify to $R_{out} = 2R_F/h_{fe}$ under the same assumptions which lead to equation (6.8), and make a measurement of R_{out} by adding a resistive load from pin 3 to pin 6.

The addition of C_1, shown in Fig. 6.5, to the experimental circuit makes a considerable improvement to the speed of response because this should compensate for the $C_{cb} R_F$ time constant of the output stage by means of the $2C_1 R_E$ time constant introduced at the input stage. The circuit is then left with two other very serious high frequency limitations which have not been mentioned so far. The first is the frequency dependence of h_{fe} for Q_2 and Q_1 and brings the argument back to equation (6.7). The h_{fe} of the npn devices in the CA3096A begins to fall off above 4 MHz, and it will no longer be possible to assume that $h_{fe} R_L$ is much greater than R_F. However, with a low frequency h_{fe} of 400 and R_L at 12 k it will be at frequencies

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well above 10 MHz before $h_{fe} R_L$ falls to equal R_F. The gain of the circuit would then begin to fall very rapidly, as does h_{fe}.

The second reason for the limited bandwidth of the circuit shown in Fig. 6.5, and the most important, is the poor high frequency performance of the pnp transistors in the CA3096A: Q_5 and Q_4. These lateral devices have a gain-bandwidth product of only 6.8 MHz and, in fact, this will be found to be about the bandwidth of the experimental circuit when C_1 is in place.

By using the CA3096A, it has been possible to build an experimental circuit of the same circuit shape as a real analog oscilloscope deflection amplifier. The high frequency performance limits, however, have been brought down into a lower frequency range where the experimentalist may make measurements with quite simple equipment.

A complete understanding of the high frequency performance of the experimental circuit shown in Fig. 6.5 calls for careful modelling of the active devices and detailed calculation. For a first consideration of this problem, chapter 7 of the book by Gray and Meyer [6] is helpful. To take the problem further, an excellent paper by Faulkner [10] will be very useful.

6.11 Output stage circuits

The output stage of an analog oscilloscope deflection amplifier calls for some special consideration because of the nature of the load which is put upon it. When the CRT is a conventional one, with electrostatic deflection, this load is a pure capacitance which could be as much as 20 pF with the cables that will be involved [11], and full vertical deflection could call for differential output voltages of 50 V amplitude. For a quite modest oscilloscope rise time of 10 ns, this then calls for a maximum output current, $i = C\mathrm{d}v/\mathrm{d}t$, of at least 100 mA from the deflection amplifier.

Very wide bandwidth analog oscilloscopes, that is instruments with bandwidths above 250 MHz, do not have the same problems because their CRTs will have a distributed vertical deflection system [12] which presents a constant and real impedance load for the wide-band deflection amplifier. The horizontal deflection amplifier will be of the type discussed here, however.

Consider Fig. 6.6 as a first step towards a solution of the problem of finding a good circuit shape for the output stage of an analog oscilloscope deflection amplifier. In Fig. 6.6, v_{in} should be thought of as the differential output from several stages of amplification of the kind discussed so far in

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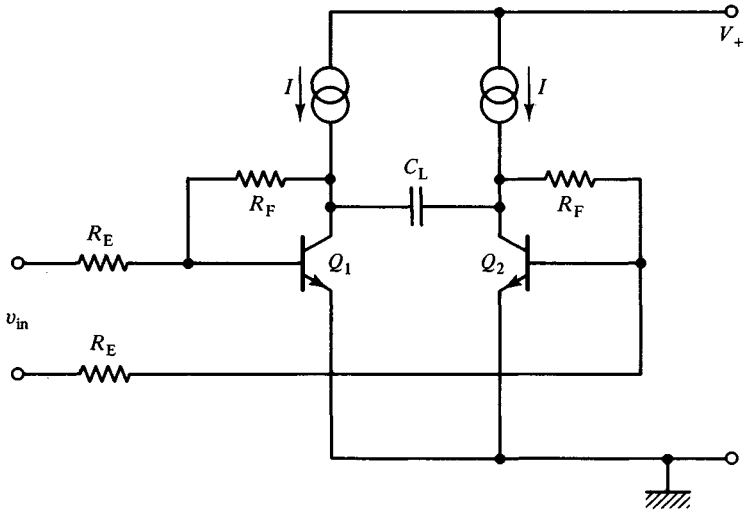

Fig. 6.6. A first step towards a good circuit shape for the output stage of an oscilloscope deflection amplifier. The CRT deflection plates are represented by the capacitor, C_L.

this chapter and illustrated by the experimental circuit shown in Fig. 6.5. The proposed output stage shown in Fig. 6.6 has a well-defined gain, R_F/R_E, and v_{in} would have a small negative common mode level, $-V_+ R_E/2R_F$, in order to bring both ends of the load capacitor, C_L, which represents the CRT deflection plates, to a voltage level $V_+/2$. It is not, of course, necessary to level shift the voltage which is actually at both deflection plates so that this voltage has zero mean level.

Now as Fig. 6.6 stands, the constant current sources which are used as collector loads for Q_1 and Q_2 will have to have a magnitude slightly greater than the maximum current demanded by the deflection plates. This was calculated to be 100 mA at the beginning of this section. Similarly, V_+ will have to be slightly greater than the maximum deflection voltage mentioned above, and this was 50 V. The argument so far is leading towards an output stage that dissipates 10 W when it is under quiescent conditions and when its true load, C_L, is taking no current at all. This is clearly a point where the circuit designer stops to consider what is really called for in this circuit.

Two points should be taken into consideration. The first is that the load, C_L, calls for negligible current for most of the time because any analog oscilloscope is, for most of the time, displaying signals which change with time very much more slowly than the maximum rate of change that the instrument is able to display. The second point is that

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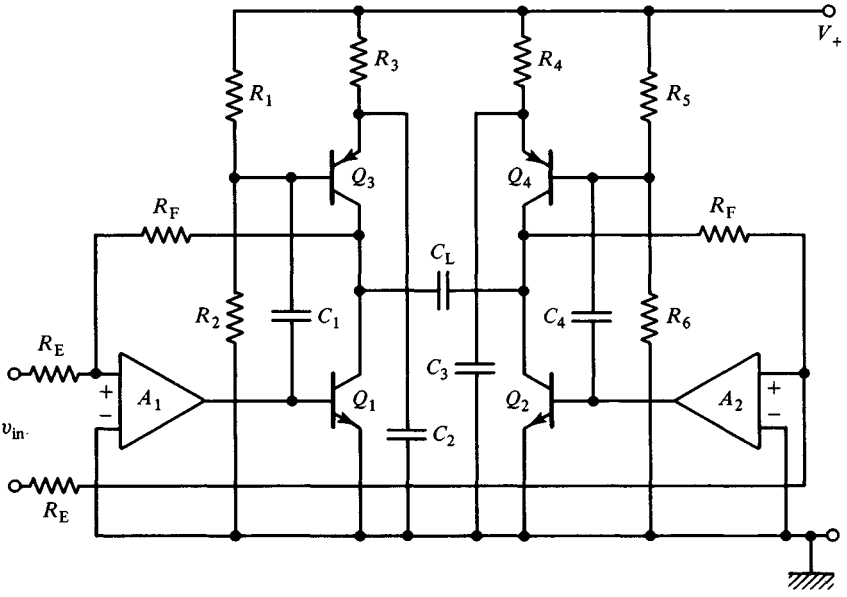

Fig. 6.7. A second step towards a good circuit shape for the output stage of an analog oscilloscope deflection amplifier.

when rapid deflections are called for, the high transient current demanded by C_L may be drawn from a capacitor somewhere in the circuit. Provided this capacitor is much greater than C_L, it will always be able to supply the transient current because rapidly repeated transients could only cause problems when these occur so frequently that the input signal frequency is beyond the bandwidth of the instrument.

These two considerations suggest a development from the circuit shape shown in Fig. 6.6 to the new circuit shown in Fig. 6.7. The details of the current sources for Q_1 and Q_2 are now shown. These current sources, Q_3 and Q_4, both supply d.c. at a level determined by the choice of R_3 and R_4, and the voltage level set at the bases of Q_3 and Q_4 by means of the potential dividers, $R_1/(R_1+R_2)$ and $R_5/(R_5+R_6)$.

While Q_3 and Q_4 supply a d.c. of only a few milliamps, the large transient currents would be available because of the way in which the capacitors C_2 and C_3 have been arranged. This, along with the fact that the base of Q_3 is now connected, at high frequencies, to the base of Q_1 through C_1 (and, similarly, Q_4 is connected to Q_2 through C_4), means that Q_3 can supply a large current, out of C_2, when Q_2 draws this same large current from the right-hand side of C_L. Similarly, Q_4 can supply the large current, out of C_3, which is called for by Q_1 when current is to be drawn from the left-hand side of C_L.

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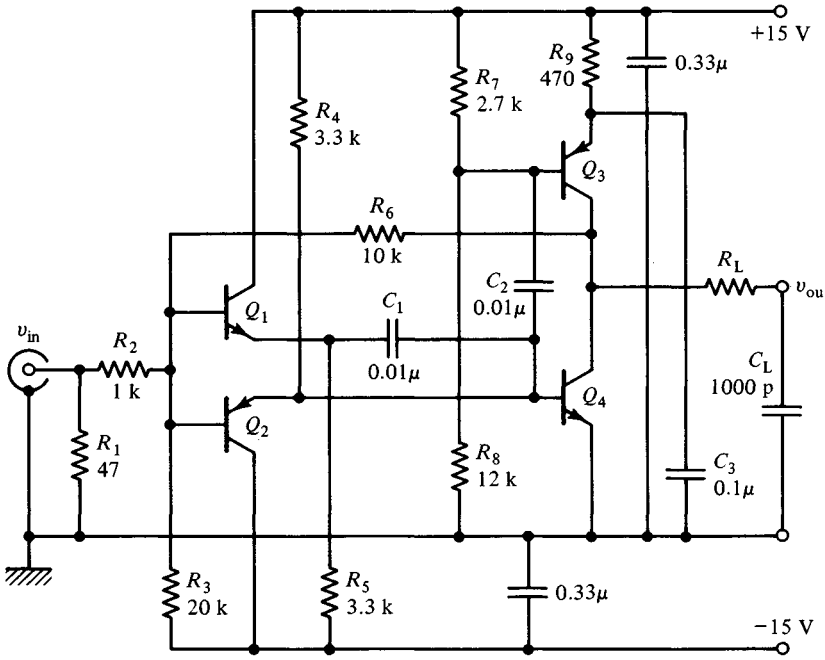

Fig. 6.8. An experimental output circuit. Q_1 and Q_4 are 2N2222A and Q_2 and Q_4 are 2N2907A. For the first measurements omit C_1 and C_2 and make R_L zero.

6.12 An experimental output circuit

Fig. 6.8 shows an experimental version of the circuit shown in Fig. 6.7. Only one side of the output stage need be built, because all the interesting behaviour can be observed when one end of the load, C_L, is grounded and the other end is driven, either positive or negative going, from a mean level of $V_+/2$.

To begin with, R_L should be made zero and C_L made 1000 pF. The operational amplifier, A_1 in Fig. 6.7, has been replaced in Fig. 6.8 by simple emitter followers, Q_1 and Q_2. These emitter followers provide a symmetrical low impedance drive to the output transistors, Q_3 and Q_4, and also, by making $R_3 = 2R_6$, set the d.c. level at the output terminal to $V_+/2$. The overall voltage gain is set by making $R_6/R_2 = 10$.

Two very valuable circuit shapes can be seen in Fig. 6.8. The first is the output stage itself, consisting of two complementary transistors with their *collectors* connected together to form the output terminal. The second is the connection of the two emitter followers, Q_1 and Q_2 in Fig. 6.8. These complementary devices have their *bases* connected together to form an

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input terminal (equivalent to the positive input of A_1 in Fig. 6.7). Unlike the well-known complementary emitter follower, however, the emitters of Q_1 and Q_2 are taken to quite separate resistors, R_4 and R_5, so that, under quiescent conditions, Q_1 and Q_2 both have the same magnitude of collector current.

Because Q_1 and Q_2 are npn and pnp respectively, their base currents are of opposite sign and this means that it is possible, when their current gains are about equal, for the quiescent current in R_2 to be very small. A further advantage of this circuit shape is that the two outputs have a level shift of about ± 0.7 V with respect to the common input. In Fig. 6.8 this is used to make the input terminal have a very small offset voltage: the level shift up to 0.7 V provided by Q_2 is just what is needed to direct-couple into Q_4 from an input terminal close to zero mean level.

The high frequency drive from Q_1 and Q_2 into Q_3 and Q_4 is though the capacitors, C_1 and C_2. It was pointed out above, in section 6.11 when discussing Fig. 6.7, that the quiescent current in the output transistors need only be a few milliamps. In the experimental circuit R_7, R_8 and R_9 have been chosen to make this quiescent current about 4 mA.

6.13 Measurements on the experimental output circuit

The power supply voltage used in the experimental circuit is only $+15$ V, in contrast to at least 100 V which would be found in any real analog oscilloscope deflection amplifier output circuit. This is done for experimental convenience. It is also convenient to make the circuit at least one order of magnitude slower than any real circuit so that measurements can be made with an oscilloscope of modest bandwidth.

This means that C_L should be at least two orders of magnitude greater than the 10 pF typical of a real circuit: one order for the lower supply voltage and one order for the lower circuit speed. The transient current in the experimental circuit will then correspond to that in the real circuit.

In view of this, C_L is made 1000 pF. To begin with C_1 and C_2 are omitted. This makes it possible to check the very slow transient performance of the experimental circuit when it is operating along lines analogous to Fig. 6.6 with constant current sources of only 4 mA.

The input signal needed is a pulse, 10 μs duration with an amplitude between ± 100 mV and ± 1 V. As the circuit has a gain of 10, it is possible to observe the maximum output swing, positive or negative, with an input pulse of less than ± 1 V amplitude. The slew rate at the output will be seen to be only a few volts per microsecond at this stage. The form of the response will be simply first order: an exponential rise or fall from $V_+/2$.

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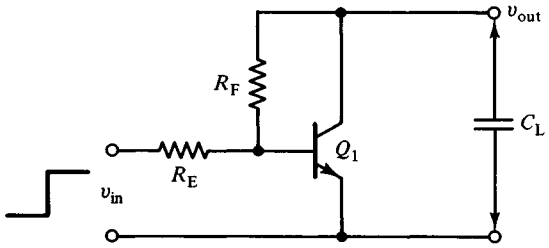

Fig. 6.9. The essential features of the circuit shown in Fig. 6.8 when there is a positive going input step and $R_L = 0$.

Now when C_1 and C_2 are added to the experimental circuit a dramatic improvement in speed naturally results. The rise and fall times at the output, across the 1000 pF load capacitor, C_L, will be only a few tens of nanoseconds. This means that currents of hundreds of milliamps are now available.

The form of the transient response, in this new fast circuit, is not at all satisfactory, however. The response to a step input will now be a damped oscillation: typically some 30% overshoot followed by several cycles of oscillation at a frequency around 10 MHz. It is important to understand why this is so, and then see how the circuit should be changed to correct for the poor transient performance.

6.14 Transient analysis

The reason for the underdamped transient response of the experimental circuit, Fig. 6.8, and the steps that should be taken to correct this, may be seen if the simple circuit of Fig. 6.9 is considered.

In Fig. 6.9, Q_1 should be thought of as representing both Q_1 and Q_4 in Fig. 6.8, because these are the two devices which are active when a positive input step, as shown in Fig. 6.9, is applied.

To analyse Fig. 6.9, the charge control equations [13]

$$i_b = q_b/T_b + dq_b/dt \tag{6.9}$$

and

$$i_c = q_b/T_t \tag{6.10}$$

are all that are required. These equations relate the instantaneous base current, i_b, and collector current, i_c, to the charge, q_b, in the base region of the device when it is working in the active state. The two characteristic time constants are, approximately, the minority carrier lifetime in the

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base, T_b, and the base transit time, T_t. In the steady state, dividing equation (6.10) by equation (6.9) leads to the relationship

$$T_b/T_t = h_{FE} \tag{6.11}$$

for the device current gain at zero frequency.

Substituting equation (6.10) into equation (6.9), and using equation (6.11) leads to

$$T_t \mathrm{d}i_c/\mathrm{d}t + \mathrm{i}_c/h_{FE} = i_b \tag{6.12}$$

as the differential equation governing the transistor.

Now in the simple circuit of Fig. 6.9, the current in R_F may be neglected in comparison to the collector current. It follows that

$$i_c = -C_L \mathrm{d}v_{out}/\mathrm{d}t. \tag{6.13}$$

The base current of Q_1, in Fig. 6.9, is simply

$$i_b = v_{in}/R_E + v_{out}/R_F. \tag{6.14}$$

Substituting equation (6.13) and (6.14) into equation (6.12) then leads to the second order differential equation which governs the entire circuit:

$$(C_L R_F T_t)\mathrm{d}^2 v_{out}/\mathrm{d}t^2 + (C_L R_F/h_{FE})\mathrm{d}v_{out}/\mathrm{d}t + v_{out} = -(R_F/R_E)v_{in}. \tag{6.15}$$

Equation (6.15) shows that the steady state output, $v_{out} = -(R_F/R_E)v_{in}$, will be approached by means of a quite lightly damped sinusoidal response. The damping time constant in equation (6.15) is $C_L R_F/h_{FE}$ and is small, because h_{FE} is the product of the current gains of both Q_1 and Q_4 in Fig. 6.8.

There is far more to this analysis than this simple conclusion, however. It is now possible to see what must be added to Fig. 6.9, and thus to Fig. 6.8, to increase the damping. The reason for the light damping is that C_L holds down the rise of the output voltage when the input step arrives, thus allowing the base current to have the very high initial value of v_{in}/R_E. What is needed is some modification to the circuit so that some feedback takes control right from the start of the transient, and there are two ways to do this.

The first thought the designer might have would be to add a capacitor in parallel with R_F. This capacitor, C_F, would begin to feed current, $C_F \mathrm{d}v_{out}/\mathrm{d}t$, back to the base of Q_1 immediately the voltage across C_L began to change.

A second approach for the designer would be to recall that this is a deflection amplifier output circuit, and that it is the voltage across C_L

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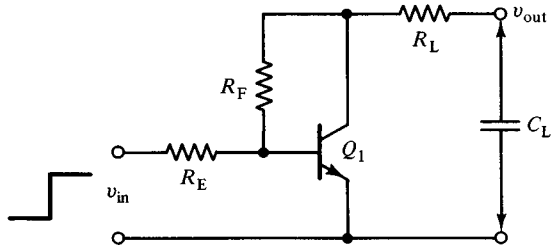

Fig. 6.10. *Adding resistor* R_L *increases the circuit damping.*

which is the output voltage of interest. Adding resistance, R_L, in series with C_L, as shown in Fig. 6.10, allows the collector voltage to change by an amount $i_c R_L$ immediately the collector current begins to flow. This change in collector voltage immediately produces a change in the current fed back through R_F. The equation governing Fig. 6.10 would then be

$$(C_L R_F T_t)\,d^2v_{out}/dt^2 + C_L R_F(h_{FE}^{-1} + R_L/R_F)\,dv_{out}/dt + v_{out} = -(R_F/R_E)v_{in} \tag{6.16}$$

in contrast to equation (6.15). The damping has been increased.

Of the two methods, adding R_L is a better solution because it increases the damping without also reducing the natural resonant frequency of the circuit, which remains at

$$\omega_n = (C_L R_F T_t)^{-\frac{1}{2}}. \tag{6.17}$$

Naturally, this very approximate model may only be used as a rough guide to the value of R_L that will give optimum transient response. What is important about the model is that it should lead the designer to see how the original circuit should be modified in order to correct for the unacceptable performance that it originally had.

6.15 Further experiments and conclusions

Equation (6.16) suggests that R_L/R_F should be made about 10^{-3} for a good transient response to be obtained from the experimental circuit of Fig. 6.8. This will be found when R_F is taken at the value of 10 kΩ, given for R_6 in Fig. 6.8, C_L is 1000 pF and T_t is taken at 0.5 ns, which is a sensible value for the kind of devices being used.

From this rough calculation, values of R_L should now be added to the experimental circuit shown in Fig. 6.8. This must be done as shown in Fig. 6.10: the output voltage is still measured across C_L. A good transient response, that is one showing a very small overshoot, should be obtained

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when R_L is about 10 Ω. The response should be the same for both positive and negative going step inputs, even when the change in the voltage across C_L is several volts. As the output transient amplitude begins to approach its maximum value, which is close to $V_+/2$ in the negative going direction but less for positive going outputs because of the voltage drop across R_9, non-linearities will be observed and these should be looked at carefully and explained.

The rise and fall times across the 1000 pF load should be in the region of 50 ns for this experimental circuit. For an output voltage of 5 V, this means that transient currents close to 100 mA are flowing in Q_3 and Q_4. The paths taken by these large transient currents, in the experimental circuit shown in Fig. 6.8, should be considered and the voltage at the emitter of Q_3, and on the positive power supply line, should be looked at with the oscilloscope on a sensitive range, using the a.c. input option. It is also interesting to look at the change in voltage which occurs at the common bases of Q_1 and Q_2. The approximate transient analysis of the previous section assumed that this was negligible.

In conclusion, the problem of designing a wide-band d-c deflection amplifier for a conventional analog oscilloscope has brought out the importance of feedback. The way feedback is supplied to the various stages of amplification is central to this design problem. In the input stages the adoption of a shunt feedback stage driving a series feedback stage, which, in turn, drives the next shunt feedback stage, means that the gain of each stage is well defined, the full bandwidth is available, and that the stages couple together with no problems because the output impedance of one is just what is needed to drive the input impedance of the next.

In the output stage, considered in the final section of this chapter, feedback is again local, applied across the output stage alone, but the circuit is now one which works at high power level because of the transient current demanded by the capacitive load. This is the reason for the interesting internal structure of the circuit, seen first in Fig. 6.7 with capacitors C_1, C_2, C_3 and C_4, and then in the experimental circuit, Fig. 6.8, with C_1, C_2 and C_3.

Notes

1 Maclean, D. J. H., *Broadband Feedback Amplifiers*, John Wiley, New York, 1982.
2 Kovács, F., *High-frequency Applications of Semi-Conductor Devices*, Elsevier, Amsterdam, 1981.
3 Carson, R. S., *High-frequency Amplifiers*, John Wiley, New York, second edition, 1982.

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4 In Fig. 6.1 the curve shown for the AD3554 has been copied from Fig. 1 of Analog Devices data sheet C700-9-4/82. The curve for the CA3100 has been copied from the RCA Solid State Data Book, SSD-240B, 1982, p. 137, Fig. 3. The curve for the AD5539 has been copied from Fig. 13 of Analog Devices data sheet C1044–2/87.

5 Von Ardenne, M., *Wireless Engineer*, **13**, 59–64, 1936. This paper describes a 0.2 Hz–3 MHz amplifier with a gain of 66 db. This was an outstanding achievement for the time. A more detailed picture of the state of electronics at that time may be obtained from O. S. Puckle's translation of von Ardenne's *Fernsehenempfang*, published by Chapman and Hall, London, 1936, under the title *Television Reception*.

6 Gray, P. R., and Meyer, R. G., *Analysis and Design of Analog Integrated Circuits*, John Wiley, New York, second edition, 1984, pp. 510–15.

7 Cherry, E. M., and Hooper, D. E., *Proc. IEE*, **110**, 375–89, 1963. This paper, entitled 'The design of wide-band transistor feedback amplifiers', marked a major step forward in technique. The rather sharp exchange of correspondence between P. J. Beneteau and the authors, on p. 1617 of the same volume, should be noted, however.

8 Slaughter, D. W., *Electronics* **28**, No. 5, 174–5, May, 1955.

9 The Hitachi V-1065/V, 100 MHz oscilloscope is an interesting example. This instrument was introduced around 1984.

10 Faulkner, D. W., *IEEE J. Sol. St. Circ.*, **SC-18**, 333–40, 1983. This paper, 'A wide-band limiting amplifier for optical fibre repeaters', describes a 470 MHz bandwidth, 60 db gain, amplifier which is made up of three shunt/series feedback pairs in cascade. The high frequency analysis and circuit simulation are considered in depth.

11 For data on conventional cathode ray tubes, the book by J. Czech, *Oscilloscope Measuring Techniques*, Philips Technical Library, Eindhoven, revised English edition, 1965 is still valuable. The input capacitance to the *Y* deflection plates of a modern CRT, specially designed for a wide-band oscilloscope with the connections to the plates available at the side of the tube, can be as small as 3 pF. The current involved would still be about 100 mA, however, because the rise time would be well below 10 ns. For today's CRT technology there is an excellent review, in English, by W. M. P. Zeppenfeld, 'Oscilloscope Tubes: past, present and future', in *Acta Electron. (France)*, **24**, No. 4, 309–16, 1981–2, which gives many references.

12 Van Schaik, H., and Zeppenfeld, K., *Electronic Engineering*, **58**, No. 710, 47–9, February 1986.

13 These simple equations for the bipolar transistor are invaluable in circuit design because they provide a simple algebraic model for the active device. In contrast to the accurate model which must be used for numerical analysis and circuit optimisation, an algebraic model is needed when the designer is still searching for a good circuit shape. The excellent text, *Solid State Electronic Devices*, by B. G. Streetman, Prentice Hall, Englewood Cliffs, NJ, second edition, 1980, deals with the charge control model on pages 259–60 and 276–8. A very valuable review is 'Past and present of the charge control concept in the characterisation of the bipolar transistor', by J. te Winkel, *Adv. Electr. Electr. Phys.*, **39**, 253–89, 1975.

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