9

Phase locked loop circuits

9.1 Introduction

The phase locked loop (PLL) is used in a number of instrumentation systems. Best's text on PLLs [1] has a chapter on applications in which he lists tracking filters; modulators and demodulators for AM, FM and PM; the recovery of weak signals; frequency synthesis, a field on which there is another valuable text [2]; motor speed control; stereo decoding; sub-carrier detection in colour television; and many others.

The original idea of the PLL probably came from the work of de Bellescize in 1932 [3], who used the PLL in AM receiver design. Later work on this application by Tucker and Ridgway provoked a considerable correspondence [4] which suggests that the PLL may be a case of multiple invention, as is so often the case in the field of electronic circuit design.

The simplest kind of PLL is shown in Fig. 9.1. A phase detector is used to give a measure of the phase difference, φ, between an incoming signal, $v_1 \sin(\omega t)$, and a VCO. This phase difference is used as an error signal in a closed loop control system in such a way that the VCO 'locks' on the incoming signal and follows its changes in phase, and thus in frequency, over some range determined by the designer.

This chapter begins with a very brief look at PLL theory, and this leads at once to an experimental programme using an easily available PLL integrated circuit. This experimental programme illustrates a number of problems in PLL design and leads to the main topic of this chapter, which is a review of some of the circuit shapes, or circuit ideas, that have been applied in PLL integrated circuits over the past 20 years.

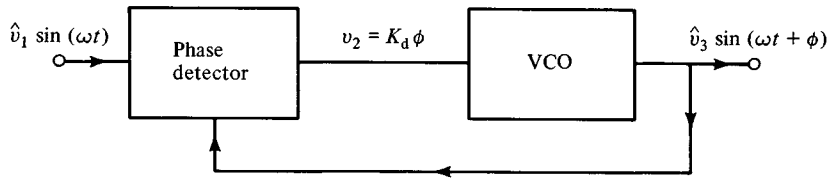

Fig. 9.1. A first order PLL.

9.2 The low pass filter

The PLL is usually introduced in the text books [5, 6] with a low pass filter in between the phase detector and the VCO. It is important to bear in mind why the need for this filter is tacitly assumed. The reason is that it is impossible to build a phase detector which gives an instantaneous measure of phase: that is one with the characteristic

$$v_2 = K_d \varphi \tag{9.1}$$

as shown in Fig. 9.1, where K_d is a simple constant, with dimensions volts per radian, involving no time dependence. The best that may be done in this direction is to build a digital phase detector that measures the time between zero crossings of the signal input and the VCO, also measures the period of one of these signals, and then gives a measure of phase, according to some algorithm, as an analog output. Best deals with such digital phase detectors in his book [7], but even such an advanced kind of phase detector must introduce a time delay of at least one cycle between the instantaneous values of its two inputs and the corresponding sampled value of their phase difference.

A simple phase detector, for example, a combination of limiting amplifiers and an analog multiplier, can only give a measure of relative phase angle by means of averaging. To implement this averaging, a low pass filter must be introduced into the PLL and this will have a profound effect upon the loop dynamics.

The most straightforward way of dealing with the dynamics of the PLL is to begin with the open-loop transfer function of the first order PLL shown in Fig. 9.1. Fig. 9.2 shows the first order loop opened, with its input and output variables now expressed as phases, φ_{in} and φ_{out}. For simplicity, the feedback input is taken as the $\varphi = 0$ reference. The change in the VCO frequency, shown in Fig. 9.2 as $\Delta f = K_o K_d \varphi_{in}$, where K_o is the control constant of the VCO in hertz per volt, may be written in terms of phase by using the fundamental relationship

$$2\pi\Delta f = \mathrm{d}\varphi_{out}/\mathrm{d}t. \tag{9.2}$$

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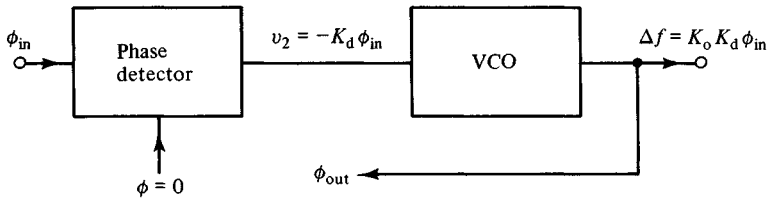

Fig. 9.2. *Opening the first order loop.*

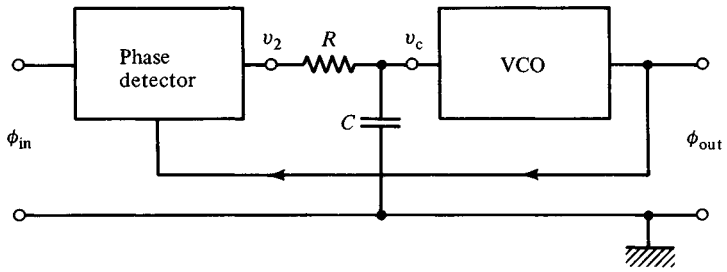

Fig. 9.3. *Adding a low pass filter to the PLL.*

By writing $\tilde{\varphi}_{in}$ and $\tilde{\varphi}_{out}$ to represent the Laplace transforms of the input and output variables, $\varphi_{in}(t)$ and $\varphi_{out}(t)$ the open-loop transfer function of the combined ideal phase detector, defined by equation (9.1), and VCO follows at once as

$$\tilde{\varphi}_{out}/\tilde{\varphi}_{in} = 2\pi K_o K_d/s \tag{9.3}$$

where s is the complex variable of the Laplace transform.

Equation (9.3) shows that the VCO behaves like an *integrator*: its transfer function is of the form $1/s$.

9.3 Loop dynamics with a low pass filter

Fig. 9.3 shows the PLL with a low pass filter inserted into the loop: a simple *RC* network. This network has a transfer function

$$\tilde{v}_c/\tilde{v}_2 = 1/(1+sCR) \tag{9.4}$$

where v_c is now the control voltage input to the VCO.

It follows that the open-loop transfer function of the PLL shown in Fig. 9.3 may be obtained by simply multiplying equation (9.3), which is the open-loop transfer function of the PLL with no filter, by equation (9.4). The result is

$$a(s) = 2\pi K_o K_d/s(1+sCR). \tag{9.5}$$

Using the well-known [8] relationship between the closed-loop transfer

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function, $A(s)$, of a feedback system (with 100% negative feedback), and its open-loop transfer function, $a(s)$,

$$A(s) = a(s)/[1 + a(s)] \tag{9.6}$$

it follows that the closed-loop transfer function of the second order PLL, shown in Fig. 9.3, may be written

$$\tilde{\varphi}_{\text{out}}/\tilde{\varphi}_{\text{in}} = \omega_{\text{n}}^2/(\omega_{\text{n}}^2 + \alpha_1 \omega_{\text{n}}\, s + s^2) \tag{9.7}$$

where

$$\omega_{\text{n}}^2 = 2\pi K_{\text{o}} K_{\text{d}}/CR \tag{9.8}$$

$\omega_{\text{n}}/2\pi$ being the natural resonant frequency of this second order control loop, and

$$\alpha_1 = 1/\omega_{\text{n}} CR \tag{9.9}$$

giving a measure of the damping.

The designer would now consider what values of ω_{n} and α_1 would be optimum for the application under consideration. For example, ω_{n} might be chosen to correspond to the bandwidth expected for the incoming phase modulated signal, and then CR chosen to make $\alpha_1 = \sqrt{2}$, which is the value that gives a maximally flat frequency response. These system considerations may run into very severe limitations, however, because of the intrinsic properties of the circuits which make up the PLL: the VCO and the phase detector. It is the circuit detail of PLLs which is really the topic of this chapter. The theory which has been outlined above is only needed to guide the designer along broadly sensible lines. It turns out that PLLs are an excellent example of circuit considerations laying considerable constraints upon system performance.

In order to introduce this aspect of PLL circuit design, it is best to go at once to a very simple experimental circuit using one of the widely available integrated circuit PLLs.

9.4 The CD74HC4046A

There are a number of integrated circuit PLLs in which a VCO, one or more varieties of phase detector, and perhaps a voltage reference along with a few operational amplifiers, are all combined together in one monolithic circuit inside a single package. The CD74HC4046A is a fairly recent example [9], and is of particular interest because it has three quite different kinds of phase detector available. Because of this, the VCO control input is brought out to one of the 16 external pins. This is a particularly useful feature for the experimentalist because it makes it

possible to insert a wide variety of filter types in between the phase detector and the VCO. Many integrated circuit PLLs do not have such flexibility because the phase detector output is connected internally to the VCO control input.

The CD74HC4046A is a CMOS integrated circuit. It is a development of the earlier CD4046A and CD4046B devices, which only have two kinds of phase detector available, and can only work up to just over 1 MHz. The CD74HC4046A can operate up to 18 MHz. Nearly all the experiments described below can be done with the earlier devices, however, using slightly different component values.

9.5 Experiments with the type I phase detector

Fig. 9.4 shows the first experimental circuit for this chapter. This uses the first kind of phase detector which is available on the CD74HC4046A device, shown on the left-hand side of Fig. 9.4, which involves two high gain amplifiers, A_1 and A_2, acting as limiting amplifiers, driving an exclusive OR gate, X. Marking this gate with an X indicates its close connection to the analog multiplier mentioned above in section 9.2.

The limiting amplifiers, A_1 and A_2, convert the two input signals into square waves. These square waves have the logic level of CMOS circuits: just above zero and just below V_{cc}. The exclusive OR gate gives a V_{cc} output if only *one* of its inputs is high. It thus produces a continuous zero output when the signals on the input pins, pins 14 and 3, are in-phase, and a continuous V_{cc} output when these two input signals differ in phase by 180°. In between these two extremes, the exclusive OR output will be a rectangular wave, at double the frequency of the input signals, varying in mark to space ratio as the phase varies, and having 1:1 mark to space ratio when the two input signals differ in phase by 90°.

It follows that this kind of phase detector, provided it is followed by a low pass filter which completely smooths its output voltage, will produce a *linearly* varying output voltage as the phase is varied. This is exactly the same as the ideal phase detector characterised by equation (9.1). The value of K_d will be V_{cc}/π. The output voltage will not vary about zero however, but about $V_{cc}/2$, which is, of course, the reference level for all the circuits in the CD74HC4046A. The input amplifiers, A_1 and A_2, for example, have their inputs referred to $V_{cc}/2$, which is why the 2200 pF coupling capacitor, shown in Fig. 9.4, is needed.

The first experimental measurement that should be made on the CD74HC4046A is to determine its VCO characteristic. To do this, the +5 V power supply should be applied to pins 16 and 8, decoupled at the

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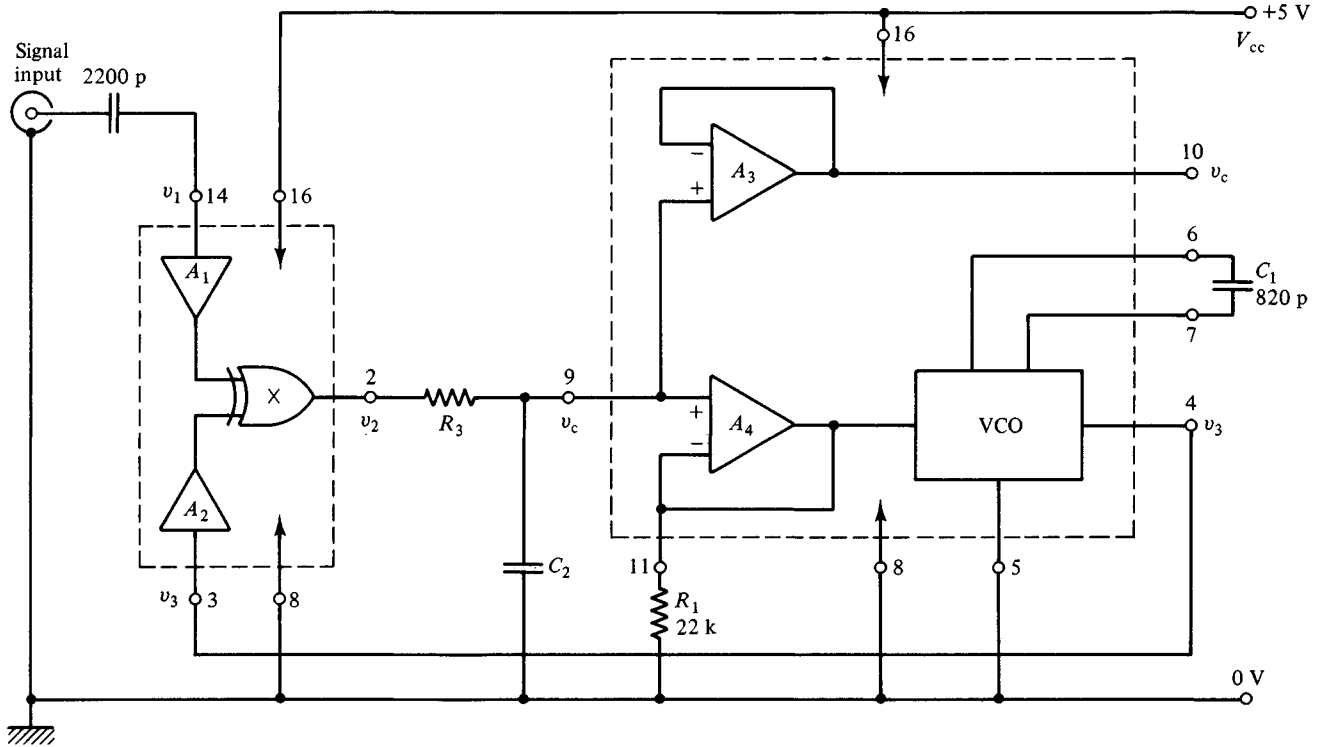

Fig. 9.4. The first experimental circuit using the CD74HC4046A. The VCO control voltage may be viewed on pin 10, which must be taken to ground through 10 kΩ.

device pins as usual, and pin 5 should be grounded to enable the VCO. The VCO is a relaxation oscillator which has a single timing capacitor, C_1, and its frequency is controlled by the current drawn from it by the output of A_4. The circuit details and waveforms of the VCO will be considered in section 9.13. The interest now is in the behaviour of this PLL as a system.

The choice of $C_1 = 820$ pF and $R_1 = 22$ kΩ, shown in Fig. 9.4, should make the free running VCO frequency close to 200 kHz. To observe this, omit the low pass filter, $R_3 C_2$ in Fig. 9.4, for the moment and take pin 9 to +2.5 V. A square wave of period close to 5 μs should be observed on pin 4, having a mark to space ratio very close to 1:1, and with a high level just below +5 V and a low level just above zero.

Now vary the voltage on pin 9 about the present level of 2.5 V. For small departures from +2.5 V, a fairly linear variation in frequency, with K_o close to 85 kHz/V, should be observed. When v_c approaches +4 V, or falls as low as +1 V, the characteristic becomes very non-linear, with K_o increasing considerably. The characteristic is shown in the data sheet [9] for various values of V_{cc}, and it is worthwhile examining this non-linear feature in some detail.

9.6 Inserting the low pass filter

The first experiments with the type I phase detector should be made with a simple *RC* low pass filter, of the kind shown in Fig. 9.4. The time constant, $C_2 R_3$, should be made very much greater than the free running period of the VCO. Such a choice makes it possible to assume that the control voltage, v_c, is effectively smoothed and is free from any ripple at the double frequency. The value $K_d = V_{cc}/\pi$ may then be attributed to the phase detector.

It will then follow that the natural resonant frequency of the PLL, given by equation (9.8), will be very low compared to the VCO frequency, and that the loop will be very lightly damped. For example, a choice of $R_3 = 47$ kΩ and $C_2 = 0.1$ μF will make $\omega_n/2\pi$ just over 2 kHz, or about 1% of the VCO centre frequency. The damping parameter, given by equation (9.9), will be less than 0.02. Nevertheless, closing the loop, to make up the complete experimental circuit shown in Fig. 9.4, will give a stable PLL and make possible some interesting measurements.

To begin with, set the input signal frequency to be at least 100 kHz higher, or lower, than the 200 kHz free running frequency of the VCO. View the VCO output, on pin 4, and the input signal with an oscilloscope. The timebase should be triggered from the input signal channel, Y_1. On first switching on the power supply, the display should show the input

signal, which should be a sine wave set to 200 mV peak. The VCO should appear as two lines across the display, because it is running at a completely different frequency to the input signal: changing the timebase trigger to Y_2 will show that the VCO is running at its free running frequency.

Now shift the input signal frequency slowly towards the VCO free running frequency. When the two frequencies almost coincide, the VCO square wave will suddenly appear on the display with its positive and negative going edges almost coincident with the input signal positive and negative peaks. The VCO is lagging the input signal by close to 90° and the loop is now in lock.

Confirm that a double frequency square wave is now present at the phase detector output and that pin 9 is, consequently, at +2.5 V. It is good practice always to view what is happening on pin 9 by looking at pin 10, that is through the buffer amplifier A_3. In some of the experiments that follow, it is very important to maintain pin 9 as a very high impedance input.

9.7 Observation of the capture process

Once the PLL of Fig. 9.4 is in lock, it will be possible to vary the input frequency over quite a wide range, at least 100 kHz–300 kHz, and observe the input sine wave and the VCO square wave staying locked together in frequency. Only the relative phase of these two signals will vary.

To begin to see the detail of what is happening, the VCO control voltage at pin 10 should be measured as a function of signal input frequency. Ideally, this should be done with a swept frequency source and an oscilloscope. The result should look something like that shown in Fig. 9.5. Once in lock, v_c will vary linearly as the input frequency varies, limited between +1 V and +4 V. These limits are determined by the values of v_c at which the VCO characteristic goes very non-linear, as the first experimental measurements, described in the previous section, have shown. If the input signal frequency goes outside the lock range, shown in Fig. 9.5, the output of the low pass filter goes to +2.5 V. This happens because the output of the exclusive OR gate, which is the input to the low pass filter, is then a square wave at the beat frequency between the input signal, at say 50 kHz or 350 kHz, and the free running VCO at 200 kHz.

Entering the lock range from outside, v_c will be seen to remain at +2.5 V until the input frequency gets very close to the VCO free running frequency. A small jump then occurs: negative going if the approach is from below, positive going if from above. These two small jumps are shown in Fig. 9.5 as defining the 'capture range', which is, in fact, very small with the component values shown in Fig. 9.4 and with $R_3 = 47\ \text{k}\Omega$

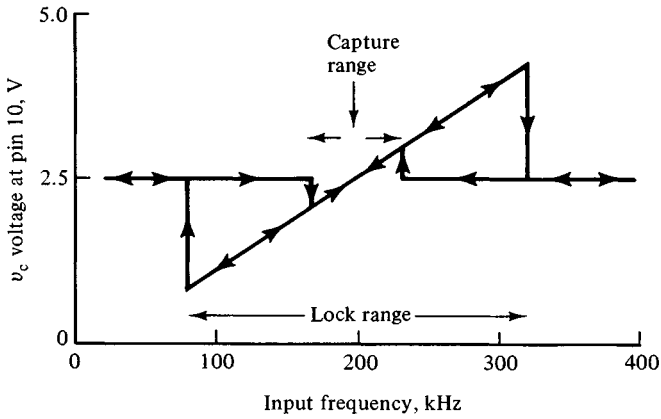

Fig. 9.5. Typical measurements of VCO control voltage as the input signal frequency to the PLL is varied slowly.

and $C_2 = 0.1\ \mu$F. For clarity, the capture range has been exaggerated in Fig. 9.5, and the figure also omits to show some small fluctuations, which will be seen on v_c, that indicate where the loop attempts to lock on input frequencies having some kind of harmonic relation to the free running VCO frequency. These harmonic relations may be very complicated and deserve close investigation.

The capture process is one of the most fascinating features of a PLL, and perhaps the most difficult to handle theoretically. Its complexity may be seen if v_c, the voltage at pin 10 in Fig. 9.4, is viewed with the oscilloscope on a timebase of about 1 ms/div, and on a sensitivity (a.c. coupled) of a few millivolts per division. Entering the lock range from outside, and approaching the VCO free running frequency, a very small sinusoidal signal will be observed, growing in amplitude and falling in frequency as the VCO free running frequency is approached. This is the beat frequency between the input signal and the VCO becoming low enough to pass through the low pass filter with less and less attenuation as its frequency falls.

Eventually, this fluctuation in v_c will be producing enough frequency modulation of the VCO to cause it, periodically, to approach the input signal frequency and, when this frequency modulation grows large enough, the PLL will lock on the input. Observation of v_c just before this happens will show how complex this behaviour really is. As the VCO free running frequency is approached, the waveform of v_c begins to depart radically from that of a sine wave, and develops a sharp cusp as the VCO frequency is pulled away from the input signal frequency. This is understandable because it is then that the rate of change of phase is at a

maximum. The waveform of v_c is distorted in the opposite way, its curvature is softened, as the VCO moves towards the input signal frequency, and the rate of change of phase is reduced. As the input signal frequency gets closer and closer to the VCO free running frequency, the distortion of v_c gets worse, its amplitude grows, and a large statistical component, or jitter, develops. Then, suddenly, the display collapses to a simple horizontal line as the PLL drops into lock. The theoretical treatment of this complex phenomenon is very interesting, and the book by Best [1] is a good guide to the literature. One paper which should be mentioned is Verrazzani's generalised study of the problem [10], as his paper includes a picture of the complex capture transient, showing $d\varphi/dt$ as a function of time.

9.8 Improving the loop damping

The very long time constant, $C_2 R_3$, which has been used up to now for the experimental circuit, shown in Fig. 9.4, has made possible some interesting observations of loop behaviour, but the loop is far too lightly damped to be of much practical use. The only exception would be an application that called for a loop with a 'flywheel' action: a loop that could tolerate a very short break in the input signal and yet stay in lock.

Glancing back at the closed-loop transfer function for a PLL with a filter of this simple kind, equation (9.7), shows that reducing CR will increase the loop natural resonant frequency, equation (9.8), and also increase the damping. This follows because substituting equation (9.8) into equation (9.9) gives the result

$$\alpha_1^2 = 1/2\pi K_o K_d CR. \tag{9.10}$$

As K_o and K_d are more or less constant, once the VCO free running frequency has been chosen, it would seem at first sight that the best tactic would be to reduce CR until $\alpha_1^2 = 2$, this being the value that gives maximally flat response in a second order system. This would be quite wrong, however, because the value of $C_2 R_3$ that would make $\alpha_1^2 = 2$ is just below 0.6 μs. Such a small time constant would offer virtually zero attenuation to the double frequency component coming from the phase detector when the PLL is in lock. There would be a very large component of ripple on the VCO control voltage, v_c, and this would certainly interfere with its action. A compromise value of $C_2 R_3$, in between the very large value of 4.7 ms, that is being used at the moment, and the obviously too small value of 0.6 μs, that equation (9.10) suggests, will give improved loop damping, a larger capture range, and still give enough filtering or

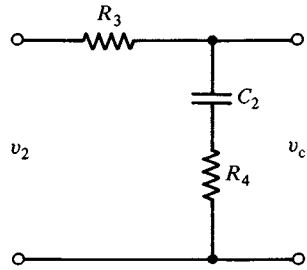

Fig. 9.6. The lead–lag filter. The component labels correspond to those in the CD74HC4046A data sheet [9], *and the input and output variables correspond to those shown in Fig. 9.3.*

smoothing on the phase detector output. Experiments along these lines are well worth while, but there is a better way to solve this problem, and that is to use a slightly more complicated filter. This is the kind shown in Fig. 9.6: the so-called lead–lag filter [11].

Some very simple algebra shows that the closed-loop transfer function for a PLL of the kind shown in Fig. 9.3, when the *RC* filter shown there is replaced with the filter shown in Fig. 9.6, is given by

$$\tilde{\varphi}_{\text{out}}/\tilde{\varphi}_{\text{in}} = \omega_{\text{n}}^2(1+sC_2R_4)/(\omega_{\text{n}}^2+\alpha_2\omega_{\text{n}}s+s^2) \tag{9.11}$$

in contrast to equation (9.7), where

$$\omega_{\text{n}}^2 = 2\pi K_{\text{o}}K_{\text{d}}/C_2R_3 \tag{9.12}$$

as before, and

$$\alpha_2 = 1/\omega_{\text{n}}C_2R_3+\omega_{\text{n}}C_2R_4 \tag{9.13}$$

now gives a measure of the damping.

Using the earlier values of ω_{n}, C_2 and R_2, the value of R_4 which will make $\alpha_2 = \sqrt{2}$, the value that should make the loop have a maximally flat response, comes out to be $R_4 = 1.2\,\text{k}\Omega$. This should be checked experimentally by using an FM signal source. With sinusoidal, and very low level, audio frequency FM on an input signal carrier at 200 kHz, the demodulated output may be observed on pin 10 as the modulating frequency is increased towards $\omega_{\text{n}}/2\pi$, which is about 2 kHz. This demodulated output should be a constant, at constant low level modulation, as the modulating frequency is increased, rolling off at 12 db/octave above $\omega_{\text{n}}/2\pi$ with negligible peaking. When $R_4 = 0$, in contrast, there is a very large resonance at $\omega_{\text{n}}/2\pi$.

There is quite a large ripple on the VCO control voltage, v_{c}, with this lead–lag filter, and this will be seen as a rectangular wave, of varying mark to space ratio, and at double the VCO frequency, superimposed upon the signal on pin 10. With the component values suggested above, the ripple is about 100 mV peak to peak.

The ripple may have a very important effect upon the behaviour of the PLL in that it will be responsible for increasing the apparent capture range. As the addition of R_4 has had no effect upon the value of ω_n, adding R_4 would not be expected to change the capture range from the very small value observed when $R_4 = 0$. In fact, with $R_4 = 1.2\ \text{k}\Omega$, a capture range of nearly 100 kHz may be observed with some samples of the CD74HC4046A. This kind of behaviour is found in many PLLs and is by no means a simple phenomenon.

A clue as to what is happening may be obtained by repeating the capture observations described at the end of section 9.7. With $R_4 = 1.2\ \text{k}\Omega$, no beat frequency between the input signal and the free running VCO will be observed just before capture, only a very complicated and constant amplitude ripple voltage. Now open the loop, by disconnecting the low pass filter from pin 9, and take pin 9 to $+2.5$ V, provided by a simple potential divider of two 10 kΩ resistors in series from V_{cc} down to ground. The VCO will now run at its centre frequency of 200 kHz. If a ripple voltage is now added to this $+2.5$ V, by simply connecting a square wave generator to pin 9, through a capacitor of 0.1 μF, the explanation for the wide capture range, discussed above, will be clear. A 100 mV amplitude square wave, varied around a frequency of 400 kHz, is quite enough to pull the VCO frequency from its centre frequency by a considerable amount. The reason for this lies, of course, in the circuit detail of the VCO, and will be discussed in section 9.13.

In applications where the PLL is used as a demodulator, the ripple on pin 10 is removed by a further low pass filter. This filter is not in the loop and, consequently, has no influence upon the loop dynamics.

9.9 The type II phase detector

The second type of phase detector which is available in the CD74HC4046A PLL is shown in Fig. 9.7. This is an example of the so-called charge–pump type of phase detector, and, although this term does not have quite the same meaning here as it had in section 8.3 the name is well chosen [12].

What Fig. 9.7, in fact, shows is a positive edge triggered phase detector. Assume that the D-type flip-flops are initially in the RESET state, and let the signal input to pin 14 lead the VCO input to pin 3 by a small angle φ. The positive edge of the input signal will clock the upper D-type flip-flop, shown in Fig. 9.7, to have its $\bar{Q}$ output low. The lower D-type flip-flop is still reset with its $\bar{Q}$ output high. Following through the signals from these two $\bar{Q}$ outputs to the gate of Q_1 shows that this p-channel MOST will have its gate low and will thus be on. At this stage both inputs to the NOR gate,

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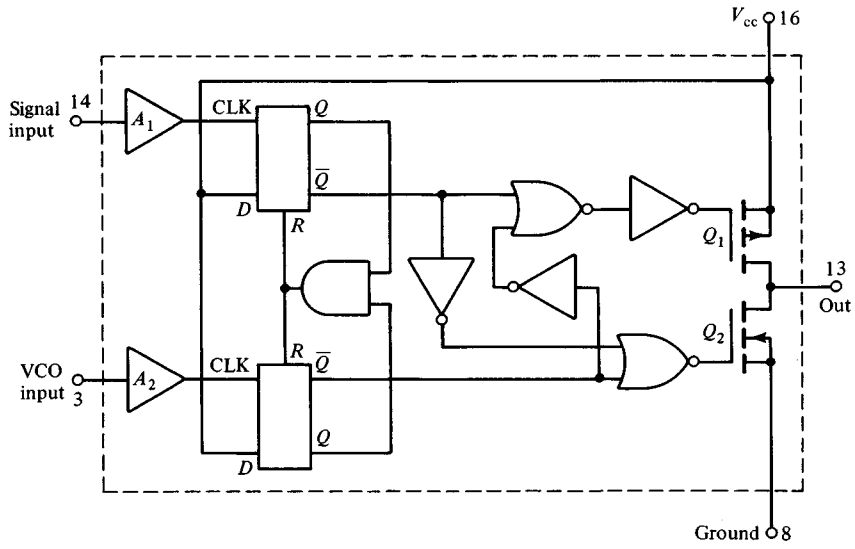

Fig. 9.7. Fig. 9.7. A block diagram of the type II phase detector in the CD74HC4046A. The figure has been adapted from the data sheet. A_1 and A_2 are the same limiting amplifiers previously shown in Fig. 9.4.

driving Q_2, are high, so that the gate of Q_2 is low, Q_2 is off, and the detector output, pin 13, is at V_{cc}.

When the positive going edge of the VCO clocks the lower D-type flip-flop, both flip-flops reset. Q_1 then goes off and Q_2 remains off. The output, pin 13, is now a very high impedance.

The opposite happens when the VCO leads the input signal. It is then Q_2 which turns on for the short time between the arrival of the positive edge on pin 3 and the positive edge on pin 14. During this time the output, pin 13, is held at ground. In fact, the output is a TRI-STATE (a trademark of the National Semiconductor Corp., as Horowitz and Hill point out [13]). Fig. 9.8 makes this clear: the type II phase detector in the CD74HC4046A may be represented by a three position switch which connects pin 13 to V_{cc}, or to ground, or to just an open circuit.

Fig. 9.8 is the second experimental circuit for this chapter, and shows the CD74HC4046A connected up to run with the type II phase detector, and with the kind of low pass filter that is needed. In fact, Fig. 9.8 is just a simple modification of Fig. 9.4: new values must be worked out for R_3, C_2 and R_4, and pin 13 used to input the low pass filter instead of pin 2. Everything else is as before.

To work out the correct values for R_3, C_2 and R_4, consider the loop to be in lock with an input signal at the VCO centre frequency, which is again

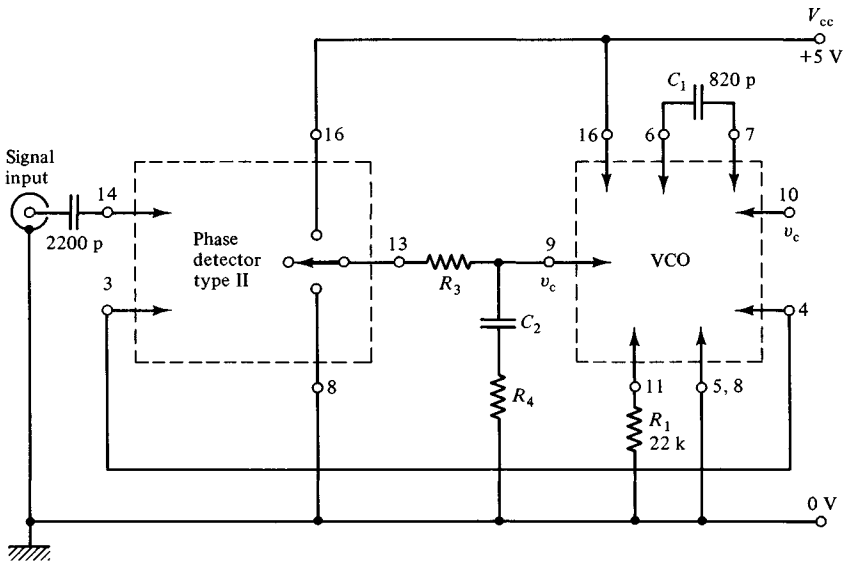

Fig. 9.8. *The experimental circuit using the CD74HC4046A with its type II phase detector.*

200 kHz. Under such conditions, $v_c = V_{cc}/2$, and the phase detector is an open circuit: the switch representing the phase detector TRI-STATE output is in the position shown in Fig. 9.8. $V_{cc}/2$ is stored on capacitor C_2, and remains there because of the very high input impedance to pin 9.

Now suppose that the input signal is increased very slightly in frequency. This means that the input signal now leads the VCO by the small angle φ, discussed above, and if the VCO does not follow, by also going to a higher frequency, φ will simply increase. The switch shown in Fig. 9.8, however, does not remain in the centre position but moves to the upper position for a time $(\varphi/2\pi)T$, where T is the period of the input signal.

When this happens, provided $R_4 \ll R_3$, the resistor R_3 has V_{cc} at its input end, pin 13, and $V_{cc}/2$ at its output end, pin 9. A current $V_{cc}/2R_3$ will thus flow for the short time, $(\varphi/2\pi)T$, that the switch remains in the upper position, and a charge, $(V_{cc}\varphi/4\pi R_3)T$, will be transferred to C_2, increasing the voltage across C_2 by a small amount. The frequency of the VCO will then increase, and the VCO will begin to move back into phase with the incoming signal.

The transfer function, $\tilde{v}_c/\tilde{\varphi}$, of the type II phase detector and its filter can be found by noting that the *mean* current flowing in R_3 must be $V_{cc}\varphi/4\pi R_3$. As v_c, the VCO control voltage, is simply the result of this

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current flowing through the impedance formed by C_2 and R_4 in series, it follows that

$$\tilde{v}_c/\tilde{\varphi} = V_{cc}(1+sC_2R_4)/4\pi sC_2R_3. \tag{9.14}$$

As φ may be taken as the input variable, φ_{in}, in the same way as in the previous analysis involving Fig. 9.2, and as the change in the VCO frequency, $\Delta f = d\varphi_{out}/dt = 2\pi K_o v_c$, it follows that

$$\tilde{\varphi}_{out}/\tilde{v}_c = 2\pi K_o/s \tag{9.15}$$

which again expresses the integrating action of the VCO, noted above after equation (9.3).

Multiplying equations (9.14) and (9.15) then yields the open-loop transfer function for the PLL shown in Fig. 9.8. Using equation (9.6) then gives the closed-loop transfer function as

$$\tilde{\varphi}_{out}/\tilde{\varphi}_{in} = \omega_n^2(1+sC_2R_4)/(\omega_n^2+\alpha_3\omega_n s+s^2) \tag{9.16}$$

which should be compared with equation (9.11): the transfer function for the PLL which used the type I phase detector with the same kind of filter now being used with the type II phase detector.

In equation (9.16), the loop natural resonant frequency is given by

$$\omega_n^2 = K_o V_{cc}/2C_2R_3 \tag{9.17}$$

while the loop damping is now given by

$$\alpha_3 = \omega_n C_2 R_4. \tag{9.18}$$

In contrast to the PLL which uses the type I phase detector, this charge–pump PLL has no damping when $R_4 = 0$. This is clear when equation (9.18) is compared with the earlier result, equation (9.13).

9.10 Experiments with the type II phase detector

Comparison of equations (9.12) and (9.17), bearing in mind that K_d was equal to V_{cc}/π for the type I phase detector, shows that C_2R_3 should be reduced to 25% of its previous value if the same value of ω_n is to be obtained with the type II phase detector. A suitable choice is $R_3 = 120\ \text{k}\Omega$ and $C_2 = 0.01\ \mu\text{F}$, making $C_2R_3 = 1.2$ ms in contrast to the earlier 4.7 ms. Further calculations, using equation (9.18), show that $\alpha_3 = \sqrt{2}$, the condition for a maximally flat loop response, when $R_4 = 10\ \text{k}\Omega$.

Such a large value of R_4 may cause problems with this PLL. The loop may appear to lock over a very wide range, the same range of at least 100–300 kHz found previously for the type I phase detector, but close examination of the VCO and input signal waveforms may show that a

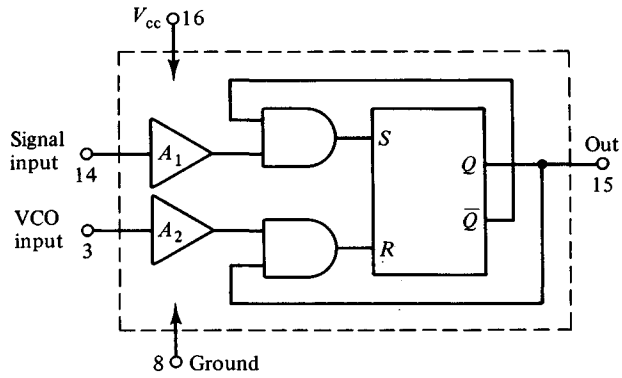

Fig. 9.9. A block diagram of the type III phase detector in the CD74HC4046A. The figure has been adapted from the data sheet [9]. *Again, A_1 and A_2 are the limiting amplifiers first shown in Fig. 9.4.*

considerable jitter exists between the two. The reason for this will be clear when the VCO control voltage is viewed, on pin 10, using a sensitive oscilloscope on a.c. Sharp voltage spikes of alternate polarity may be observed, showing that the VCO frequency is 'hunting' about the correct value. This is not because of incorrect system damping, but because the voltage spikes are interfering with the action of the VCO.

Reducing R_4 will cure this problem, at the expense of making the PLL rather lightly damped. A value of $R_4 = 2.2\ \text{k}\Omega$ is suitable. The same experimental program, described above for the type I phase detector, may then be followed. The capture range for this type II phase detector will be found equal to the lock range, and jitter, once in lock, should be really negligible. When the PLL is just on the point of capture, a lightly damped transient oscillation should be seen periodically on pin 10. This is the transient discussed by Gardener [12] and is shown in his paper as Fig. 10. Once in lock, the VCO control voltage is very free from ripple with this type II phase detector.

9.11 The type III phase detector

The third type of phase detector which is available on the CD74HC4046A is shown in Fig. 9.9. This is a positive edge triggered *RS* flip-flop, and it is clear that the output, from pin 15, will go to V_{cc} when the positive going edge of the signal input arrives, and then be reset to zero when the positive going edge of the VCO arrives. The initial state is assumed to be $\bar{Q} = 1$.

This type III phase detector thus needs a low pass filter in order to provide a VCO control voltage, v_c. This control voltage will be just above

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zero when the input leads the VCO by a small angle, increasing linearly towards V_{cc} and φ increases towards 2π. Should φ exceed 2π, v_c, will fall back at once to near zero: the output from this type III phase detector, when the PLL slips out of lock, is a sawtooth waveform, whereas the type I phase detector produces a triangle waveform.

It follows that the theory for a PLL using a type III phase detector is just the same as that for type I, except that K_d should be given the value $V_{cc}/2\pi$ instead of V_{cc}/π. When in lock, at the VCO centre frequency, $\varphi = \pi$ with the type III phase detector. Ripple on the VCO control voltage is more of a problem with the type III phase detector, because it is at the signal frequency, not double the signal frequency. The capture process with a type III phase detector is most interesting because, when the PLL is not in lock, the VCO free running frequency does not take up the value corresponding to $v_c = +2.5$ V, as it does with a type I phase detector. This should be looked at carefully. A further complication is that a PLL using a type III phase detector can lock on input signals having some harmonic relationship to the VCO. This is the same kind of behaviour, noted above, found with the type I phase detector.

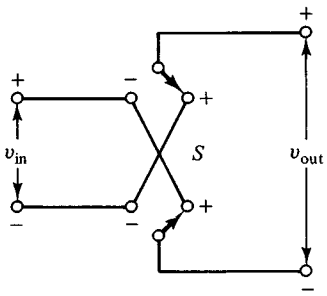
9.12 Circuit shapes for phase detectors

The three types of phase detector in the CD74HC4046A are members of three classes into which virtually all analog phase detectors may be placed.

Classification of a phase detector as type I implies the exclusive OR function, which is identical to analog multiplication. When this is followed by a low pass filter, the detector has the characteristic given by equation (9.1) and the PLL will lock over the range $0 < \varphi < \pi$, always provided that both input and VCO signals have 50% duty cycles.

Classification of a phase detector as type II implies the charge–pump mode of operation. A capacitor is charged repetitively with very short pulses of current when the input signal is above the VCO frequency, and repetitively discharged when it is below. This type of phase detector does not need signals with a 50% duty cycle, and it ignores input signals which are harmonically related to the VCO. A real advantage of the type II phase detector is that its output is virtually ripple free when the loop is in lock.

Classification of a phase detector as type III implies the positive edge triggered set–reset mode of operation. After low pass filtering, this phase detector provides an output which varies linearly over the range $0 < \varphi < 2\pi$. It can handle inputs of any duty cycle.



v_{in}	S	v_{out}
+	+	−
−	+	+
+	−	+
−	−	−

Fig. 9.10. A simple change-over switch effects the exclusive OR function. Switch positions are labelled + and −, while the same labels are used to define the polarity of input and output signals.

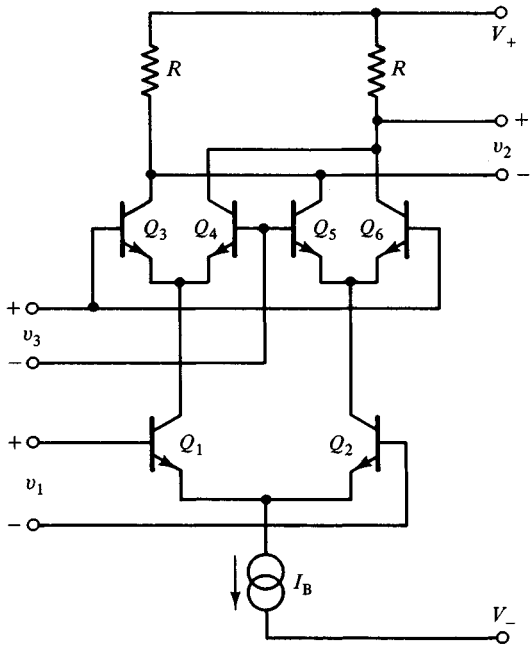
These three classes of phase detector may now be considered from the point of view of their circuit shapes. The exclusive OR function, which forms the basis of the type I phase detector, may be realised with the simple change-over switch circuit shown in Fig. 9.10 When the switch positions are labelled + and −, and the same symbols are used to define the polarity of the input and output, the truth table shown in Fig. 9.10 confirms the exclusive OR property of this simple circuit.

The same change-over switch topology, or circuit shape, is found in a well-known four quadrant multiplier circuit, first described in 1968 by the simultaneous publications of Bilotti [14] and Gilbert [15]. This circuit is shown in Fig. 9.11, and, again, the adjoining truth table shows the 'if only v_1 or only v_3 is positive, then v_2 is positive' function essential to the exclusive OR. The reason for this circuit property, however, lies in the cross connection of Q_3, Q_4, Q_5 and Q_6. These four transistors play the same role as the switch contacts in Fig. 9.10.

The circuit shown in Fig. 9.11 is at the heart of many integrated circuit analog multipliers [16], and its use as a phase detector in an early PLL has been dealt with in detail by Gray and Meyer [17].

A second example of a type I phase detector, which has the same circuit shape as the simple change-over switch shown in Fig. 9.10, is shown in Fig. 9.12. Four diodes are used in this case as the four contacts which are needed to implement a change-over function. This is quite an old idea in electronics, often referred to as a ring demodulator [18].

The particular circuit shown in Fig. 9.12 would have a VCO signal of several volts applied to the v_3 input, but the signal input to v_1 would be small compared to a forward diode drop. The circuit then functions with D_1 and D_3 turning on during the positive half cycle of the VCO, while D_2 and D_4 turn on during the negative half cycle. When there is no



v_1	v_3	v_2
+	+	−
−	+	+
+	−	+
−	−	−

Fig. 9.11. *The four quadrant analog multiplier circuit which is often employed as a type I phase detector.*

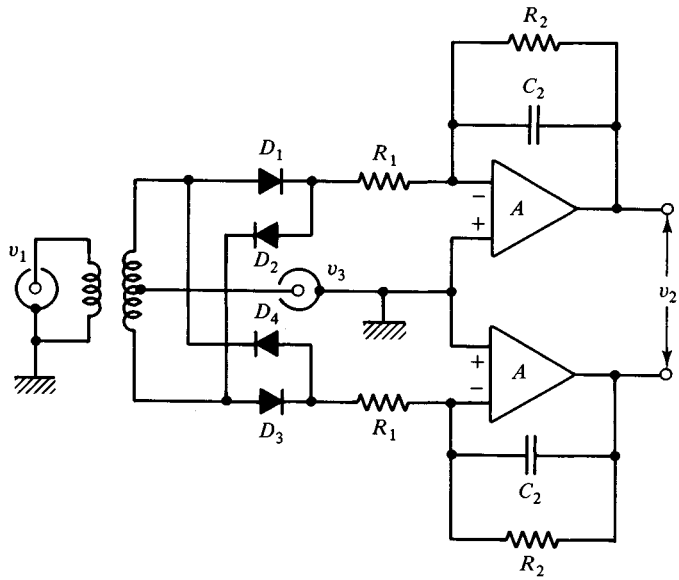


Fig. 9.12. *A schematic circuit diagram of a type I phase detector using diodes in a change-over switch mode. As in Fig.* 9.1, v_1 *would be the signal input,* v_3 *the VCO, and* v_2 *the output.*

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component of v_1 in phase with v_3, the output, v_2, will be zero, because the demodulator is balanced. When v_1 is in phase with v_3, the output will be negative, and when v_1 lags or leads v_3 by π, the output will be positive. The actual value of the differential output depends upon the turns ratio of the input transformer, which would usually be $1:1+1$ because it would be a trifilar wound wide-band transformer on a toroid core. The two amplifiers shown in Fig. 9.12 have transfer functions $-R_2/R_1(1+sC_2R_2)$, the same low pass filter characteristic given previously in equation (9.4), but now with the additional possibility of some gain: R_2/R_1. The actual value of R_1 may also be chosen to provide the desired input impedance for v_1 and v_3.

It is interesting to note that there is another very well-known circuit [19], of exactly the same *circuit shape* as the circuit shown in Fig. 9.12, and this is also a type I phase detector but it works on a completely different principle. This circuit is shown in Fig. 9.13.

Fig. 9.13 shows exactly the same 'ring' connection of four diodes as Fig. 9.12: in both cases the four diodes are connected in a closed ring, all forward conducting in the same direction around this ring. Fig. 9.12 was drawn in such a way that the ring was somewhat obscured, and this was done to bring out the change-over switch topology. The circuit shown in Fig. 9.13 does not operate like a change-over switch at all. The high level input to this phase detector, the local oscillator, v_3, is now applied so that *adjacent* diodes, D_1 and D_2 followed by D_3 and D_4, are turned on every half cycle. In the circuit shown in Fig. 9.12, diodes *opposite* one another are turned on: D_1 and D_3 in one half cycle, D_2 and D_4 in the text.

The local oscillator level, in the circuit shown in Fig. 9.13, is set so that the forward current in the diodes makes them present an impedance at the local oscillator input socket which is a reasonable match. The signal input transformer then has a secondary load consisting of two forward biassed diodes and two reverse biassed diodes in a series–parallel combination. As the forward biassed diodes will be mainly resistive, and the reverse biassed diodes mainly capacitive, this load impedance may be designed to give a good match at the signal input socket, over quite a wide range of frequency, by making use of the transformer leakage inductance to resonate with the diode capacitance. It follows that this circuit is used for VHF applications.

The output from the circuit shown in Fig. 9.13 comes from the centre tap of the local oscillator transformer. There will be no output when the input signal is at the local oscillator frequency, and also lagging or leading the local oscillator by $\pi/2$. This follows because the circuit will be balanced under these conditions. A signal input at a frequency other than the local oscillator frequency, or one which has a component in phase with

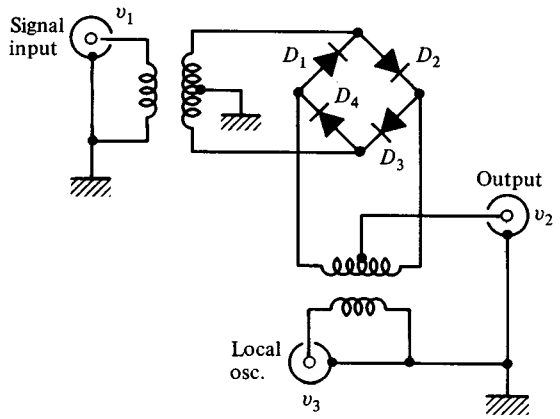

Fig. 9.13. *The ring, or balanced, mixer which is used at VHF. This works on quite a different principle to the previous circuit, shown in Fig.* 9.12, *although it has the same circuit shape.*

the local oscillator, will produce an output because it will unbalance the circuit. For example, if D_1 and D_2 were forward biassed by the local oscillator, a signal input which was in phase with the local oscillator would decrease the current in D_1 but increase the current in D_2. Then D_1 would have a higher resistance than D_2, because of the non-linear forward characteristic of these diodes, and an output would result. This output would be at the double frequency, plus a constant level, characteristic of a type I phase detector. The two circuits, shown in Figs. 9.12 and 9.13, are both type I phase detectors, and both have the same circuit shape, but they work on quite different principles, because the signal levels and the input and output connections are quite different. This is something to look out for in electronic circuit design.

Turning now to the type II, or charge–pump type, phase detector, the schematic block circuit diagram, Fig. 9.7, shows how this kind of phase detector may be realised with standard logic gates and flip-flops. The TRI-STATE output circuit, shown in Fig. 9.7, is also a standard feature in all logic families.

An interesting paper by Yaeger [20] describes a charge–pump phase detector using bipolar transistors, in contrast to the MOSTs of Fig. 9.7, but the logic driving these bipolar devices is virtually the same in both designs. Yaeger's paper is particularly useful in that it tackles the problem of compensating for the changing closed-loop transfer function of a PLL when this is used in a frequency synthesizer. Frequency synthesis with a PLL involves a high frequency VCO followed by a frequency divider [2]. The phase detector deals with the lower frequency output of the divider,

which is made to lock on to a low frequency crystal oscillator. As the division ratio is changed, to obtain different output frequencies, so does the effective value of K_o, and hence the loop gain of the PLL. Type II phase detectors are a good choice for frequency synthesizer applications, because of the wide capture range which is possible. Yaeger adds a further advantage, by slight modification of the TRI-STATE output circuit, which enables the current pulse it supplies to be varied in magnitude, and thus compensate for the changes in K_o, mentioned above.

Finally, type III phase detectors may be considered, along with a few other circuit ideas for phase detectors which have been proposed.

Fig. 9.9 shows a schematic block diagram of the type III phase detector used in the CD74HC4046A. This is implemented with standard logic gates and flip-flops. The whole point of the type III phase detector, as was summarised at the beginning of this section, is its ability to handle a variation in phase over the full range of zero to 2π. This means that the output from the low pass filter, which must be used with this type of phase detector, is a saw-tooth wave when the phase angle is increasing continuously, at a sufficiently slow rate for the low pass filter to follow, whereas the output from a type I phase detector, under the same conditions, is, of course, a triangle wave. Response over the full range, 0–2π, has advantages in some applications, and an interesting way of realising such a type III phase detector, which is quite different to that shown in Fig. 9.9, has been published by Fyath [21].

There are a number of other circuit ideas for phase detectors which have been published. These may be simplifications of some of the ideas which have already been dealt with here. For example, a phase detector identical to the one shown in Fig. 9.12, but with diodes D_2 and D_4 omitted, is a classical circuit shape for a phase detector [22]. Such a 'half wave' realisation has obvious disadvantages. Another apparent simplification of one of the circuits which has been treated above is the phase detector published by Soyuer and Meyer [23]. This is identical to the circuit shown in Fig. 9.11, except that Q_5 and Q_6 are omitted, and the collector of Q_2 is taken directly to V_+. The output from the circuit, v_2 in Fig. 9.11, will then be zero when v_1 is negative: the v_2 column in the truth table shown in Fig. 9.11 becomes $-0+0$, instead of $-++-$, as it is with the completely balanced circuit. Soyuer and Meyer were able to show that such a phase detector would have better dynamic performance, in a PLL with a square wave VCO, for both deterministic and random input signals.

The review of phase detectors, which has been given in this section, is incomplete and has been restricted to circuits which are really analog phase detectors. No mention of the fully digital phase detectors,

considered briefly in section 9.2, has been made in this section, but these are of great importance in digital PLLs, and the reader is again referred to Best's work on this topic [7].

9.13 Circuit shapes for voltage controlled oscillators

The VCO in the CD74HC4046A, the device that was used for the experimental work in this chapter, is built up from the standard logic blocks which are available in CMOS. Fig. 9.14 shows the circuit detail of the VCO from this logic block point of view. The pin numbers in Fig. 9.14, and the amplifier A_4, are the same as in Fig. 9.4, where the complete CD74HC4046A was shown. This circuit detail may be inferred from the data sheet [9] and from an excellent application note [24] which was written for an earlier CMOS PLL: the CD4046A.

The action of the VCO shown in Fig. 9.14 may be understood, and examined experimentally, if pin 9 is taken to $V_{cc}/2 = +2.5$ V, pin 5 is grounded, to put the clock input of the *JK* flip-flop up at $V_{cc} = +5$ V and enable the VCO, and $C_1 = 820$ pF and $R_1 = 22$ kΩ as before. The amplifier A_4 then establishes a current $V_{cc}/2R_1$ (about 115 μA) in Q_1.

The oscillator part of the circuit shown in Fig. 9.14 is made up of Q_3–Q_6, C_1 and the *JK* flip-flop. The flip-flop ensures that either Q_3 and Q_6 are on (and Q_5 and Q_4 off), or that Q_5 and Q_4 are on (and Q_3 and Q_6 off). In the former case, pin 7 will be held just above ground while pin 6 will rise at a constant rate, $dv/dt = I/C_1$, where I is the current in Q_2. Now Q_1 and Q_2 form a current mirror, but the area of Q_2 is about five times that of Q_1. This means that the current, I, available to charge up C_1, is about 500 μA, so that I/C_1 will be about 0.6 V/μs when $C_1 = 820$ pF.

The voltage on pin 6 will be observed to rise linearly at about this rate until it reaches a level close to 1.4 V. The K input on the *JK* flop-flop is then triggered, resetting $\bar{Q}$ high and Q low. This turns on Q_4 and turns off Q_6. The current in Q_2 is now directed, though Q_5, into C_1 again, but in the opposite direction to that of the previous situation. The waveforms actually observed are sketched in Fig. 9.15.

Fig. 9.15 shows that, during the time that Q_6 is on, pin 7 is not exactly at zero but positive by a small amount, due to the current in Q_6 causing a small drop across it. The same applies when it is the turn of Q_4 to be on: pin 6 is slightly positive. What may be unexpected in Fig. 9.15 is the asymmetry of the waveforms: if C_1 charges up to the +1.4 V shown in Fig. 9.15, why does the waveform not begin at −1.4 V and pass through zero at the quarter period? The answer to this question lies in the structure of Q_4 and Q_6 in the CMOS process. The drains of these two n-channel

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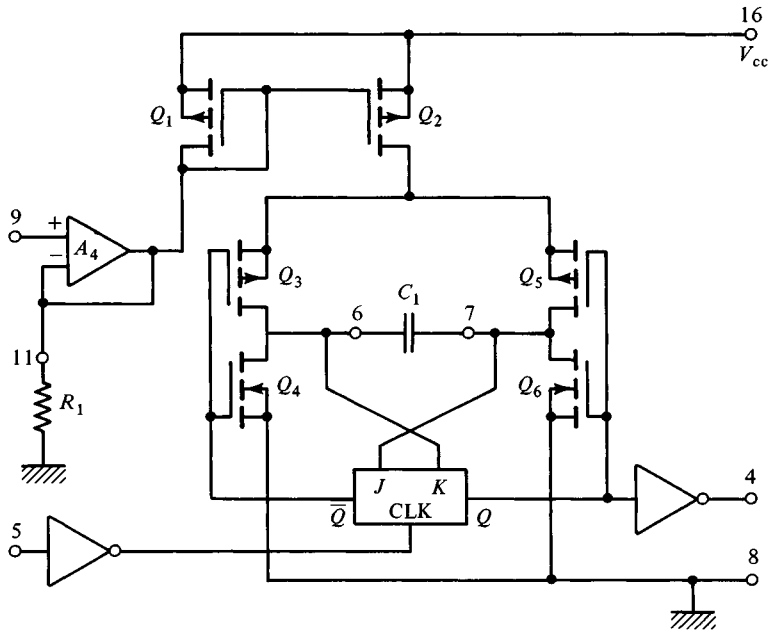

Fig. 9.14. The essential circuit detail of the VCO in the CD74HC4046A.

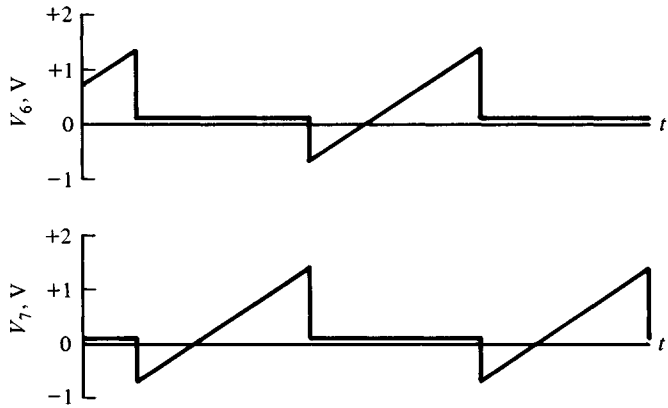

Fig. 9.15. The waveforms that will be observed on pins 6 and 7 of the CD74HC4046A.

MOSTs must be n-type regions of silicon in a p-type substrate which, as Fig. 9.14 shows, is grounded. It follows that this np intrinsic diode will 'catch' if any attempt is made to drive the drain below about −0.7 V. The intrinsic diode discharges C_1 a certain amount each half cycle, and this is another factor (the first being the current multiplication of Q_1 and Q_2) that makes this VCO operate at a higher frequency than would be expected

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from a first glance at the circuit and a note of the values chosen for C_1 and R_1. For this reason it is interesting to experiment with smaller values of C_1 and R_1, taking the operating frequency towards the 18 MHz maximum given on the data sheet, and observing and understanding the changes which occur in the waveforms.

At the end of section 9.8, attention was drawn to the problem of the ripple on the VCO control voltage that may have to be tolerated in some PLL designs. In an experiment, which was suggested in section 9.8, an externally generated square wave ripple voltage was injected at pin 9, on a free running VCO in a CD74HC4046A, and this was found to pull the oscillator frequency.

The circuit detail shown in Fig. 9.14 suggests why a ripple voltage on pin 9 might influence the VCO in this way. A sudden increase in the voltage at pin 9 would produce only a discontinuity in the *slope* of the ramp across C_1, if Q_4 and Q_6 had really zero resistance, and if C_1 were really a perfect capacitor. This is not the case, however, and a step increase in the voltage at pin 9 must produce a step increase, or, even more important, a voltage spike, at pins 6 or 7. This may trigger the *JK* flip-flop early, and thus increase the operating frequency so that the VCO locks on to the ripple voltage. Similarly, a step decrease in the voltage at pin 9 may produce synchronisation at frequencies below the free running frequency. All these possibilities may be examined experimentally with the CD74HC4046A. It is important to note that the same problem arises with virtually all VCO designs.

Fig. 9.16 shows a VCO circuit which is a classical circuit inasmuch as it was used in a whole series of very successful bipolar PLLs, the NE560, 561 and 562, introduced by Signetics in 1971 [25]. This circuit, which is dealt with in detail by Gray and Meyer [26], has much in common with the previous VCO, shown in Fig. 9.14. In both circuits, the capacitor, C_1, is being charged with a constant current, first from one side and then the other. The output from the VCO shown in Fig. 9.16 is the square wave developed across R_1 and R_2, the voltage level there being clamped by Q_1 and Q_2.

This rather crude voltage clamping is replaced by much better technique in the current bipolar PLL of the 560 series: the NE564 [27]. This device, which can operate up to 50 MHz, uses simple resistors in place of $Q_1 R_1$ and $Q_2 R_2$, shown in Fig. 9.16, and there is an arrangement of current sinks which maintains a constant current in these resistors as the capacitor current is varied to change frequency. This results in a great improvement in the temperature stability of the VCO centre frequency. An important paper by Gilbert [28] reviews developments in this field, and lists the

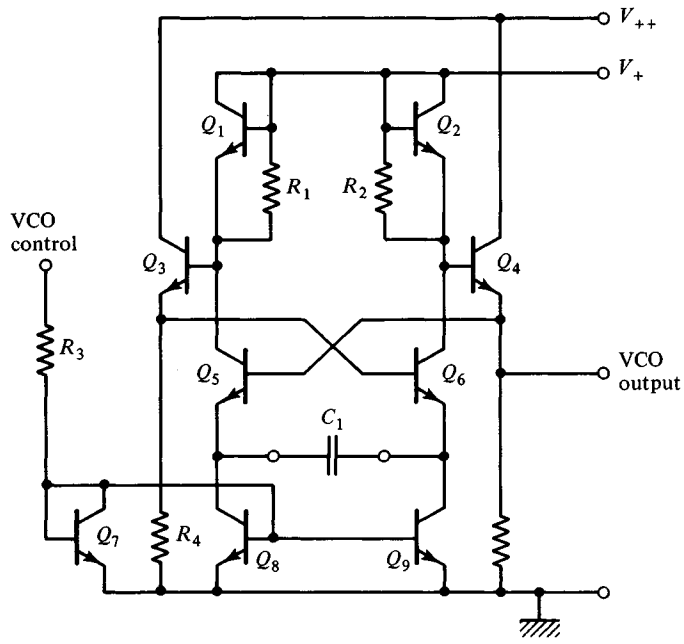

Fig. 9.16. A simplified circuit diagram of the VCO in the classic NE560 PLL.

advantages of the astable multivibrator circuit, of which Figs. 9.14 and 9.16 are examples. Gilbert's solution, to the temperature dependence problems of this circuit, is to use a subtle arrangement of a bandgap reference and diode switches. His paper is a good guide to the foundation literature in this area of electronic circuit design.

Developments in integrated circuit PLLs have taken the technique into the VHF region. A device fabricated with a 2 μm CMOS process can be used up to 128 MHz [29] and the device described by Soyuer and Meyer [23], referred to in the previous section, can operate up to 350 MHz. This latter device was fabricated with a 2 μm bipolar process, and was interesting in that it used a varactor tuned VCO with a high Q LC resonator. This meant an external inductor had to be used with this device, but, because of the high Q possible with this technique, a very small noise bandwidth for the resulting PLL could be obtained.

9.14 Conclusions

This chapter began with a review of PLL theory, which was supported by a series of experimental circuits built around the CD74HC4046A device. This made it possible to introduce the three most commonly used kinds of

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phase detector found in analog PLLs and discuss the low pass filters which must be used with these different kinds of phase detector.

In all these cases, the behaviour of the PLL is best examined by looking at the way in which the VCO control voltage changes as the frequency of the input signal is varied. Fig. 9.5 shows one particular example. Measurements along these lines show up all the complicated behaviour of a PLL as it drops into lock, either with the expected signal, or with one which may be quite unexpected in that it has some harmonic relationship to the VCO frequency at that particular instant.

The charge–pump, or type II, phase detector is perhaps the most interesting one to be looked at here. It provides a very wide capture range, and, when the low pass filter is designed correctly, the PLL is very stable and jitter free. A further advantage of the type II phase detector is that it makes the loop sensitive only to input signals which lie within the tuning range of the VCO.

The chapter continued with a look at the circuit detail, the circuit shapes and circuit ideas, found in phase detectors and VCOs. In the case of phase detectors, circuit shapes have remained very much the same over a very long period of time. Developments in this area have clearly been in device performance: higher speeds and better device matching, both the result of advances in process technique.

Circuit development for VCOs appears to be more circuit shape, or circuit idea, directed. This is clear when the early 560 circuits [25] are compared with the far more complex 564 circuit [27], or with a more recent device [29]. All use the basic astable multivibrator circuit shape, shown in Figs. 9.14 and 9.16, but advances have been made by adding compensating circuits, or more accurate level references. There have also been new developments in the way that the VCO problem may be tackled, which have not been discussed here in connection with PLLs because the VCO for a PLL must have a very fast response to a change in its input control voltage. These new developments have been called 'precision charge dispensing' techniques by Gilbert [28], and are used, for example, in the AD651 voltage to frequency converter [30]. The charge dispensing technique is similar to the method described here, in chapter 8, to obtain an ultra-linear VCO. This was done by using a charge–pump frequency to voltage converter as a feedback element across a crude VCO, and resulted in the experimental circuit shown in Fig. 8.6. Such an ultra-linear VCO, which also has remarkable stability against changes in temperature, does not have the speed of response called for in most PLL applications.

Notes

1 Best, R. F., *Phase-Locked Loops: Theory, Design and Applications*, McGraw Hill, New York, 1984.
2 Egan, W. F., *Frequency Synthesis by Phase Lock*, John Wiley, New York, 1981.
3 de Bellescize, H., *L'Onde electrique*, **11**, 209–72, 1932.
4 Tucker, D. G., and Ridgway, J. F., *Electronic Engineering*, **19**, 75–6, 238, 241–5, 276–7, 366 and 368, 1947.
5 Horowitz, P., and Hill, W., *The Art of Electronics*, Cambridge University Press, Cambridge, second edition, 1989, pp. 641–55.
6 Gray, P. R., and Meyer, R. G., *Analysis and Design of Analog Integrated Circuits*, John Wiley, New York, second edition, 1984, pp. 605–34.
7 Note 1 above, pp. 89–96.
8 Note 6 above, p. 528.
9 RCA Data File No. 1854.
10 Verrazzani, L., *IEEE Trans. Aero. Electr. Syst.*, **AES-14**, 329–33, 1978.
11 Note 5 above, p. 648.
12 The term may have come into wide use after the publication of F. M. Gardener's review: Charge–pump phase-lock loops, in *IEEE Trans. Comm.* **COM-28**, 1849–58, 1980. Gardener is also author of the classic *Phaselock Techniques*, John Wiley, New York, second edition 1979.
13 Note 5 above, p. 487.
14 Bilotti, A., *IEEE J. Sol. St. Circ.*, **SC-3**, 373–80, 1968.
15 Gilbert, B., *IEEE J. Sol. St. Circ.*, **SC-3**, 365–73, 1968.
16 For example, the Analog Devices AD530 series, the Motorola MC1459L, and the RCA CA3091D.
17 Note 6 above, pp. 622–32.
18 For example, by Tucker and Ridgeway, who used the ring demodulator as a phase detector in one of their circuits back in 1947. See note 4 above, p. 277.
19 Skolnik, M. J., *Radar Handbook*, McGraw-Hill, New York, 1970, p. 5.42.
20 Yaeger, R., *RCA Review*, **47**, 78–87, 1986.
21 Fyath, R. S., *Electronic Engineering*, **59**, No. 726, 28, 1987.
22 Greenwood, I. A., Holdam, J. A., and Macrae, D., *Electronic Instruments*, McGraw-Hill, 1948, p. 384.
23 Soyuer, M., and Meyer, R. G., *IEEE J. Sol. St. Circ.*, **SC-24**, 787–95, 1989.
24 The RCA COS/MOS phase-locked-loop. A versatile building block for micropower digital and analog applications. ICAN 6101. In: *COS/MOS Integrated Circuits*, RCA Solid State Data Book, SSD 250C, 1983, pp. 714–17.
25 Grebene, A. B., *IEEE Trans. Broadcast and Television Receivers*, **BTR-17**, 71–80, 1971.
26 Note 6 above, pp. 628–31.
27 For the circuit diagram of this device, see the Data Brief in *Radio and Electronics World*, pp. 49–51, Nov. 1983.
28 Gilbert, B., *IEEE J. Sol. St. Circ.*, **SC-11**, 852–64, 1976.
29 Kato, K., Sase, T., Sato, H., Ikushima, I., and Kojima, S., *IEEE J. Sol. St. Circ.*, **SC-23**, 474–84, 1988.
30 *1986 Update and Selection Guide*, Analog Devices Inc., Massachusetts, pp. 3.137–3.152.