Chapter 14

Switched Capacitor Circuits

14.1 Introduction

To meet the advances in technology, realization of monolithic electronic analog filters became an important issue. In the beginning, the problem of inductance realization was solved through its simulation using active RC circuits. However, integration needed the solution of a few more problems such that the realized filters perform as close to the design as possible. One of the main issues faced while integrating circuits was the amount of tolerance in passive elements; it was too large. This large tolerance resulted in large errors in the realized filter parameters. These errors could be reduced through electronic tuning of components or the tuning of filter parameters, with an obvious increase in circuit complexities. It was observed that the need of electronic tuning could be reduced through schemes in which filter parameters depend on the ratio of passive components, especially capacitors, as capacitor ratio tolerance is much better in integrated circuits. Switched capacitor filter (SCF) realization technique is one such scheme in which all filter parameters depend on capacitor ratios. Equally important is the fact that switched capacitor (SC) schemes do not use external resistors. This saved a large amount of chip area; a highly attractive feature for integrated circuits.

In this chapter, the basic concepts of SCF realization will be discussed. One important approach is the simulation of grounded and floating resistors using capacitors, switches, and non-overlapping clock signals. Such a realization and its simple applications including integrators are shown in Sections 14.2 and 14.3. As switches and clocks are the basic components of integrated circuits, these are further studied in Section 14.4. The rest of the chapter covers the topic of first- and second-order SCF sections.

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14.2 Switched Capacitor Resistor

Let us examine a simple circuit as shown in Figure 14.1(a), containing two switches and a capacitor C_R. The port voltages are v_1 and v_2, and the two switches become ON and OFF continuously at a certain clock frequency f_c. This means that each switch can remain on for a maximum time duration $T_c = 1/2\, f_c$. It is further assumed that either voltages v_1 or v_2 will remain constant during the small duration T_c when either of the switches is ON.

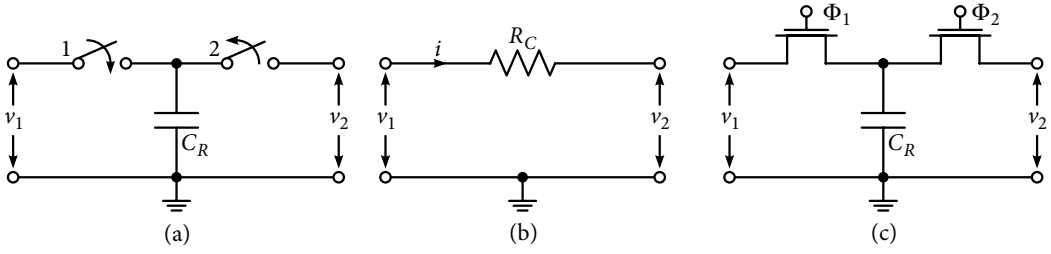

Figure 14.1 (a) Capacitor C_R switched alternately to voltages v_1 and v_2, (b) its equivalent resistance under certain conditions and (c) MOS based switches driven by a two-phase non-overlapping clock.

Initially, taking the switches as ideal, the capacitor C_R is first connected to port 1; as a result, on the kth switching cycle, the capacitor gets charged to a value $v_1(kT_c)$. Next, switch 1 is turned off and switch 2 is turned on for the half time period $T_c/2$. Now the capacitor C_R gets charged to $v_2(kT_c)$. Hence, the net charge transferred from port 1 to port 2 over the period T_c is given as:

$$\Delta Q = C_R\{v_1(kT_c) - v_2(kT_c)\} \tag{14.1}$$

This transfer of charge ΔQ takes place in a time period $\Delta T = T_c$. From the simple definition of current flow ($i = \Delta Q/\Delta T$), a current flows from port 1 to port 2 as:

$$i(kT_c) = \{C_R v_1(kT_c) - C_R v_2(kT_c)\}/T_c \tag{14.2}$$

If a resistance R_c is placed between port 1 and port 2 as shown in Figure 14.1(b), its current–voltage relation is simply:

$$i(kT_c) = \{v_1(kT_c) - v_2(kT_c)\}/R_c \tag{14.3}$$

Comparing equation (14.2) and (14.3), we get a very significant relation:

$$R_c = T_c/C_R = 1/f_c C_R \Omega \tag{14.4}$$

which implies that the switched capacitor circuit of Figure 14.1(a) behaves like an equivalent resistance depending on the value of the capacitance being switched OFF and ON, and the clock frequency f_c. It will be shown soon that the simulation of resistance using a capacitor and a clock has many advantages, but before that a few words of caution.

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An important consideration is that Ohm's law applied in equation (14.3) is valid only when voltages v_1 and v_2 remain constant during the time interval T_c. One of its implication may be that f_c has to be so high that T_c is small enough and rate of variation in v_1 and v_2 is small as well. It is to be noted that, in practice, there are certain restrictions on f_c to be too large; though the conditions are not arbitrary as will be seen later.

Another important consideration is the non-idealness of the switches which are to be realized either using BJT (bipolar junction transistor), but mostly using MOS (metal–oxide semiconductors) transistors, as shown in Figure 14.1(c).The switches are shown to be operated by two non-overlapping clocks. The effect of the non-idealness of the switches on the performance of the switched capacitor circuits needs to be taken care of. Hence, a brief discussion on the working of a practical MOS switch is also important while realizing switched capacitor circuits. The reason for using two-phase non-overlapping clocks and the simple method of generating such a clock will also be discussed.

The active RC filter circuit's pole frequency ω_o depends on the RC product time constant. Because of larger tolerances in the absolute values of resistor and capacitor elements in integrated circuits, the practically obtained value of ω_o suffers from inaccuracy. If resistance is simulated as in Figure 14.1, time constant τ in an RC circuit will become:

$$\tau = R_c C = \frac{1}{f_c C_R} C = \frac{1}{f_c} \frac{C}{C_R} \tag{14.5}$$

This means that the time constant now depends on (i) a clock frequency, which can be realized very accurately, using a stable crystal-based oscillator and (ii) the ratio of capacitors which can be realized up to an accuracy better than 0.1%. As a result, in most non-critical situations, parameter tuning is not needed for ω_o.

Another significant advantage in SC circuits is the saving in chip area; resistance is not realized in the conventional form of metal/polysilicon strips, which may consume greater chip area. Moreover, capacitors simulating resistances are not realized in absolute value but in ratio form, as evident from equation (14.5). Hence, capacitors C and C_R can be as small as practically feasible resulting in saving in chip area.

14.3 Switched Capacitor Integrators

Figure 14.2(a) and (b) show an OA-RC integrator and its SC version with resistance being simulated using capacitor C_1. Figure 14.2(c) shows the wave forms of the clock signal for the two phases φ_1 and φ_2. For the circuit of Figure 14.2(a), the well-known voltage relation is:

$$V_{\text{out}}/V_{\text{in}} = -1/sC_2R_1 \tag{14.6}$$

For the SC version in Figure 14.2(b), application of equation (14.4) gives:

$$V_{\text{out}} = -\frac{I_2}{sC_2} = -\frac{1}{sC_2}\frac{V_{\text{in}}}{R_{C1}} \rightarrow \frac{V_{\text{out}}}{V_{\text{in}}} = -\frac{f_c C_1}{sC_2} \tag{14.7}$$

where f_c is the clock frequency and comparison of equation (14.7) with (14.6) shows that the switched capacitor C_1 represents an equivalent resistance R_{C1}.

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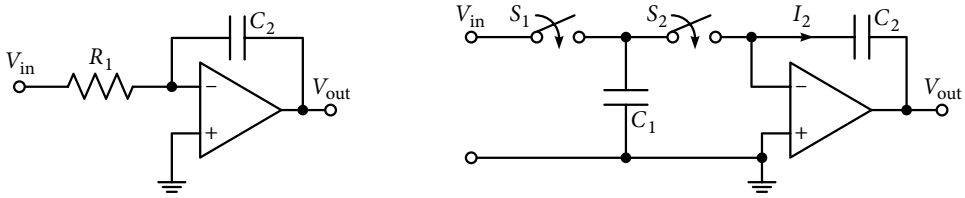
Example 14.1: What shall be the output in the SC integrator of Figure 14.2(b) if R_1 = 500 kΩ and C_2 = 0.5 nF for input signal V_{in} = 5 sin $5\pi \times 10^3$.

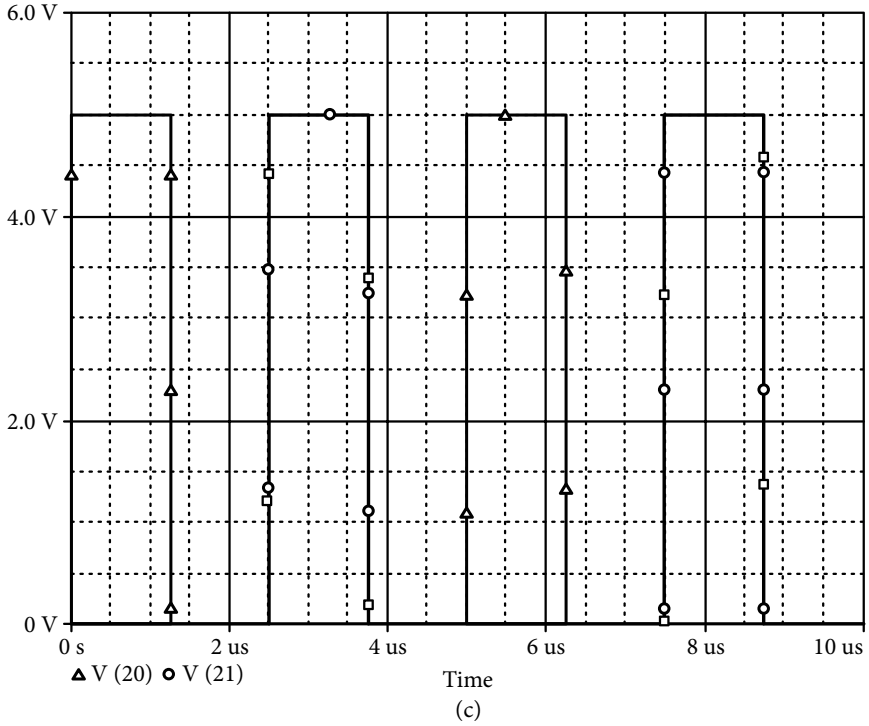
Solution: If a clock frequency of 2×10^5 rad/s is used to simulate the resistance R_1 by switching a capacitance, equation (14.4) requires the value of the capacitance C_1 in Figure 14.2(b) to be:

$$C_1 = 1/2 \times 10^5 \times 5 \times 10^5 = 10\text{pF}$$

If no parasitic capacitance is assumed in the switching act, use of equation (14.7) gives the peak-to-peak output voltage as:

$$V_{out}\,|_{pp} = -10\frac{2\times10^5\times10^{-11}}{5\pi\times10^3\times0.5\times10^{-9}} = -2.5454\,\text{volts}$$





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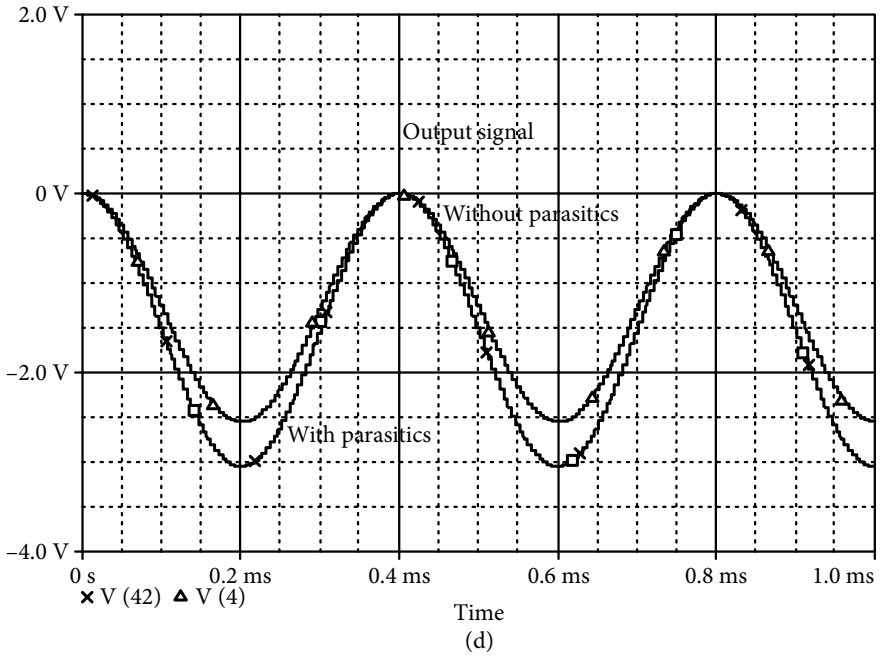

Figure 14.2 (a) Analog inverting integrator, (b) its switched capacitor version and (c) wave form of the non-overlapping clock signal applied to the switches. (d) Simulated output with and without the effect of parasitic capacitances for Example 14.1.

Figure 14.2(d) shows the PSpice simulated response, where peak-to-peak voltage of the output is 2.552 volts. It is common knowledge that there are parasitic capacitances when a MOS transistor is used for switching. The issue will be discussed later in the chapter; however, at present, if a parasitic capacitor of 2 nF is assumed to be present in parallel with C_1, the response will be affected and needs investigation. Figure 14.2(d) also shows that in such a case, peak-to-peak output voltage becomes 3.061 volts. It is an obvious effect of total switching capacitance becoming 12 nF. The effect of the parasitic capacitance and their elimination/minimization needs to be studied for accurate results in SC circuits.

The integrator circuit shown in Figure 14.2 can easily be modified to add and integrate two or more signals as shown in Figure 14.3(a)-(b). For Figure 14.3(a), an already known relation is:

$$V_{\text{out}} = -\frac{1}{sC_F}\left(G_1V_1 + G_2V_2 + G_3V_3\right) \tag{14.8}$$

For the SC version in Figure 14.3(b), the added currents of the inputs send more current in the form of a packet of charge to the capacitor C_F. In order to add the input currents, switches should become on and off at the same time. When these conditions are valid:

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$$V_{\text{out}} = -\frac{I_F}{sC_F} \rightarrow V_{\text{out}} = -\frac{f_c}{sC_F}\left(C_1V_1 + C_2V_2 + C_3V_3\right) \tag{14.9}$$

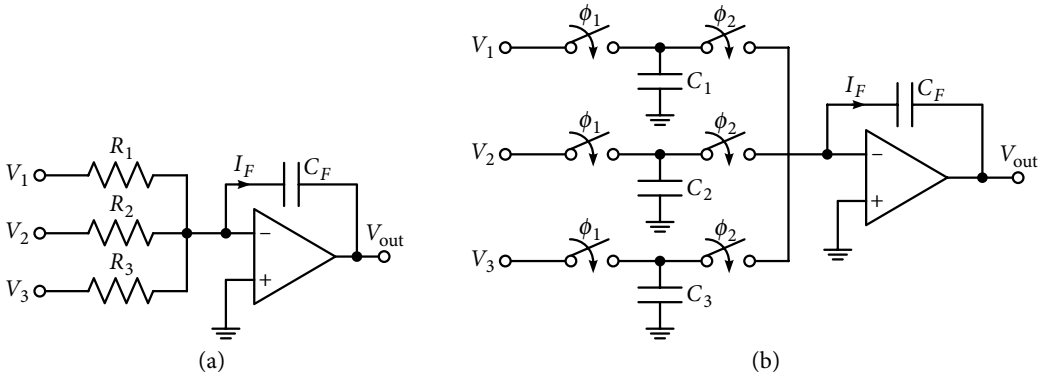

Figure 14.3 (a) Analog inverting summer, (b) its switched capacitor version.

For $C_1 = C_2 = C_3 = C_F$, input voltages will be added without any weightage during integration.

In an analog OA based circuit if a signal is to be subtracted, it needs to be inverted first. For example, in Figure 14.3(a) if V_1, V_3 were positive and V_2 was negative, the output would have been obviously:

$$V_{\text{out}} = -(G_1V_1 - G_2V_2 + G_3V_3)/sC_f \tag{14.10}$$

In the SC circuits, if an input signal is to be subtracted, it need not be inverted. Instead, it needs to be switched to the alternate phase compared to the other signals as shown in Figure 14.4. Obviously, now the current (charge) is sent to C_F in one direction from V_1 and V_2, but the current is sent in the reverse direction from V_3 . Effectively, resistance R_1 and R_2 are simulated as positive resistances and R_3 as a negative resistance. It results in the following relation:

$$\left|V_{\text{out}}\right| = -\frac{f_c}{\omega}\left(\frac{V_1C_1}{C_F} + \frac{V_2C_2}{C_F} - \frac{V_3C_3}{C_F}\right) \tag{14.11}$$

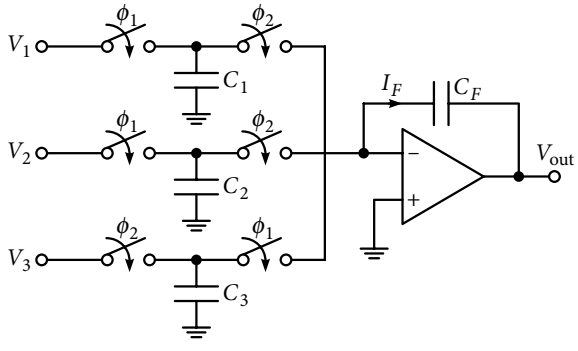

Figure 14.4 A signal (V_3) being subtracted while the other two are added in inverting summer.

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Example 14.2: Using the SC inverting integrating summer of Figure 14.3(b), voltages $V_1 = 2\sin(5\pi\times 10^2\, t)$, $V_2 = 3\sin(5\pi\times 10^2\, t)$ and $V_3 = 1.0\sin(5\pi\times 10^2\, t)$ are to be added with respective multiplication factors of 1, 0.8 and 1.2. Find output voltage without any parasitic, and with a parasitic capacitance of 2 nF with each switch.

Solution: For input signals at 250 Hz, a clock frequency of 200 krad/s (arbitrary, but the same as in Example 14.1) is employed. With selected capacitance $C_F = 1$ nF, for the given multiplication factor of unity for the input signal V_1, the value of the capacitor C_1 is found using equation (14.9) as:

$$2 = \frac{2\times 10^5}{5\pi\times 10^2\times 10^{-9}}\left(C_1\times 2\right) \rightarrow C_1 = 7.857\,\text{pF}$$

Similarly, for a gain of 0.8 for V_2 and a gain of 1.2 for V_3 values of the capacitors $C_2 = 6.285$ pF and $C_3 = 9.428$ pF. Using these elements, the simulated output is shown in Figure 14.5, where the peak-to-peak voltage is 11.34 volts; theoretically, Vpp = 11.19 volts from equation (14.9).

If lump-sum parasitic capacitances (each of 2 pF) are also present at input, the effective input capacitances will increase and the output voltage will become:

$$V_{\text{pp}} = -\frac{2\times 2\times 10^5}{5\pi\times 10^2\times 10^{-9}}\left(9.857\times 2 + 8.285\times 3 + 11.428\times 1\right)\times 10^{-12} = -14.25 \text{ volts}$$

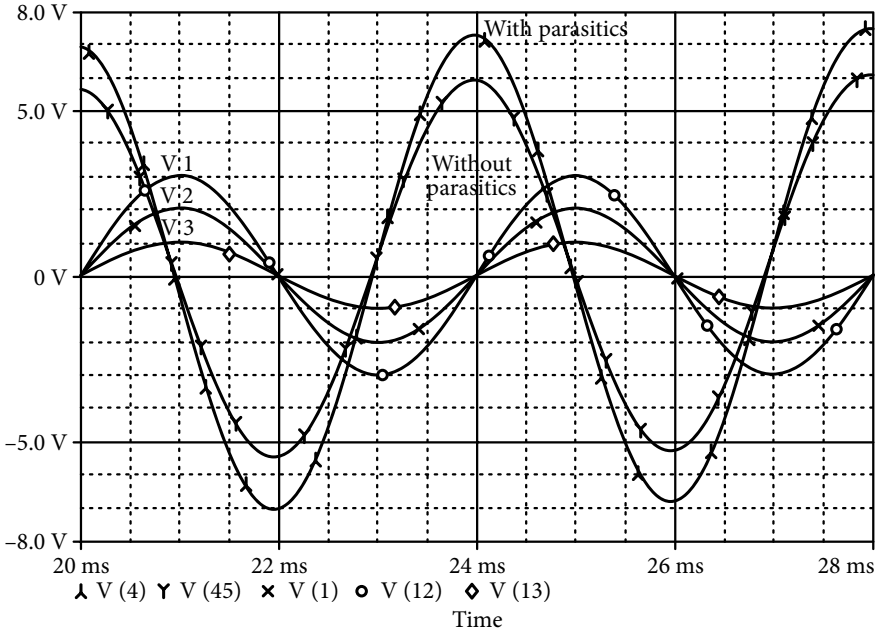

Figure 14.5 Simulated input and output voltages for the inverting summer in Example 14.2, with and without parasitic capacitors.

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The simulated response in this case is also shown in Figure 14.5, where peak to peak output voltage is 14.31 volts confirming the predicted value.

14.4 MOS Switches

Some simple SC circuits were discussed in the previous sections assuming the switches to be ideal (and with lump sum arbitrarily connected parasitic). Before moving ahead to discuss first-order filter sections, it is important to briefly discuss some issues connected with the use of the MOS switch, its switching act and the effect of some of its important non-idealities.

14.4.1 Finite resistance

From its name *switched capacitor* circuits, it is evident that switches are the basic components along with capacitors. BJTs, MOS and CMOS transistors as transmission gates have been used widely as switches. Presently, we shall discuss only MOS transistor switches which are economical and also better suited for integration. Figure 14.6(a) shows a MOS transistor schematic and its conventional simple model.

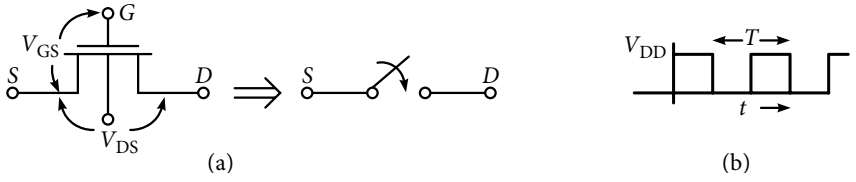

Figure 14.6 (a) MOS schematic and switch, (b) clock with 50% duty cycle.

For an ideal switch, its resistance should be zero when it is on and infinite when it is off. However, in practice, the resistance values depend on size and fabrication process of the transistor. In general, for a minimum size transistor, its ON resistance R_{on} ranges around 10^3 –10^4 Ω and when it is off, its resistance R_{off} ranges around 100–1000 MΩ.

14.4.2 Permissible clock frequency

As obvious from Figure 14.1, alternate charging and discharging of capacitors takes place in order to transfer net charge from one port to another. The equivalence of it is seen to be a measure of the total charge transfer per cycle. For practical implementation, it is essential to keep port voltages constant during respective half cycle. It represents the idea of *sample and hold* of the port voltages at a suitable clock frequency at which the capacitor (dis)charges. Frequency of the clock is important, as it sets the available half (or less; as shall be shown later) time period for charging of capacitors.

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The practical time for charging and discharging depends on the on and off resistance of the switches and the involved capacitor. For example, if $R_{on} = 5\ k\Omega$, $R_{off} = 500\ M\Omega$ and a capacitor C_R of 10nF is switched, then *on-time constant*, τ_{on} and *off-time constant*, τ_{off} will be respectively:

$$\tau_{on} = R_{on}\, C_R = 5 \times 10^3 \times 10 \times 10^{-12} = 12\ ps \tag{14.12a}$$

$$\tau_{off} = R_{off}\, C_R = 500 \times 10^6 \times 10 \times 10^{-12} = 5\ ms \tag{14.12b}$$

The ratio τ_{off}/τ_{on}, which is essentially R_{off}/R_{on} and generally known as the *discrimination factor* of the MOS switch is 10^5 or 100 dB in the aforementioned example. The larger the value of the discrimination factor, the closer it is to the ideal. The large discrimination factor enables the switched capacitor to acquire the charge through sampling, and holding it for relatively larger time, compared to the acquisition time of charge. Practically, it has been observed that in order to acquire a signal with sufficient accuracy during the half cycle of the clock period, the half cycle time duration should be greater than the time constant τ_{on}, that is, the following condition is required for the switch clock rate to get a sufficiently good output response.

$$0.5T_c > 5\tau_{on} = 5R_{on}\, C_R \rightarrow T_c > 10\, R_{on}\, C_R \tag{14.13}$$

The Nyquist frequency definition states that in order to reconstruct a sampled signal, the sampling clock frequency has to be more than twice the frequency corresponding to that component of signal which has the maximum frequency, f_{max}. Only this condition provides a reconstructed signal without anti-aliasing. The condition, based on Nyquist criteria, helps in finding the lower limit of the switching frequency, whereas equation (14.13) mentions the condition of the upper limit of the clock frequency. Combining the two conditions gives the following relation governing clock frequency range.

$$2f_{max} \leq f_c \leq 1/5\, R_{on}\, C_R \tag{14.14}$$

14.4.3 Non-overlapping clock generation

It is essential that the clock pulses are non-overlapping with sufficient duration in which both the switches are off. This is considered as a *break-before-make* scheme in which switching in the next half-cycle starts only when it is ensured that capacitor C_R has been completely disconnected from the other port. If the two phases have 50% duty cycle, with no time when both the switches are off, it may create a serious problem. Even a small delay or advancement in one of the pulses creates specific time durations in which two switches become simultaneously on; this spoils the sequence of charging and (dis)charging of the capacitor.

Few circuits are available for generating non-overlapping two-phase clocks. One of these circuits is shown in Figure 14.7(a) employing two NOR, one inverter and a 50% duty cycle input clock φ_{in}. The input clock, its inverted output form delayed by one inverter delay φ_A and the final outputs φ_1 and φ_2 are shown in Figure 14.7(b). As each NOR has an input from the output of the other NOR, it ensures that output φ_1 and φ_2 will never be simultaneously on. In

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reality, the delay of the gates ensures a definite time gap between φ_1 becoming too high and φ_2 becoming too low, and vice versa.

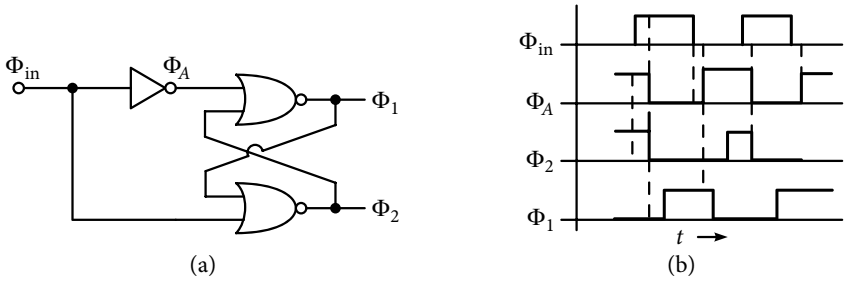

Figure 14.7 (a) Generation of a two-phase non-overlapping clock and (b) its waveforms.

14.4.4 Parasitic capacitances

One of the intended advantages of the SC circuits is the use of capacitors in ratio form with practically the smallest size capacitors, resulting in the consumption of as less chip area as possible. It is certainly a great advantage, but a potential threat to it comes from the fact that fabrication of capacitors itself generates quite a few number of parasitic capacitances. Hence, it is essential to not only know these parasitic elements, but account for them in such a way that their effect is either eliminated or minimized. Steps also have to be taken to assimilate the parasitic capacitances in the filter design.

There are many schemes of capacitor fabrication in integrated circuits; however double poly or poly-poly capacitors, which are realized using two polysilicon layers, with a thin silicon dioxide in between, are the most common approach. The intended capacitor to be realized is C_R which is fabricated between top and bottom poly layers and C_T and C_B are, top plate to substrate, and bottom plate to substrate parasitic capacitances, respectively, as shown in Figure 14.8(a). Here, C_B is generally 10–15% of the fabricated value of C_R and C_T is in the range of 1–2% of C_R. The behavior and effect of the parasitic capacitor depends on the type of fabrication, voltage level of the substrate depending on the kind of transistor used, NMOS (negative metal–oxide semiconductor) or PMOS (positive metal–oxide semiconductor), and whether C_R will be a floating, or a grounded capacitor in which the bottom plate terminal will be connected to ground. With V at ground level for NMOS, C_B becomes short circuited if C_R is a grounded capacitor; this is why grounded capacitances are preferred in active circuit designs.

There are other parasitic capacitances introduced due to switches and the input capacitance of OA used. Different techniques are used to counter the effect of all these parasitic capacitances either through the proper usage of switches or the formation of circuit structures as will be shown here and in the next section.

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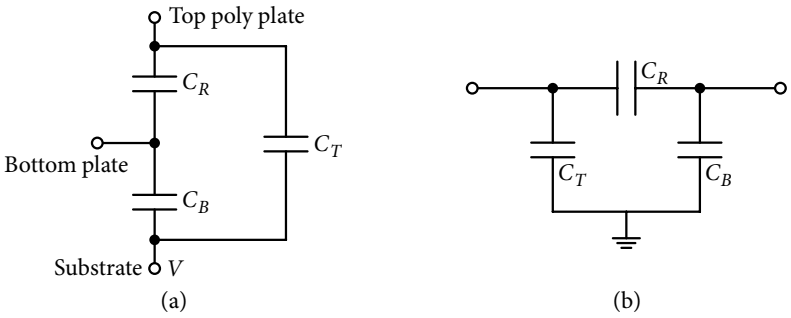

Figure 14.8 (a) Simplified view of important parasitic capacitances in a poly-poly capacitor; (b) its small signal equivalent C_R in floating form, and its parasitic.

For a good circuit design, effort is made such that charge flow in C_T and C_B becomes independent of the charge delivered by C_R. If C_R is to be used as a floating capacitor, Figure 14.8(a) will have to be modified to Figure 14.8(b) with the substrate at ground potential. To eliminate the effect of the parasitic capacitance, the symmetrically switched capacitor arrangement shown in Figure 14.9 can be used. The circuit uses four single-pole single-throw (SPST) switches with clock phases shown alongside. When φ_1 is on, φ_2 remains off, which makes C_R and C_T parallel, charging both of these to voltage v_1. At the same time, C_B gets short-circuited; hence, it is disconnected from C_R. In the next half cycle, φ_1 is off and φ_2 is on. Charge on C_T goes to ground, but C_R and C_B, which are in parallel get charged to v_2. Obviously, in the next half cycle, the charge on C_B goes to ground, making its presence also ineffective. The principle behind the operation is that the capacitor is switched to voltage sources in such a way that the parasitic conductances are parallel to the capacitor, thereby nullifying the effects of these parasitic conductances on filter performance.

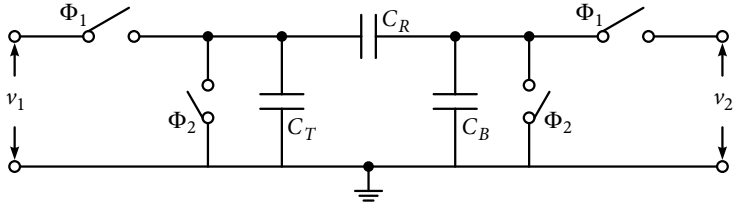

Figure 14.9 Symmetrically switched capacitor simulation of a resistor.

14.5 Parasitic Insensitive Integrators

Other than the parasitic capacitances of the switches, there are a few more parasitic capacitances and these are also to be accounted for. Figure 14.10(a) shows the conventional OA-RC integrator, in which the resistance is simulated using switched capacitor C_R. The circuit shows the parasitic capacitance of the capacitor C_R and the feedback capacitor C_F, parasitic capacitance of the switches C_S, and input capacitance of the OA, C_{OA}.

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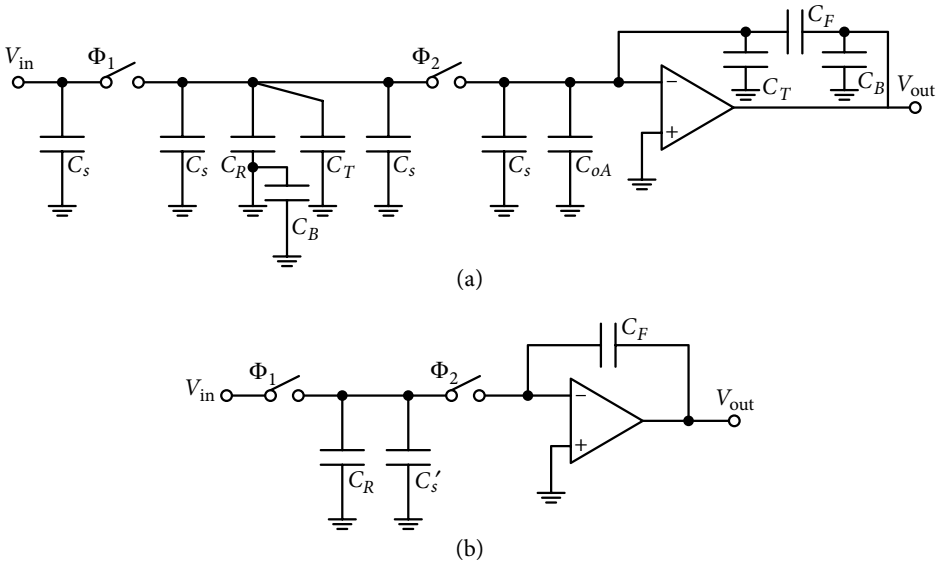

Figure 14.10 (a) Switched capacitor inverting integrator showing parasitic capacitances and (b) parasitic capacitances-accumulated simplified circuit.

As C_R is grounded, the corresponding C_B get short circuited. All parasitic capacitors connected to the inverting terminal of the OA also become ineffective as the terminal is at virtual ground. Switch capacitor C_s on the left of switch φ_1 and the bottom plate capacitance of C_F are driven by input and output voltages, respectively; they become ineffective. This means that the switched capacitor on the right of switch φ_1 and left of switch φ_2 and the top plate parasitic capacitance of C_R, combined together as one capacitance C_s' appear in parallel with C_R, as shown in Figure 14.10(b). This further means that the RC product of the integrator has changed and in comparison with equation (14.7), now the transfer function will become:

$$\frac{V_{\text{out}}}{V_{\text{in}}} = -f_c \frac{(C_R + C')}{sC_F} \tag{14.15}$$

If the value of C' was known correctly, it could have been included in the design. However, in addition to the value being probably incorrect, it is also quite variable. To eliminate the effect of C', the technique proposed in the previous section of applying symmetrically placed switches is used. Figure 14.11(a) and (b) show the application of symmetrical switching applied to the integrator of Figure 14.10, which results in a *parasitic insensitive* integrator in inverting and non-inverting mode, respectively. Practically, there is no difference in the operation of the circuit shown in Figure 14.11(a) with the circuit shown in Figure 14.11(b); both eliminate the parasitic C_1' and C_2' completely. Compared to the circuit shown in Figure 14.11 (a), in Figure 14.11(b), there is a difference in the ordering of the switching as shown. For φ_2 on and φ_1 off, C_R is charged by v_{in} but it is not connected with C_F, thus, no change in C_F takes

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place. Next for φ_2 off and φ_1 on, C_R is connected to C_F at the inverting terminal of the OA with its negative polarity; it gets discharged to ground. This negative discharging which equals $(-f_c C_R V_{in})$ flows into C_F and adds to its charge; this is opposite to what happens in the inverting integrator case. Hence, it can also be considered as though this kind of switching, simulated resistance becomes negative, $-R_R$. Therefore, the transfer function will be:

$$\frac{V_{out}}{V_{in}} = f_c \frac{C_R}{sC_F} \rightarrow -\frac{1}{sC_F(-R_R)} \tag{14.16}$$

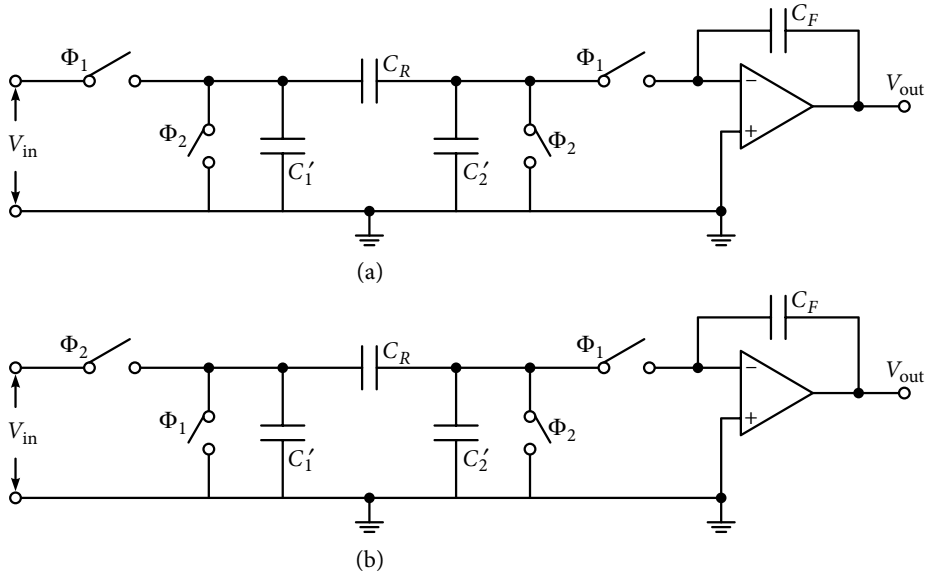

Figure 14.11 (a) Parasitic insensitive integrator using symmetrical switching in inverting mode and (b) in non-inverting mode.

Effectively, the transfer function in equation (14.16) realizes a non-inverting integrator. Hence, if there are more than one input signals, these can be added as in Figure 14.3. Moreover, subtraction can also be done by proper selection of switching. In Figure 14.3, if resistances R_1 and R_3 are simulated as positive resistances and R_2 is simulated as negative, it results in the following relation, with $s = j\omega$:

$$V_{out} = -\frac{f_c}{\omega}\left(\frac{V_1 C_1}{C_F} - \frac{V_2 C_2}{C_F} + \frac{V_3 C_3}{C_F}\right) \tag{14.17}$$

In case of a simple subtraction without any weightage to the input voltages, $C_1 = C_2 = C_3$, and the output voltage expression becomes:

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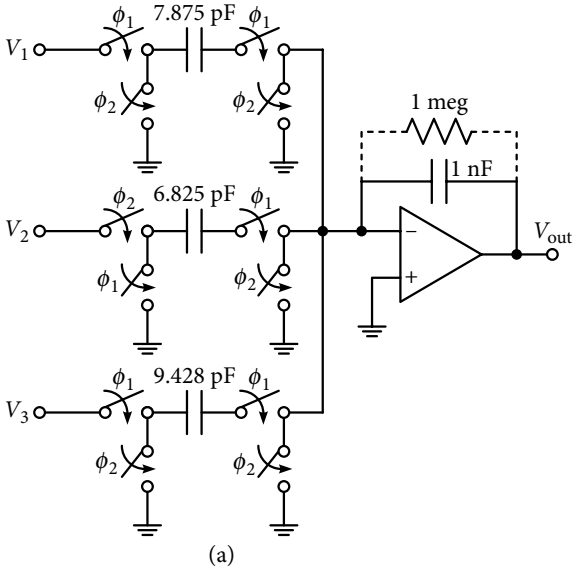
$$V_{\text{out}} = -\frac{f_c}{\omega}\frac{C_1}{C_F}\left(V_1 - V_2 + V_3\right) \tag{14.18}$$

Repeating Example 14.2 with V_2 becoming negative, the peak-to-peak output voltage from equation (14.17) becomes 1.61 volts. The circuit shown in Figure 14.12(a) was simulated, with intentionally introduced 2 nF parasitic capacitances as well at each switch location. Figure 14.12(b) shows the simulated response, with output as 1.55 volts p-p; the parasitic capacitances have no effect. It is to be noted that a high value resistance is connected in the feedback path; otherwise, the output voltage remains clamped to $+V_{\text{CC}}$.

14.6 Sampled Data Switched Capacitor Filters

While studying SC resistors in Section 14.2, it was assumed that the clock frequency is much greater than the signal frequency and the node voltages remain constant for a small duration (nearly half cycle) and then changes in small steps. This simply means that the signal is not continuous with time; therefore, its analysis as a purely analog circuit is not exactly correct. In reality, the correct procedure of analysis (and synthesis) is to use discrete-time equations rather than continuous ones. While using discrete-time equations, the frequency domain consideration is known as *sampled data characterization* and the frequency variable is also different. Instead of using Laplace transformation and complex frequency variable s, z-transform is used. A brief discussion about the relation between continuous-time domain and the sampled data characterization is now included with the help of the simple SC integrators discussed in Sections 14.3 and 14.5.



(a)

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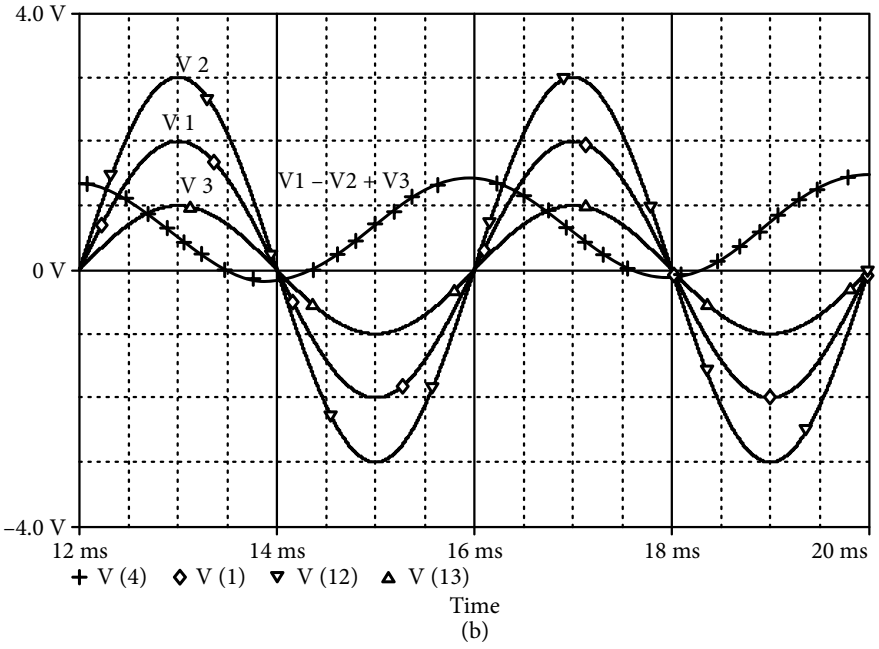

Figure 14.12 (a) Summing (and subtracting) switched capacitor integrator. (b) Simulated response in a parasitic insensitive subtractor using equation (14.18).

14.6.1 Sampled data integrators

The OA-RC inverting integrator and its SC version are shown in Figure 14.2(a) and (b) and the non-overlapping clock signal is shown in Figure 14.2(c). The clock signal φ_1 makes switches on at time instants $(n-1)T$, nT, $(n+1)T$, … and the clock signal φ_2 makes switches on at time instants $\left(n-\frac{1}{2}\right)$, $\left(n+\frac{1}{2}\right)$, $\left(n+\frac{3}{2}\right)$, and so on. In contrast to the analog signal case, where the topology of the circuit remains unchanged with time, the topology of the circuit is distinct in two phases of the clock period in SC case. Figure 14.13(a) and (b) shows the topology of the inverting integrator during the two respective phases of the clock.

To convert the discrete-time domain relations into discrete frequency domain equations, the z-transform is to be applied to the two distinct sampling sequences, for phase φ_1 and for phase φ_2. One such transformations has been obtained as:

$$s \leftrightarrow \frac{1}{T}\frac{1-z^{-1}}{z^{-\frac{1}{2}}} \rightarrow s \leftrightarrow \frac{1}{T}(z^{\frac{1}{2}} - z^{-\frac{1}{2}}) \tag{14.19}$$

Equation (14.19) is an important transformation relation between frequency variables s and z, and it is known as a *lossless digital integrator* (LDI) transformation. This transformation is obtained while considering phase 2 as the valid output. There are other transformations available based on the structure through which resistance is simulated in an SC circuit.

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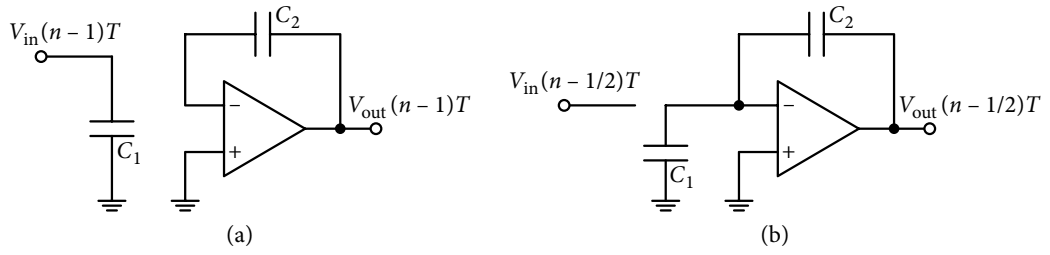

Figure 14.13 Inverting integrator equivalent circuits for the two respective non-over lapping clock inputs.

14.7 Bilinear Transformation: Warping Effect

As mentioned earlier, there are other *s to z* transformations. One of the most popular transformations is known as the *bilinear* transformation, which is given as:

$$s \leftrightarrow \frac{2}{T}\frac{1-z^{-1}}{1+z^{-1}} \tag{14.20}$$

The main reason behind the popularity of the transformation is that the entire analog frequency ranging from zero to infinity is transformed from zero to (π/T) in the sampled data frequency domain.

If we substitute $z = e^{j\Omega T}$ in equation (14.20), we get:

$$s \leftrightarrow \frac{2}{T}\frac{1-e^{-j\Omega T}}{1+z^{-j\Omega T}} \rightarrow \omega = \frac{2}{T}\tan\frac{T\Omega}{2} \tag{14.21}$$

For equation (14.21), it is observed that when $\omega = 0$, $\Omega = 0$ but when $\omega = \infty$, $\tan\frac{T\Omega}{2} = \infty$ implies $\Omega = (\pi/T)$. This also implies that when bilinear transformation is used while deriving $H(z)$ from $H(s)$, the response of $H(z)$ will get some what squeezed. This is known as the *warping effect* of the bilinear transformation.

The warping effect can be compensated by *pre-warping*. In an analog circuit, if ω_o is a critical frequency, like the center frequency of a BP filter, in the transfer function $H(s)$, then $H(s)$ is re-written with ω_o replaced by a pre-warped frequency ω_o^*, which is related as:

$$\omega_o^* = \frac{2}{T}\tan\frac{\omega_o T}{2} \tag{14.22}$$

Obviously, the s domain transfer function will change, which can be symbolized as $H(s^*)$. This operation results in the critical frequency Ω_o in $H(z)$ same as ω_o in $H(s)$:

$$\Omega_o = \frac{2}{T}\tan\frac{\omega_o^* T}{2} = \frac{2}{T}\tan^{-1}\left\{\frac{T}{2}\frac{2}{T}\tan\frac{\omega_o T}{2}\right\} = \omega_o \tag{14.23}$$

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The biquadratic transfer function expressions in the sampled data domain is given in Table 14.1 for the most commonly used analog transfer functions when the bilinear transfer function is applied with the following relations:

$$H(s) = N(s)/D(s),\ \ D(s) = s^2 + (\omega_o/Q_o)s + \omega_o^2 \tag{14.24}$$

$$H(z) = h_D \frac{1 + a_{1N}z^{-1} + a_{2N}z^{-2}}{1 - a_{1D}z^{-1} + a_{2D}z^{-2}},\ D(z) = a^2 + (\omega_o^*/Q_o)a + \omega_o^{*2} \tag{14.25}$$

$$a = 2/T,\ \omega_o^* = a\tan\left(\frac{\omega_o}{a}\right),\ \omega_n^* = a\tan\left(\frac{\omega_n}{a}\right) \tag{14.26}$$

$$a_{1D} = 2(a^2 - \omega_o^{*2})/D(z),\ \ a_{2D} = \left\{a^2 - (\omega_o^*/Q_o)a + \omega_o^{*2}\right\}/D(z) \tag{14.27}$$

Table 14.1 Sampled data transfer functions when bilinear transformation is applied to analog transfer functions

Filter type	Numerator $N(s)$ of the transfer function $H(s) = N(s)/D(s)$	$h_D \times D(z)$	a_{1N}	a_{2N}
LP	$H_{LP}\omega_o^2$	$H_{LP}\omega_o^{*2}$	2	1
HP	$H_{HP}s^2$	$H_{HP}a^2$	–2	1
BP	$H_{BP}(\omega_o/Q_o)s$	$H_{BP}(\omega_o^*/Q_o)a$	0	–1
AP	$H_{AP}\{1 - 2(\omega_o/Q_o)/D(s)\}$	$H_{AP}a_{2D}\,D(z)$	$-a_{1D}/a_{2D}$	$1/a_{2D}$
Notch	$H_N(s^2 + \omega_{on}^2)$	$H_N(a^2 + \omega_n^{*2})$	$-2\dfrac{(a^2 - \omega_n^{*2})}{(a^2 + \omega_n^{*2})}$	1

Example 14.3: Obtain the sample data transfer function for the following BP transfer function by applying bilinear transformation. Use a clock frequency of 16 kHz.

$$H(s) = \frac{1.5\times10^4 s}{s^2 + 1500s + 2.25\times10^8} \tag{14.28}$$

Solution: From equation (14.28), parameters are obtained as:

$$\omega_o = \sqrt{2.25}\times10^4 = 1.5\times10^4 \text{ rad/s}, \omega_o/Q_o = 1500 \rightarrow Q_o = 10, H_{BP} = 10$$

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For clock frequency f_{CL} = 16 kHz, time period T = 62.5 μs. It gives pre-warped center frequency as:

$$\omega_o^* = 2f_{CL}\tan\left(\frac{\omega_o}{2f_{CL}}\right) = 2\times16*10^3\tan\left(1.5\times10^4\times180/32\times10^3\pi\right) = 16.19\,\text{krad/s}.$$

So, the pre-warped transfer function shall be:

$$H\left(s^*\right) = \frac{1.6197\times10^4 s^*}{s^{*2}+1.6197\times10^3 s^* + 1.6197^2\times10^8} \tag{14.29}$$

From equation (14.24) to equation (14.27), parameters for the z-domain transfer function are evaluated as:

$a = 2/T = 32 * 10^3$

$D(z) = (32 * 10^3)^2 + 1.6197 * 10^3 * 32 * 10^3 + 1.6197 * 10^8 = 13.3817 * 10^8$

$a_{1D} = 2(32 * 10^6 - 2.6234 * 10^8)/D(z) = 1.13836$

$a_{2D} = \{(32 * 10^3)^2 - 1.6197 * 10^3 * 32 * 10^3 + 1.6197^2 * 10^8\}/D(z) = 0.9225$

$h_D = 10 * 1.6197 * 10^3 * 32 * 10^3/D(z) = 0.5183$

Therefore,

$$H(z) = \frac{0.5183(1-z^{-2})}{1-1.3836z^{-1}+0.9225z^{-2}} \tag{14.30}$$

It may be mentioned that $H(z)$ in equation (14.30) can also be obtained by applying the $s \leftrightarrow z$ transformation of equation (14.20) on the pre-warped analog transfer function of equation (14.29).

14.8 First-order Filters

Ideal integrators are first-order LP filters since the output starts dropping as soon as the frequency is finite. To have its cut-off frequency as finite, the integrators are made lossy through the simple addition of a resistance in the feedback path of the OA based integrator. Other first-order circuits are HP or bilinear ones. One of the simplest ways to obtain any of these first-order filters in SC form is to simulate the resistance, using switches and capacitors, in a corresponding OA-RC circuit. The parasitic insensitive approach is mostly used to eliminate

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errors. Hence, specific to first-order SCFs, no specific theory is involved. The following exercises will be helpful.

Example 14.4: Figure 14.14 shows an LP filter circuit. Design it for a 3-dB frequency of 3.4 kHz and dc gain of 5 dBs. Convert it as a first-order SC LPF while selecting a suitable clock frequency. Compare the output response of both the versions.

Solution: Both the resistors in Figure 14.14 are simulated as SC. The converted SC circuit is shown in Figure 14.15, for which the transfer function is obtained as:

$$H(s) = \frac{V_{\text{out}}}{V_{\text{in}}} = -\frac{1/C_F R_1}{s + 1/C_F R_2}$$

With

$$\omega_{3dB} = \frac{1}{C_F R_2}, \text{dc gain } H(0) = \frac{R_2}{R_1} \tag{14.31}$$

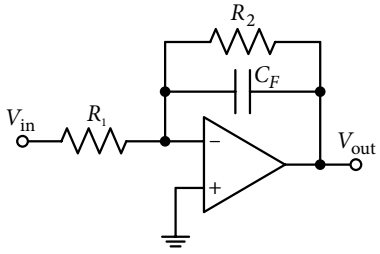

Figure 14.14 First-order OA-RC active low pass filter for Example 14.4.

For $\omega_{3\text{dB}}$ = 3.4(2π) krad/s, selecting C_F = 10 nF, the obtained value of R_2 = 4.679 kΩ and for the dc gain of 5 dB, R_1 = 2.631 kΩ. For these element values, its frequency response is now compared with that of the SC version. For converting the circuit to the SC form, capacitor values are preferably in the pF range. Hence, now the selection of C_F = 20 pF means the resistance values will become R_2 = 2.3395 MΩ and R_1 = 1.3158 MΩ. For the cut-off frequency of 3.4 kHz, we assume a maximum operating frequency of 34 kHz to get the whole range of the response spectrum. Since the clock frequency needs to be preferably 5 times the maximum operating frequency, the selected clock frequency f_c = 180 kHz. Now, if R_1 is simulated using capacitor C_1, its value will be $1/180 \times 10^3 \times 1.3158 \times 10^6$ = 4.22 pF and C_2 = 2.374 pF. For the SC version employing symmetrical switching shown in Figure 14.15, the time domain response is shown in Figure 14.16 for the OA-RC as well as the SC version. The respective voltage gains for both types of filters are shown in Table 14.2.

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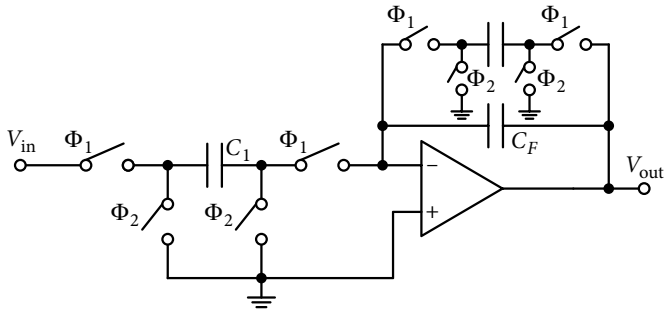

Figure 14.15 SC inverting integrator as first-order low pass filter from Figure 14.14.

Table 14.2 Voltage gains of the OA-RC and SC filters of Figures 14.14 and 14.15

Voltage gain at frequency (kHz)	0.20	3.4	5.0	10.0
OA-RC circuit	1.774	1.252	1.0	0.567
SC circuit	1.808	1.229	0.965	0.56

At 200 Hz, the respective gains are almost 5 dBs and 5.15 dBs, and at 3.4 kHz, the respective gains drop to 3.02 dBs and 3.35 dBs; this confirms their design cut-off frequency.

14.9 Simulation of SC Networks

Continuous-time active filters use PSpice and similar software for analysis. However, these simulation tools become too time-consuming for the analysis of SC networks when the MOS transistors are modeled as voltage-controlled switches. Therefore, one option is to simulate the SC network in time domain, as has been shown for Example 14.4.

In an alternate scheme, the s domain transfer function is first transformed into the z domain, and then the z domain transfer function is simulated in terms of delay lines and voltage-controlled voltage sources (VCVSs). The reason for the adoption of this technique lies in the following relation. From the z domain transfer function, the output signal $V_{\text{out}}(z)$ can be expressed as:

$$V_{\text{out}}(z) = k_1 V_i + k_2 V_i z^{-\left(\frac{1}{2}\right)} + k_3 V_i z^{-1} + \ldots + A V_{o1} z^{-\left(\frac{1}{2}\right)} + B V_{o2} z^{-1} + C V_{o3} z^{-\left(\frac{3}{2}\right)} \qquad (14.32)$$

Here, k_1, k_2, ……A, B, …. are constants, V_i, V_{o1}, V_{o2} … are the z transformed input and output voltages, and $z^{-(1/2)}$, z^{-1} … are delays by half-a-period, one full period, and so on. Obviously, the delay is represented by the transmission line with delay, and the constants are implemented either by VCVS or an amplification factor. The technique is illustrated by taking a specific case of Example 14.4.

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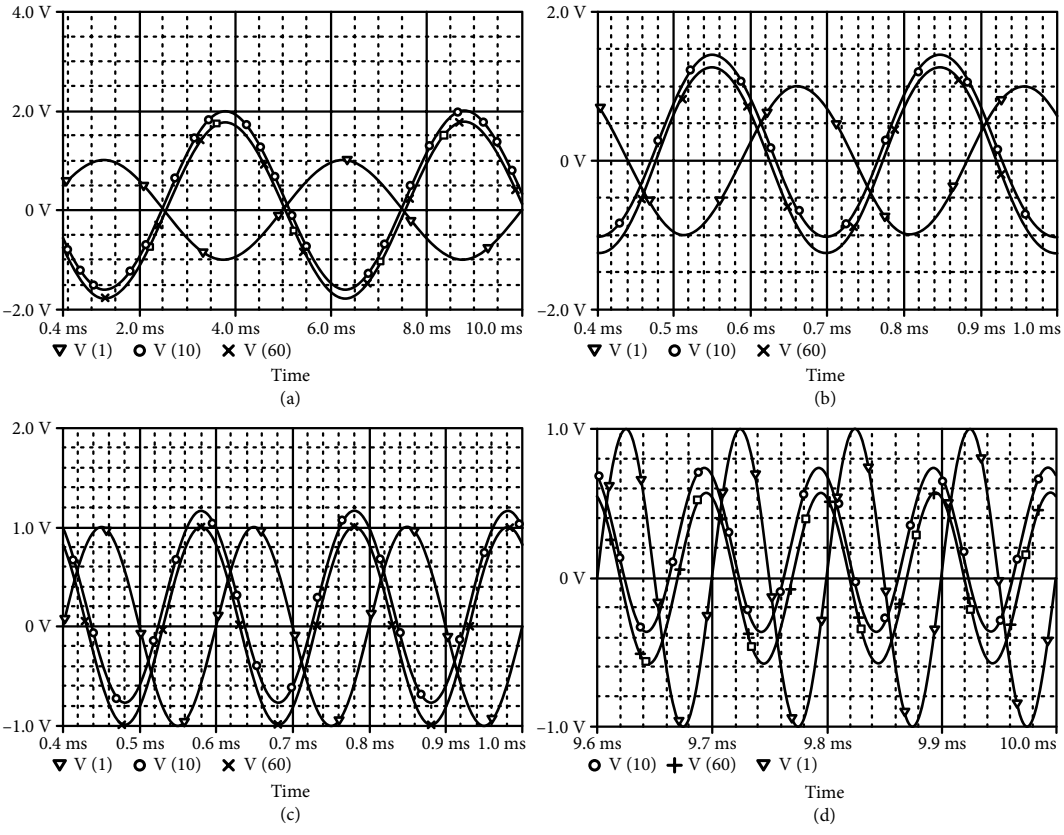

Figure 14.16 Time domain response of the OA-RC circuit of Figure 14.14 and the switched capacitor filter of Figure 14.15 at (a) 0.2 kHz, (b) 3.4 kHz, (c) 5 kHz and (d)10 kHz.

The transfer function of the first-order LPF given in equation (14.31) is re-written as:

$$H(s) = \frac{V_{out}}{V_{in}} = -\frac{1/C_F R_1}{s + 1/C_F R_2} = -\frac{a}{s+b} \tag{14.33}$$

Using bi-linear transformation equation (14.20), the z domain transfer function for $H(s)$ is obtained as:

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = -\frac{a(1+z^{-1})}{2f_s\left(1-z^{-1}\right) + b(1+z^{-1})} \tag{14.34}$$

It gives:

$$V_{out}(z) = -k_1 V_{in}(z) - k_3 V_{in}(z)z^{-1} + BV_{out}(z)z^{-1} \tag{14.35}$$

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In equation (14.34), the clock frequency $f_s = 1/T$ and in equation (14.35):

$$k_1 = k_3 = \frac{a}{2f_s + b} \text{ and } \mathrm{B} = \frac{2f_s - b}{2f_s + b} \tag{14.36}$$

Figure 14.17(a) shows the block diagram for the realization of equation (14.35) using basic delay, adder and multipliers. For simulating the block diagram of Figure 14.17(a), the expanded form is shown in Figure 14.17(b). For Figure 14.17 and for other simulations in the z domain, a systematic adopted procedure is outlined in the following.

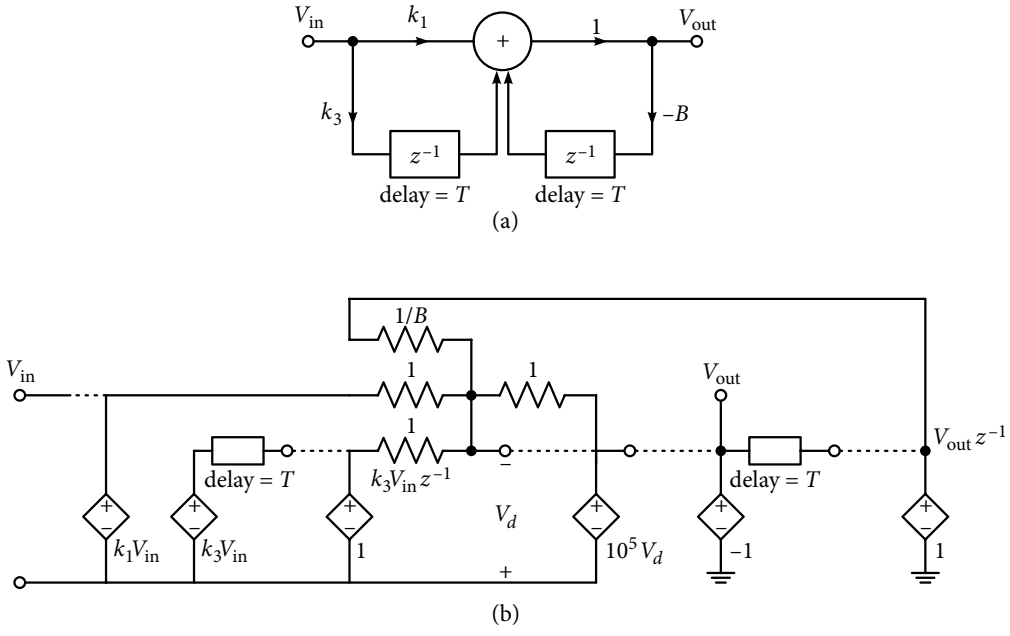

Figure 14.17 (a) Block diagram for realizing equation (14.35), employing inverting summer, delay lines and multipliers. (b) Expanded form of the block diagram shown in Figure 14.17(a).

The first step, which is already taken, is the formation of equation (14.35) for V_{out}, in which a feedback factor from the output will be a must. The next step is in the formation of basic units of half-a-delay ($T/2$) isolated by a buffer (or inverter), because in some cases, factors of ($z^{-1/2}$) are also involved. Then, the delay blocks and the VCVSs for the implementation of buffers (or inverters) and gain (or attenuation) are appropriately joined together as suggested by basic equations like equation (14.35).

The above steps are completed for each OA sub-network in the original active RC network and proper connectivity is ensured in a network on the lines of Figure 14.17(b); the simulation is then performed.

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Example 14.5: Simulate the first-order LPF of Example 14.4 using the delay line approach.

Solution: For the LPF of Example 14.4, the cut-off frequency was 3.4 kHz and the desired gain at dc was 5 dBs. Hence, comparison of equation (14.33) with equation (14.31) gives a = 38 krad/s and b = 21.3714 krad/s. Substitution of the values of a and b in equation (14.36) for the selected clock frequency f_s = 32 kHz, gives the following relation:

$$V_o = -0.4451V_{\text{in}} - 0.4451V_{\text{in}}z^{-1} + 0.4993V_o z^{-1} \tag{14.37}$$

For the implementation of equation (14.37) in the form of Figure 14.17(b), the netlist is shown in Figure 14.18. Since this realization does not require half the delay time, delay lines of only full delay time were used. The selected value of the clock frequency being 32 kHz, T = 31.25 μs. With $k_1 = k_3$ = 0.4451, and B = 0.4993, gain values of the amplifiers used and resistances employed are mentioned in Figure 14.18 and the PSpice simulated response is shown in Figure 14.19. This gives a dc gain of 1.778 and a cut-off frequency of 3.28 kHz (20.63 krad/s). A small difference between the simulated and the theoretical cut-off frequency is due to the warping effect of the BLT. To effectively overcome this problem, equation (14.26) is used to get the pre-warped values of constants a and b as:

$$b^* = 64 \times 10^3 \tan\left(\frac{3.4 \times 2\pi \times 10^3 \times 180}{64 \times 10^3 \times \pi}\right) = 22.193 \text{ krad/s and}$$
$$a^* = 1.778 \times b^* = 39.457 \text{ krad/s} \tag{14.38}$$

```
*FIRST-ORDER LOW PASS
.SUBCKT DEL 1  2  4
*CLOCK PERIOD   T=31.25US
E11 3  0  1  2  1
T1  3  0  4  0  ZO=50  TD=31.25US
RT  4 0   50
.ENDS  DEL
*WITHOUT PRE-WARPING
VS   1  0  AC  1
E1   2  0  1  0  0.4451
E2   10  0  1  0  0.4451
X1   10  0  11  DEL
E4   12  0  11  0 1
R23   2  3  1K
R133   12  3  1K
E3   4  0  0  3  1E+5
E5   6  0  4  0  -1
```

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```
X3     6   0   7   DEL
R7     3   4   1K
E6     9   0   7   0   1
R93    9   3       2.0026K
.AC    DEC   100   10    100K
.PROBE
.END
```

Figure 14.18 Netlist for the first-order low pass filter of Example 14.5 without pre-warping.

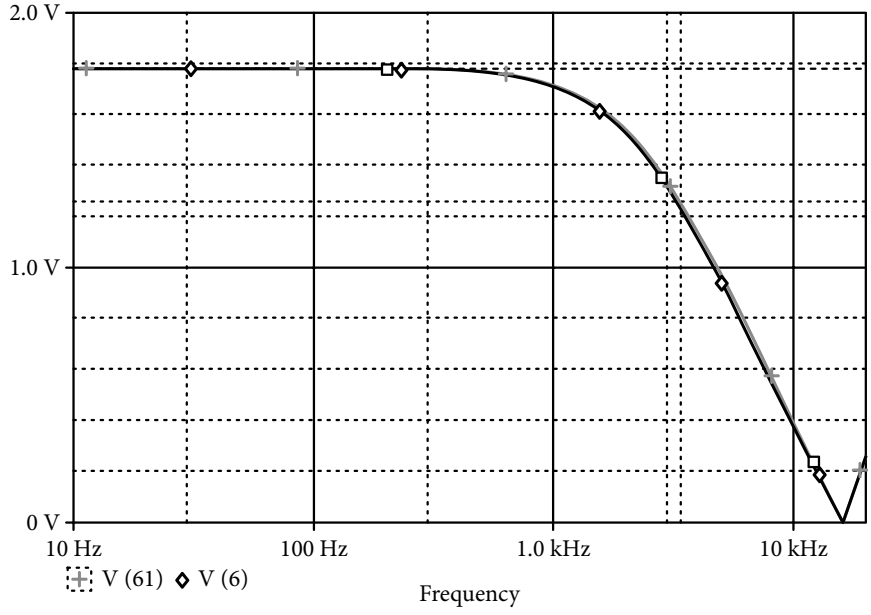

Figure 14.19 Simulated response of the first-order low pass filter for Example 14.5.

Use of the parameters in equation (14.38) gives new values of the coefficients as $k_1 = k_3 = 0.4581$ and $B = 0.4849$. PSpice simulation using these coefficients in the original netlist gives the simulated dc gain of 1.779 and cut-off frequency of 3.412 kHz, as designed is also shown in Figure 14.19.

Example 14.6: Simulate the second-order transfer function $H(z)$ in equation (14.30) using the delay line approach.

Solution: Transfer function $H(z)$ has been obtained for a BPF having the following specifications: $\omega_o = 15$ krad/s, $Q_o = 10$ and $H_{BP} = 10$. Equation (14.30) can be written as:

$$V_{out}(1 - 1.13836z^{-1} + 0.9225z^{-2}) = 0.5183(1 - z^{-2})V_{in} \tag{14.39}$$

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Comparing equation (14.39) with equation (14.36), it can be written as:

$$V_{out} = k_1 V_{in} - k_5 V_{in} z^{-2} + B V_{out} z^{-1} - D V_{out} z^{-2} \tag{14.40}$$

In equation (14.40), $k_1 = -k_5 = 0.5183$, $B = 1.13836$ and $D = -0.9225$

Figure 14.20(a) shows a network implementing equation (14.40) for the realization of the BP function in terms of delay lines and amplifiers. The simulated response of the BPF is shown in Figure 14.20(b). The obtained center frequency is 2.343 kHz (14.72 krad/s), with a mid-band gain of 11.11 and a bandwidth of 243 Hz, resulting in pole-Q = 9.64.

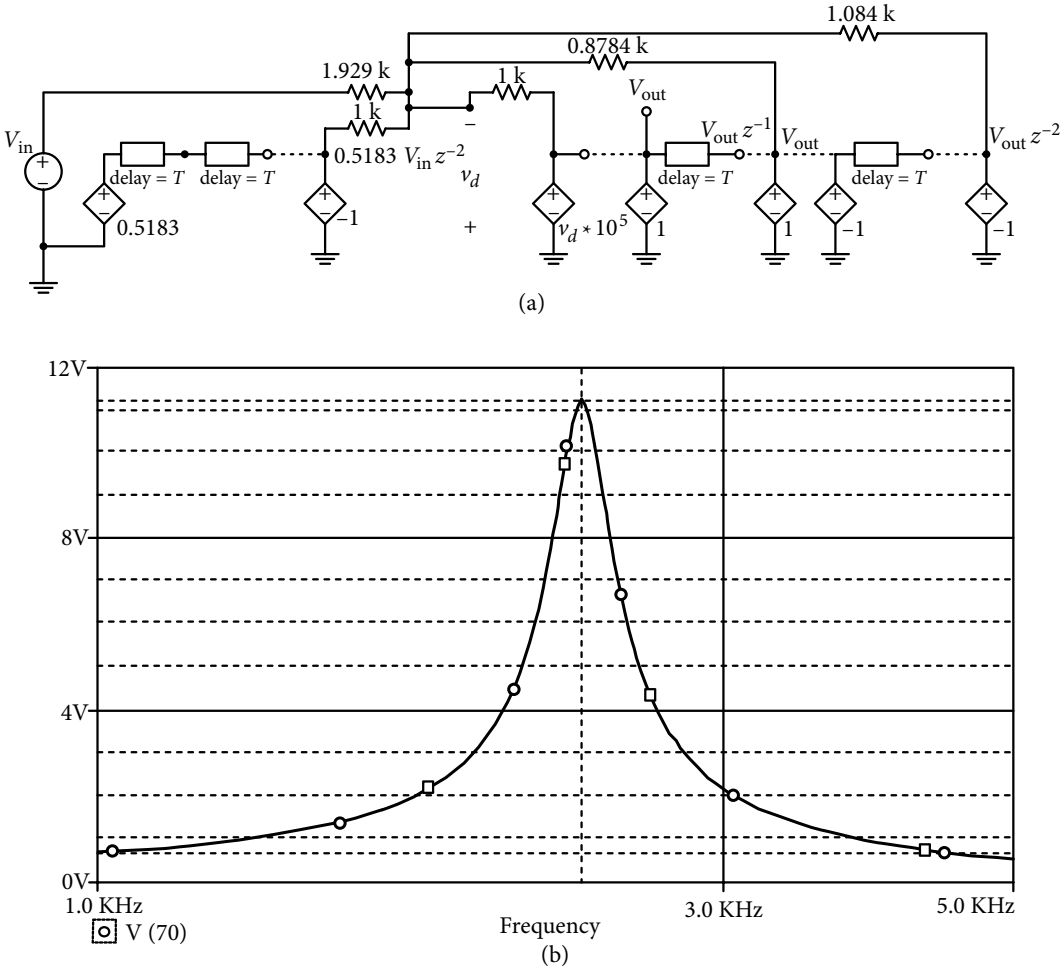

Figure 14.20 (a) Delay line-based simulation network for the second-order z domain transfer function in Example 14.6. (b) Simulated response in Example 14.6.

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Example 14.7: Design and simulate a BPF with the following specifications:

$\omega_o = 2\pi(3.4)$ krad/s, $Q = 5$ and $h_{\text{obp}} = 10$

Solution: The filter's transfer function in the s domain will be:

$$H_{\text{BP}}(s) = \frac{2\pi(6.8)10^3 s}{s^2 + 2\pi(0.68)10^3 s + \{2\pi(3.4)10^3\}^2} \tag{14.41}$$

Using equation (14.26), with the selected value of clock frequency $f_c = 16$ kHz, pre-warped center frequency will be:

$$\omega_o^* = 32000 \tan\left(\frac{21371.4}{32000}\frac{180}{\pi}\right) = 25226.7 \text{ rad/s.} \tag{14.42}$$

With $Q = 5$, bandwidth will be $\omega_o^* / 5 = 5045.3$ rad/s.

Using equations (14.24)–(14.27) and Table 14.1, z parameters are calculated as:

$$D(z) = \left\{32^2 + 32 \times 5.045 + 25.226^2\right\}10^6 = 1821.8 \times 10^6 \tag{14.43 a}$$

$$a_{1D} = \frac{2(32^2 - 25.226^2)10^6}{1821.8 \times 10^6} = 0.4255 \tag{14.43 b}$$

$$a_{2D} = \frac{1498.9 \times 10^6}{1821.8 \times 10^6} = 0.8227, \; h_D = \frac{1614.5 \times 10^6}{1821.8 \times 10^6} = 0.8862 \tag{14.43 c}$$

From parameter values in equation (14.43), z-domain transfer function becomes as:

$$\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{0.8862\left(1 - z^{-2}\right)}{1 - 0.4255z^{-1} + 0.8227z^{-2}} \tag{14.44}$$

Hence, the output voltage may be written as given below, where output voltage contains terms involving output voltage as well:

$$V_{\text{out}} = 0.8862\left(1 - z^{-1}\right)V_{\text{in}} + 0.4255V_{\text{out}}z^{-1} - 0.8227V_{\text{out}}z^{-2} \tag{14.45}$$

Figure 14.21 (a) shows representation of equation (14.45) in terms of delay lines. PSpice simulated response is shown in Figure 14.21 (b), wherein center frequency is 3.324 kHz, h_{obp} = 8.52 and bandwidth is 568.8 Hz, resulting in $Q = 5.84$.

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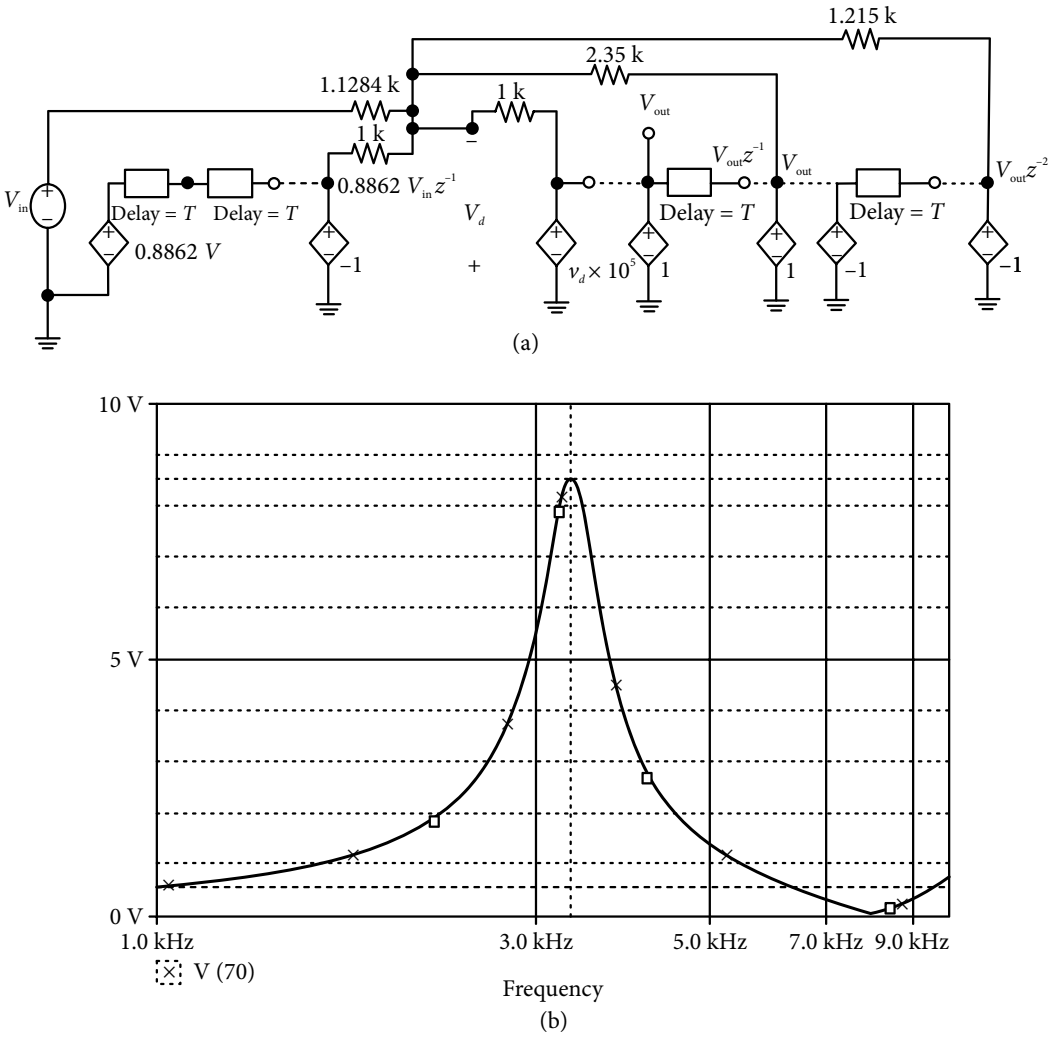

Figure 14.21 (a) Delay line-based simulation network for the second-order z-domain transfer function in Example 14.7, (b) simulated response of the network in Figure 14.21(a).

Practice Problems

14-1 An LPF is to be designed having a cut-off frequency of 250 Hz. Find the resistance values to be used, if the maximum value of the capacitor to be employed is 10 pF. Convert the active RC filter into a switched capacitor filter using a clock frequency of 256 kHz. What will be the size of the capacitor simulating the resistor?

14-2 Design a first-order ideal LP structure to get an output voltage of 1 V peak-to-peak, for a sine wave input having a peak value of 1 V at a frequency of 2.5 kHz. What will be the output voltage if a parasitic capacitance of 2 pF is present in parallel with the capacitor simulating the input resistance?

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14-3 Design and test a switched capacitor inverting integrator for the given input voltages: $v_1 = 3\sin(2\pi \times 10^3)$, $v_2 = 4\sin(2\pi \times 10^3)$ and $v_3 = 2\sin(2\pi \times 10^3)$. The respective weightage of the input voltages is (i) 1, 0.5 and 1.5 (ii) equal weightage.

14-4 Repeat Problem 14-3 if a 2pF parasitic capacitance is also present with each capacitor simulating the resistances.

14-5 Repeat Problem 14-3 for v_3 being subtracted instead of added to the inputs v_1 and v_2.

14-6 Repeat Problem 14-5 if a 2pF parasitic capacitance is also present with each capacitor simulating the resistances.

14-7 Design a first-order switched capacitor LPF to get the difference of two voltages v_1 and v_2. v_1 is to be multiplied by 3 dB and v_2 by 2 dB. The LPF should have a cutoff frequency of 1.59 kHz; assume clock frequency as 64 kHz.

14-8 Sketch the equivalent OA-RC circuit and find the transfer function for the circuit shown in Figure P-14.1. Element values in the OA-RC circuit are: $R_2 = R_3 = 50\ \text{k}\Omega$, $C_1 = 0$ and $C_4 = 2$ nF. Also find the transfer function of the equivalent discrete-time filter if the sampling frequency is 64 kHz.

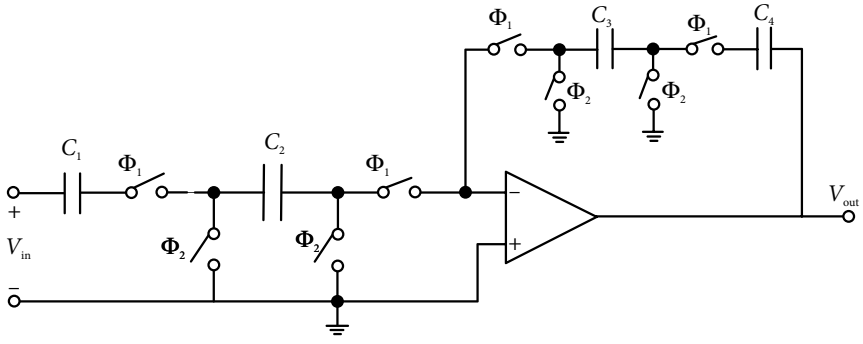

Figure P14.1

14-9 Repeat Problem 14-8 for $C_1 = 2$ nF.

14-10 Obtain the sample data transfer function for the following s domain function by applying bilinear transformation. Use a clock frequency of 32 kHz.

$H(s) = N(s)/D(s)$, $N(s) = 1.25 \times 10^4\, s$, $D(s) = s^2 + 2500s + 6.25 \times 10^8$

14-11 Repeat Problem 14-10 for $N(s) = 1.25\, s^2$.

14-12 Repeat Problem 14-10 for $N(s) = 1.25 \times 10^8$.

14-13 Repeat Problem 14-10 for $N(s) = 1.25(s^2 + 10^8)$.

14-14 Design the LPF of Figure 14.14 having a 3 dB frequency of 1.5 kHz and 6 dB gain at dc. Convert it to a switched capacitor form with a clock frequency of 128 kHz. Find the voltage gain of the OA-RC and the switched capacitor filters at 150 Hz, 1.25 kHz, 1.5 kHz, 1.75 kHz and 5 kHz.

14-15 Simulate the first-order switched capacitor LPF of Problem 14-14 using the delay line approach.

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14-16 Simulate the first-order switched capacitor LPF of Problem 14-10 using the delay line approach.

14-17 Simulate the first-order switched capacitor LPF of Problem 14-11 using the delay line approach.

14-18 Simulate the first-order switched capacitor LPF of Problem 14-12 using the delay line approach.

14-19 Simulate the first-order switched capacitor LPF of Problem 14-13 using the delay line approach.

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