Chapter 15

Operational Transconductance Amplifier-C Filters

15.1 Introduction

Operational transconductance amplifiers (OTAs) have emerged as a powerful alternative to OAs because of their current mode (CM) nature. Their CM nature allows OTAs to be used for much higher frequencies. Another major advantage of using OTAs is the electronic control it has over trans-conductance, which allows much easier tuning of filter parameters. The fact that only OTAs and capacitors are needed also makes the filter attractive for monolithic integrated circuit fabrication.

Since the development of OA-RC filter design is well established and extensively studied, it has been used to advantage while using OTAs. Filter design using OTAs follow a similar pattern and design procedures used in OA-RC synthesis; however, they are tailored to specific needs as will be shown in this chapter.

A brief review of the basic building blocks using OTAs is provided in Section 15.2. Simulation of grounded and floating resistors, inverting and non-inverting integrators, addition of voltages (and currents) and voltage amplifiers, for their stand-alone use or their application for realizing filter sections is included. First-order LPFs (low pass filter) and HPF (high pass filter) design is shown in Section 15.3 using integrators. Because of the suitability of OTA based circuits for differential outputs, the filter circuits discussed in Section 15.3 are then converted to differential mode. Similar to OA-RC synthesis, second-order filters are realized using the two-integrator loop method. Higher-order filters are realized using the *element substitution method* through the simulation of inductances and capacitances in Section 15.6 and 15.7. Filter realization using operational simulation is also discussed in Section 15.8.

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15.2 Basic Building Blocks Using OTAs

OAs have been used for inverting and non-inverting amplification, summation (subtraction), integration and differentiation. In addition, while designing filters, OAs have been extensively used for simulating inductors and FDNRs (frequency dependant negative resistors). OTAs have also been used for all such entities; in addition, they are used for simulating grounded resistances (GRs) and floating resistances (FRs) as well. Hence, the resulting OTA-C circuits are not only realizable, but preferred as it makes them easily integratable in the monolithic form with more precise filter parameters.

To study and realize OTA based circuits, we will be using the circuit symbol, its ideal and first-order non-ideal model shown in Figure 15.1(a–c), where r_i, C_i and r_o, C_o are parasitic elements and g_m is trans-conductance.

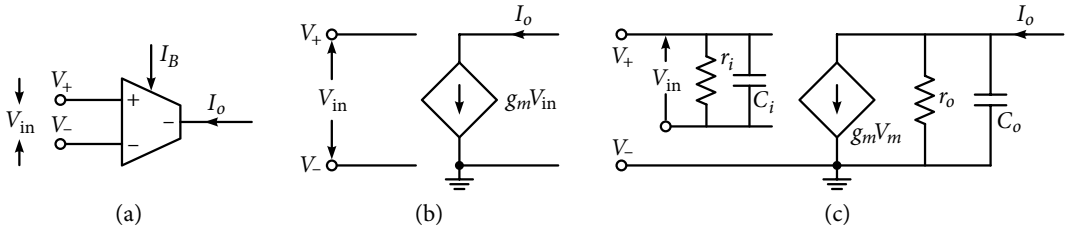

Figure 15.1 (a) Symbol of a single-ended OTA; (b) model of an ideal OTA; and (c) simple model of a non-ideal OTA.

15.2.1 Resistor simulation

The number of resistances used may not be large in a filter circuit, but these cannot be avoided and needs to be fabricated or simulated. It will be observed that the positive or negative resistor in the grounded or floating form can be easily simulated using a single OTA (or possibly two for a floating resistor) and the value of the resistor is controllable through the biasing current (or voltage) which changes trans-conductance (g_m) of the OTA. The external control of g_m is a great advantage in integrated circuits where it is not possible to make changes in elements after fabrication. Resistance realization through g_m saves considerable chip area as well compared to fabrication of large value resistors using diffusion or metal deposition. Another important advantage of such realizations is that they track with active devices.

In one of the simplest realizations, Figure 15.2 shows the simulation of a GR with one of its terminals connected to the ground. Assuming OTA as ideal for the circuit shown in Figure 15.2, the current–voltage relation is:

$$I_o = I_1 = (V_{\text{in}} - 0)g_m \rightarrow Z_{\text{in}} = (V_{\text{in}}/I_1) = 1/g_m \tag{15.1}$$

Meaning thereby that it realizes a resistor having a value $1/g_m$. If the input voltage is applied at the non-inverting terminal, the simulated resistance becomes negative, $-1/g_m$.

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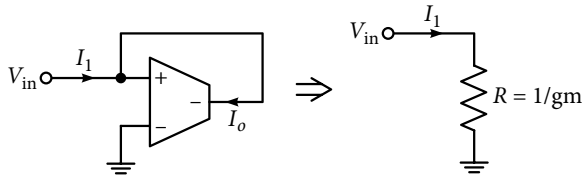

Figure 15.2 Grounded resistance simulation.

To realize an FR, a commonly used procedure of lifting a terminal off the ground in a GR can be used. The resulting circuit, using two such circuits in back-to-back form is shown in Figure 15.3. Once again, assuming ideal OTAs, currents are given as:

$$I_1 = I_{o1} = g_{m1}(V_1 - V_2),\ I_2 = I_{o2} = g_{m2}(-V_1 + V_2) \tag{15.2}$$

Equation (15.2) yields the following admittance matrix, which represents a floating element.

$$[y] = \begin{bmatrix} g_{m1} & -g_{m1} \\ -g_{m2} & g_{m2} \end{bmatrix} = g_m \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \tag{15.3}$$

For $g_{m1} = g_{m2} = g_m$, the realized element is an FR having value $(1/g_m)$. An alternate scheme for simulating an FR using differential OTA will be taken up later.

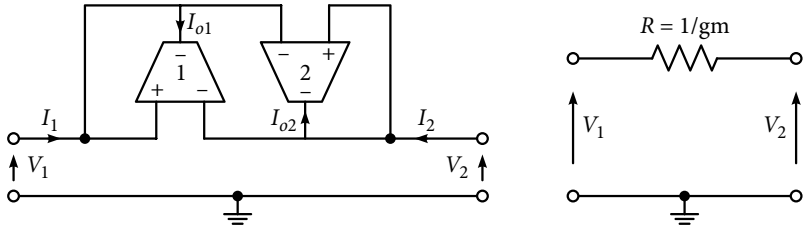

Figure 15.3 Simulation of floating resistance with two OTAs.

Simulation of GR and FR is highly advantageous as it converts active RC circuits to active C only and large value resistors are realized using only a small chip area.

15.2.2 Integrators

Integrators are required in both inverting and non-inverting mode; with or without loss. As the OTA output is current, it acts as an integrator when it terminates in a capacitor as shown in Figure 15.4(a). With OTA taken as ideal, the output voltage is easily obtained as:

$$V_{out} = -(I_o/sC) = -(V_+ - V_-)\ (g_m/sC) = -V_{in}(g_m/sC) \tag{15.4}$$

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This means that the circuit integrates the input voltage, $V_{in} = (V_+ - V_-)$, without loss in the inverting mode. This basic integrator circuit leads very easily to a non-inverting integrator, with or without loss, and an inverting integrator with loss; a big advantage with circuits realized using OTAs. All the four structures are also available in differential output mode; an attractive and sometimes an essential feature as will be shown later.

If the input voltage V_{in} is applied at the inverting terminal with the non-inverting terminal grounded, the circuit realizes a lossless non-inverting integrator. In addition, either of the integrators become lossy if the terminating impedance contains a resistor in addition to the capacitor. Figure 15.4(b) shows such a configuration for a non-inverting integrator. The terminating resistor being simulated by OTA-2 has transconductance g_{m2}, and its transfer function is given as:

$$(V_{out}/V_{in}) = g_{m1}/(sC + g_{m2}) \tag{15.5}$$

Interchange between input terminals in either one of the OTAs will convert it to a lossy inverting integrator.

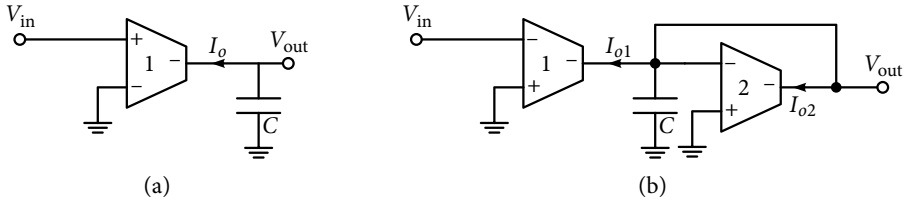

Figure 15.4 (a) Inverting ideal integrator and (b) non-ideal non-inverting integrator.

As of now, expressions have been derived without any parasitic element in the OTA model. Quite often it becomes essential to include the first-order parasitic because their value may not be negligible in comparison to the physical elements used. The commonly used OTA-3080, whose pin connection diagram is shown in Figure 15.5 and a first-order non-ideal model which was shown in Figure 15.1(c) has the following typical parameters when tested at bias current I_B = 500 μA and at full operating temperature: input resistance r_i = 26 kΩ, input capacitance C_i = 3.6 pF, output resistance r_o = 1.5 MΩ, and output capacitance C_o = 5.6 pF, forward transconductance g_{mo} = 5400 μS, and peak output current is 300 μA.

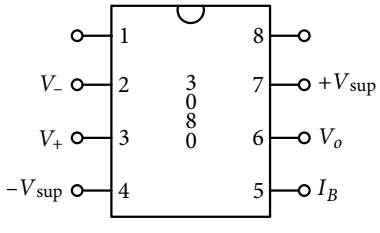

Figure 15.5 Pin connection diagram of the commonly available OTA-3080.

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If the OTA is represented by its first-order model, the small signal equivalent circuit of the inverting integrator shown in Figure 15.4(a) becomes as shown in Figure 15.6; the input resistance is neglected as it is very high. The transfer function becomes:

$$\frac{V_o}{V_{\text{in}}} = -\frac{g_m}{s(C + C_o) + g_o} \tag{15.6}$$

Hence, the total effective load capacitance is increased by the parasitic output capacitance C_o and the output resistance ($r_o = 1/g_o$) makes it a bit lossy resulting in a 3 dB frequency $f_{3\text{dB}} = \{1/2\pi(C + C_o)r_o\}$, and a dc gain of $g_m r_o$.

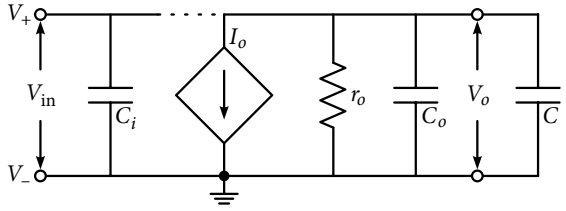


Figure 15.6 Small signal equivalent circuit of the OTA based integrator of Figure 15.4(a).

Figure 15.7(a) shows the small signal equivalent circuit of the lossy non-inverting integrator of Figure 15.4(b) with important parasitic elements. Here the current–voltage relations are:

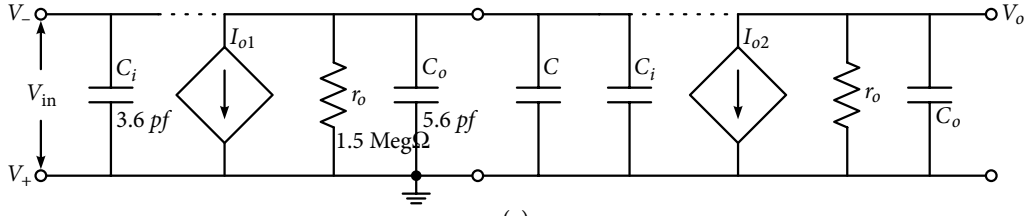
$$I_{o1} = -g_{m1} V_{\text{in}},\ I_{o2} = g_{m2} V_o,\ V_o = -(I_{o1} + I_{o2})/(C + 2C_o + C_i)s + 2g_o \tag{15.7}$$

It gives the transfer function as:

$$\frac{V_o}{V_{\text{in}}} = \frac{g_{m1}}{(C + 2C_o + C_i)s + g_{m2} + g_o} \tag{15.8}$$

Its 3 dB frequency and the dc gain expressions are obtained as:

$$f_o = (g_{m2} + g_o)/2\pi(C + 2C_o + C_i) \text{ and gain} = g_{m1}/(g_{m2} + 1/r_o) \tag{15.9}$$



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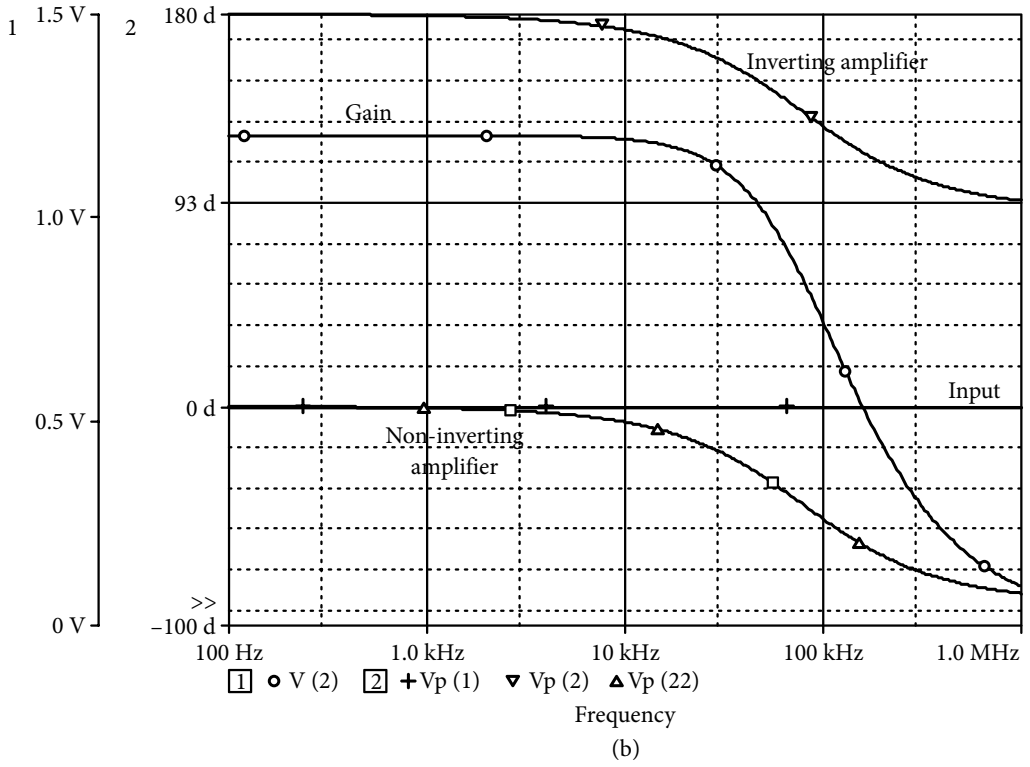

Figure 15.7 (a) Small signal equivalent circuit of the non-ideal non-inverting integrator of Figure 15.4(b). (b) Magnitude response of the non-inverting integrator of Example 15.1 and phase responses of the non-inverting and the inverting integrators, with input applied at the inverting and non-inverting terminals, respectively.

Example 15.1: Design a non-inverting integrator using the circuit shown in Figure 15.4(b), having a 3 dB frequency of 500 krad/s and a dc gain of 1.2.

Solution: Using the aforementioned parameters of the OTA and assuming g_{m2} = 4 mS, equation (15.9) representing equivalent circuit of Figure 14.4(a) with parasitics gives:

$$(C + 2C_o + C_i) = (g_{m2} + r_o)/2\pi f_o = (4 \times 10^{-3} + 1/1.5 \times 10^6)/(5 \times 10^5) = 8.0013 \text{ nF}$$

Substituting the values of the parasitic capacitances, the required value of the physical capacitance C = 7.9865 nF, and for the desired dc gain of 1.2, the required g_{m1} = 4.808 mS. Using these element values in the circuit shown in Figure 15.4(b), the magnitude response was simulated using PSpice.

Figure 15.7(b) shows the magnitude response as having a 3 dB frequency of 79.83 kHz (501.7 krad/s) and a dc gain is 1.2. Figure 15.7(b) also shows the phase response; there is no phase difference with the input at low frequencies, confirming that the circuit is a non-inverting integrator.

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The non-inverting integrator can be easily converted into the inverting form by applying input at the non-inverting terminal. Its phase response, also shown in Figure 15.7(b), confirms the integrator as inverting, having a phase difference of 180° at low frequencies.

15.2.3 Current and voltage addition

As the output of the OTA is current, a number of output currents can be added (or subtracted) at a junction in a simple way. The same is the case with voltages; of course, through the means of output currents. For example, as shown in Figure 15.8(a), two voltages V_1 and V_3 can be added and V_2 subtracted therefrom, through the choice of input terminals. It is important to note that in this circuit, output current flows in a grounded resistor realized by OTA-4. Using the ideal model for the OTAs, we get the following relations.

$$I_{o1} = g_{m1}\, V_1,\ I_{o2} = -g_{m2}\, V_2,\ I_{o3} = g_{m3}\, V_3, \text{ and } I_{o4} = g_{m1}\, V_1 - g_{m2}\, V_2 + g_{m3}\, V_3 \tag{15.10}$$

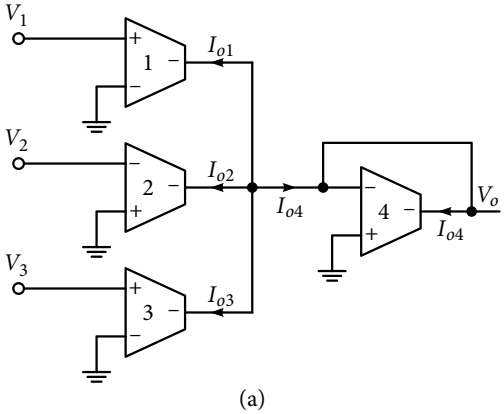
Addition (or subtraction) of currents is done easily, with weightage having unequal transconductance; without weightage, all transconductance are equal. With $I_{o4} = g_{m4} V_o$, we get:

$$V_o = \frac{g_{m1}}{g_{m4}} V_1 - \frac{g_{m2}}{g_{m4}} V_2 + \frac{g_{m3}}{g_{m4}} V_3 \tag{15.11}$$

Equation (15.11) provides scaled algebraic addition of voltages with different weights. If all transconductance are made equal, the relation will simplify as:

$$V_o = V_1 - V_2 + V_3 \tag{15.12}$$

It is obvious that the number of inputs can be increased easily.



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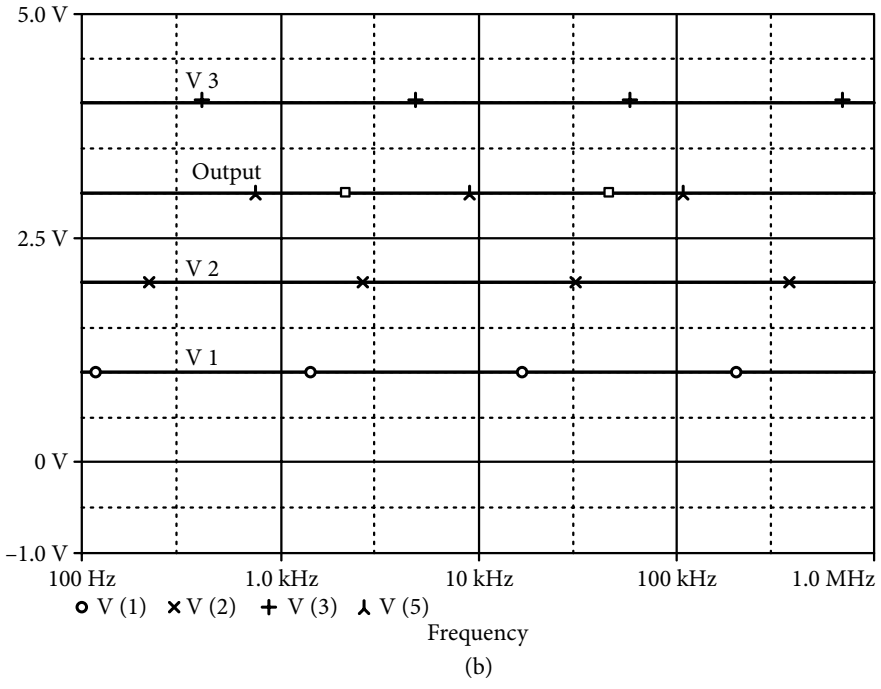

Figure 15.8 (a) Addition (and subtraction) of voltages through output currents. (b) Summing two voltages and subtracting the third voltage from it; input voltages have different weightages.

Example 15.2: Verify the summation circuit shown in Figure 15.8(a) for V_1 = 1.0 V, V_2 = –2.0 V and V_3 = 4.0 V, with a respective weightage of 1.0, 1.05 and 0.9.

Solution: If g_{m4} = 4 mS, for the given weightages, g_{m1} = 4 mS, g_{m2} = 4.2 mS and g_{m3} = 3.6 mS. With the respective voltages applied in the circuit shown in Figure 15.8(a), the output voltage becomes 2.5 V; confirmed in Figure 15.8(b). Performance can be repeated with equal weightage to input voltage, with all transconductance being equal. It can be observed that summation of voltages is valid at large frequencies as well.

15.2.4 Voltage amplifiers

If output current I_o of an OTA flows in a resistance, its output becomes a voltage amplifier. Figure 15.9 shows OTA-1 having transconductance g_{m1} loaded with OTA-2 forming a load resistor. The current–voltage relations are:

$$I_{o1} = g_{m1}\, V_{\text{in}},\ I_{o2} = -I_{o1} \text{ and } V_{\text{out}} = (I_{o2}/g_{m2}), \text{ or } (V_{\text{out}}/V_{\text{in}}) = (-g_{m1}/g_{m2}) \tag{15.13}$$

The circuit shown in Figure 15.9 realizes an inverting amplifier; the amplification is controllable by a single transconductance only. To get a non-inverting amplifier, only one of the input terminals needs to be swapped.

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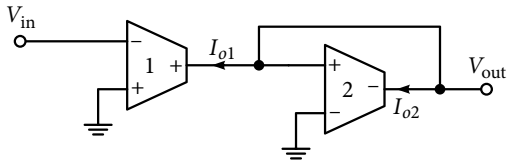

Figure 15.9 Inverting amplifier; easily convertible to non-inverting mode.

15.3 First-order Sections

The lossy integrator of Figure 15.4(b) acts as a first-order LP section. If the transconductance of the two OTAs is different, it provides the variable dc gain = g_{m1}/g_{m2}. If the variable gain is not essential, an alternate circuit shown in Figure 15.10(a) also serves as lossy integrator or a first-order LP section with the following relation:

$$V_{out} = -V_{in}\, g_m/(g_m + sC) \tag{15.14}$$

The non-inverting LP section is obtained by interchanging input and output terminals.

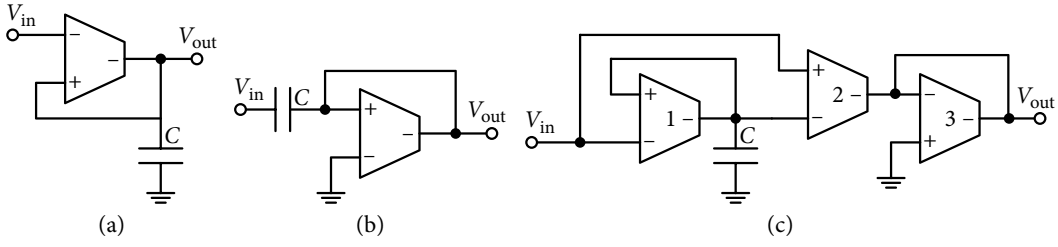

Figure 15.10 (a) First-order low pass section with unity dc gain. (b) First-order high pass section using a floating capacitor and (c) using a grounded capacitor.

The first-order HP section is obtained by either using a floating capacitor or a grounded capacitor as shown in Figure 15.10(b) and (c). Their respective transfer functions are:

$$\frac{V_{out}}{V_{in}} = \frac{sC}{(sC + g_m)} \tag{15.15a}$$

$$\frac{V_{out}}{V_{in}} = \frac{sC}{(sC + g_{m1})}\frac{g_{m2}}{g_{m3}} \tag{15.15b}$$

The first-order HP behaves like a lossy differentiator. A lossless differentiator cannot be realized directly as obvious from the expressions in equation (15.15). Hence, the technique shown in Figure 15.11 is applied, wherein a lossless integrator is connected in the feedback path of an amplifier. Its output voltage is obtained as:

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$$V_o = -\frac{g_{m3}}{g_{m1}g_{m2}} sC V_{\text{in}} = -\left(\frac{sC}{g_m}\right) V_{\text{in}} \text{ for equal transconductance} \tag{15.16}$$

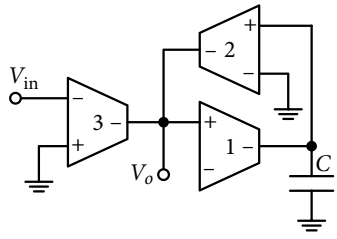

Figure 15.11 A lossless differentiator using feedback in an amplifier circuit.

Example 15.3: (a) Design an HP filter having a 3 dB frequency of 480 krad/s using the circuit shown in Figure 15.10(b).

(b) Design an HP filter using the circuit shown in Figure 15.10(c), with a 3 dB frequency of 50 kHz and a high frequency gain of 1.6.

Solution: (a) The circuit uses a floating capacitor and realizes a fixed gain of unity at high frequencies. From equation 15.15(a), if capacitor C is selected as 10 nF, the required g_m = 4.8 mS. Employing these elements, the simulated response of the circuit is shown in Figure 15.12; cut-off frequency is obtained as 76.45 kHz (480.54 krad/s).

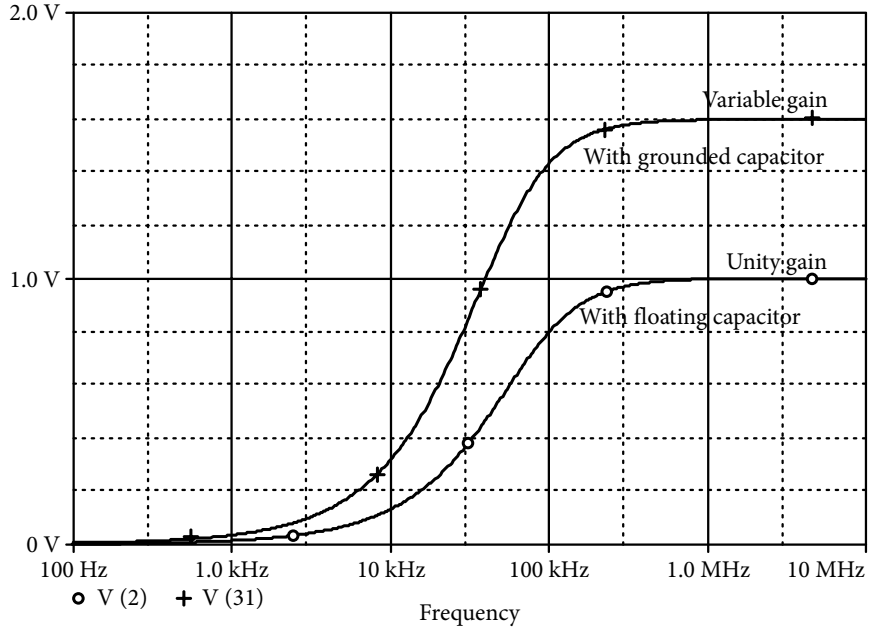

Figure 15.12 Simulated response of first-order high pass filter with a high frequency gain of unity using a floating capacitor of Figure 15.10(c) and an OTA and a variable high frequency gain high pass filter using a grounded capacitor and three OTAs of Figure 15.11.

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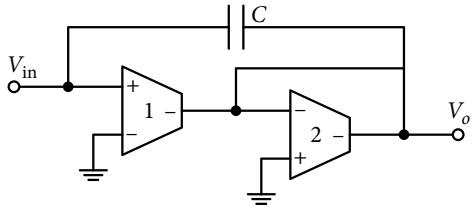
(b) From equation 15.15(b), for a selected value of capacitor C of 10 nF, required g_{m1} = 3.1428 mS, and for a high frequency gain of 1.6, with g_{m2} = 4 mS required, g_{m3} = 2.5 mS. Figure 15.12 shows the simulated response, having a cut-off frequency of 50.105 kHz and gain of 1.6; the response is not constrained to have only unity gain.

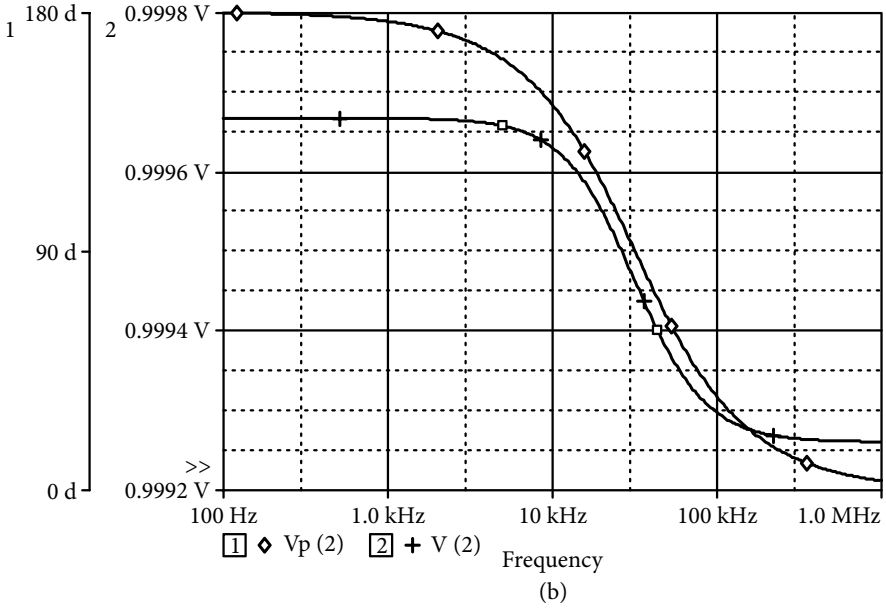
Example 15.4: Realize an APF (all pass filter) such that it has a phase shift of 90° at 200 krad/s.

Solution: A first-order APF section is shown in Figure 15.13(a), for which the transfer function is obtained as:

$$\frac{V_o}{V_{\text{in}}} = \frac{sC - g_{m1}}{sC + g_{m2}} \tag{15.17}$$



(a)



(b)

Figure 15.13 (a) First-order all pass section; (b) Magnitude and phase response of the all pass filter circuit.

Using non-ideal OTAs with the parasitic elements as mentioned in Section 15.2.2, an equal transconductance value of 4 mA/V is selected for realizing the APF. For the desired parameters

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required value of C = 20 nF. The circuit is simulated and its response in Figure 15.13(b) shows that the magnitude is almost unity, as its variation is only from 0.9997 V to 0.9993 V. Phase response is also shown in Figure 15.13(b), which starts dropping from 180° to zero and becomes 90° at 31.845 kHz (200.04 krad/s).

Figure 15.14 shows a general first-order section having the following transfer function with $C_1 = \alpha C$ and $C_2 = (1 - \alpha) \times C$.

$$\frac{V_{out}}{V_{in}} = \frac{s\alpha C + g_{m1}}{sC + g_{m2}} \tag{15.18}$$

The previously discussed LP (low pass) section of Figure 15.4(b), the HP (high pass) section of Figure 15.11(a) and the AP (all pass) section of Figure 15.13 are easily shown as special cases of this general first-order section.

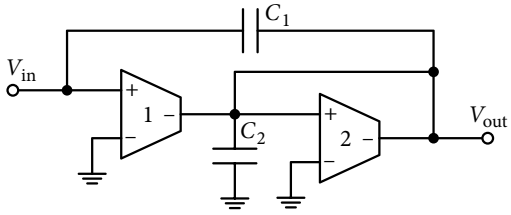

Figure 15.14 A general first-order section.

15.4 Single-ended to Differential Output Conversion

The advantages and requirements of using differential networks are well-known. These networks help in reducing common-mode noise considerably; though at the expense of more hardware. An added advantage in such circuits is the availability of the true output along with its inverted version; both the versions can possibly be used in the same network and elsewhere as well. Due to the desirability of fabricating linear filters on the same chip with digital circuits, the operating voltage of the filters had to be reduced which also requires reduction in the circuit noise. Hence, differential circuits became preferable and more common with OTAs. The reason being their inherent limited voltage–signal level capability, and more importantly, reduction in noise. Moreover, realization of a differential structure is simpler in OTA based networks compared to (say) OA based circuits.

For generating a differential output structure, a mirror-image circuit is combined with its original, in which each input and output sign is reversed; all non-essential circuitry is eliminated. Simultaneous change in the sign of the input and output does not affect the realized function. While combining the original and its mirror image, the input voltage is effectively doubled; this means that the output current is doubled. If a doubled output current flows in any capacitor, it doubles the voltage across it. To avoid this doubling of voltage, the capacitor

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value needs to be doubled. However, while adjustment of non-essential circuitry is done, a few capacitors can also be connected in differential mode; consequently, the total capacitance gets reduced. The following example will help illustrate the process.

Example 15.5: Develop a differential output, general first-order section from Figure 15.14.

Solution: Mirror image of the general first-order section of Figure 15.14 is drawn in Figure 15.15(a) with all input/output terminals interchanged; the input voltage becomes $-V_{\text{in}}$, and the output voltage becomes $-V_o$. They are combined with the original circuit of Figure 15.14, which results in Figure 15.15(b). The current–voltage relations of the circuit are:

$$I_{o1} = \{-V_{\text{in}} - (V_{\text{in}})\}\, g_{m1},\ \ I_{o2} = \{-V_o - (V_o)\} g_{m2} \tag{15.19}$$

As currents are doubled, charging of capacitors is also doubled; hence, doubling of capacitor values give:

$$I_{o1} + I_{o2} = 2sC_1\,(V_o - V_{\text{in}}) - 2sC_2\,V_o \tag{15.20}$$

Combining equations (15.19) and (15.20) with $C_1 = \alpha C$ $C_2 = (1 - \alpha)C$, we get:

$$\frac{V_o}{V_{\text{in}}} = \frac{sC\alpha + g_{m1}}{sC + g_{m2}} \tag{15.21}$$

As both the $2C_2$ capacitors are grounded, these can be connected in series, resulting in a single floating capacitor C_2 as shown in Figure 15.15(c). It gives an advantage of lesser overall capacitance from $4C_2$ to only C_2; but in floating mode.

With α = 1, equation (15.21) gives an APF with unity gain. For the selected value of $g_{m1} = g_{m2}$ = 5 mS and C = 2 nF, the circuit shown in Figure 15.15(c) is simulated, taking OTAs as non-ideal; $2C_1$ becomes 4 nF and C_2 is open circuited. Figure 15.15(d) shows that the magnitude is almost unity with variation from 0.9997 V to 0.9926 V only; the phase variations clearly depict the outputs in inverted and non-inverted forms.

An APF is to be designed with a low frequency gain of 1.1 and a high frequency gain of 0.5, with phase shift of 90° at 740 krad/s. For a high frequency gain of 0.5, α = 0.5 from equation (15.21), and for a low frequency gain of 1.1, if g_{m2} = 4 mA/V, it will require g_{m1} = 4.4 mA/V. With these values of α and transconductance, $2C_1$ = 4 nF and floating capacitor C_2 = 2nF. The designed APF was simulated and its magnitude response shown in Figure 15.15(e) verifies the designed voltage gains at low and high frequencies. The simulated response in Figure 15.15(e) shows a phase variation of 90° for both the true and false outputs at 117.9 kHz (741.35 krad/s).

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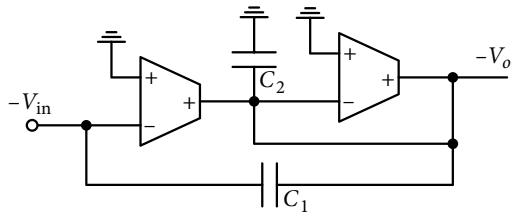
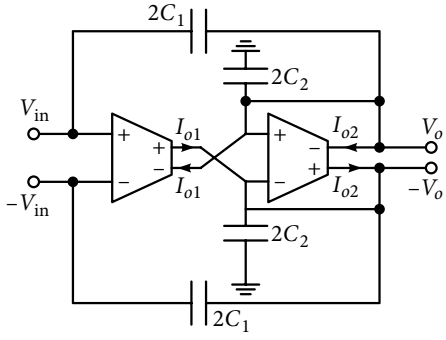


(a)



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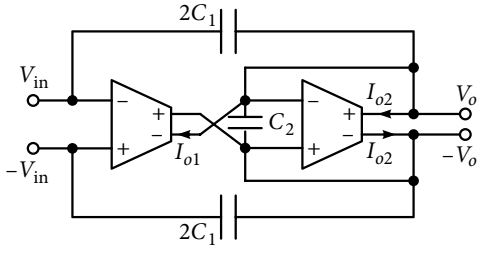

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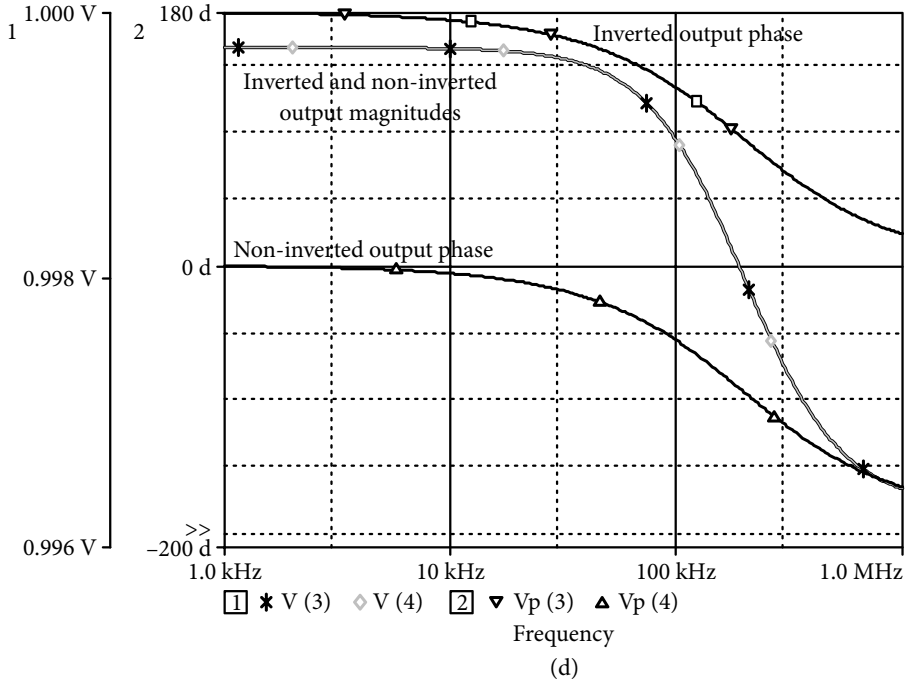

(d)

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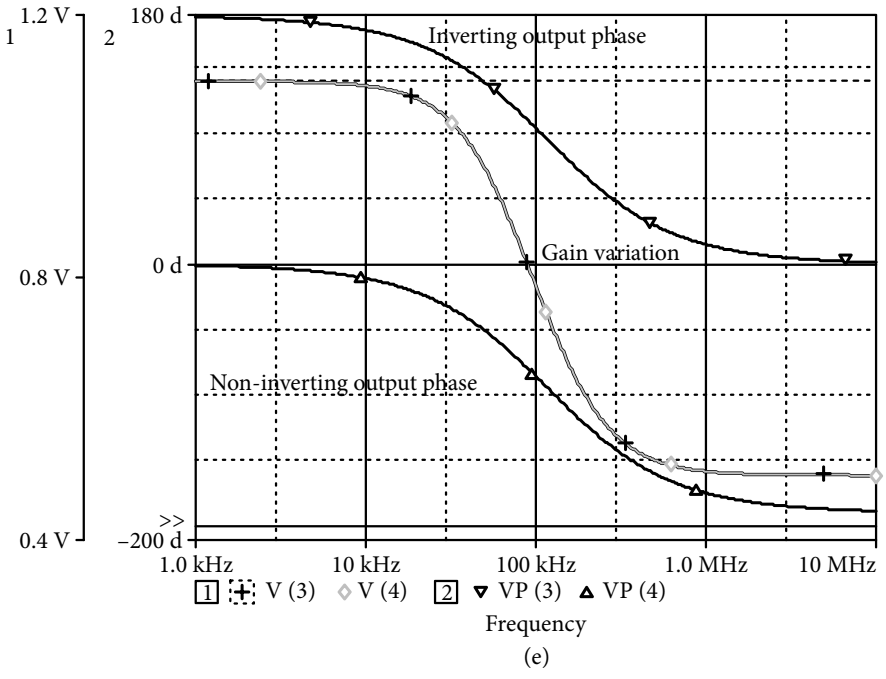

Figure 15.15 (a) Mirror image of the general first-order filter of Figure 15.14, (b) combination of Figures 15.14 and 15.15(a) with grounded capacitors $2C_2$, and (c) with floating capacitor C_2. (d) Magnitude and phase responses of the all pass filter using differential mode OTA in Figure 15.15(c) with C_2 open circuited. (e) Magnitude and phase responses of the all pass filter using the differential mode OTA shown in Figure 15.15(c).

15.4.1 Differential floating resistance and integrators

Floating resistance as simulated in Figure 15.3(c) using two single-output OTAs can also be realized using a single OTA with both outputs as shown in Figure 15.16(a). However, a differential resistance can be simulated as shown in Figure 15.16(b); which can become negative if the output terminals are interchanged.

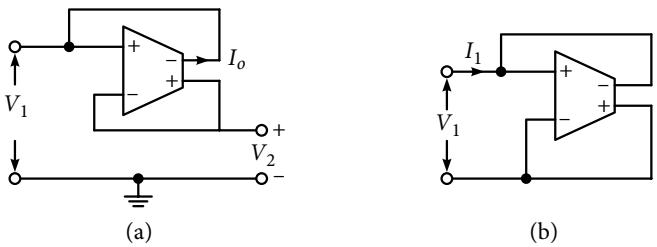

Figure 15.16 (a) Floating resistance simulation using single OTA and (b) a differential resistance simulation.

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To obtain a differential inverting amplifier, we begin with a single-ended inverting amplifier as shown in Figure 15.9, where the output current of OTA-1 passes through a grounded resistor realized with OTA-2. Gain of the amplifier was obtained as

$$(V_o/V_{in}) = -(g_{m1}/g_{m2}) \tag{15.22}$$

The circuit shown in Figure 15.17 is obtained by combining a mirror image of the circuit in Figure 15.9(a) with the original, while taking care of the proper input sign; the generated circuit has the same gain as given in equation (15.22), but is differential in nature.

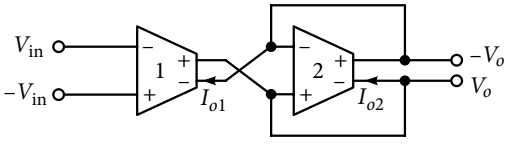

Figure 15.17 Inverting amplifier in differential mode.

In a similar way, the lossless integrator shown in Figure 15.4(a) will have a mirror image as shown in Figure 15.18(a), which can be combined with it. The resulting circuit will have either two grounded capacitors or one floating capacitor as shown in Figures 15.18(b) and 15.18(c), respectively. For Figure 15.18(a), the ratio of output to input voltage will be:

$$(-V_o/-V_{in}) = -(g_m/sC) \tag{15.23}$$

which is true for Figure 15.18(b) and (c) as well.

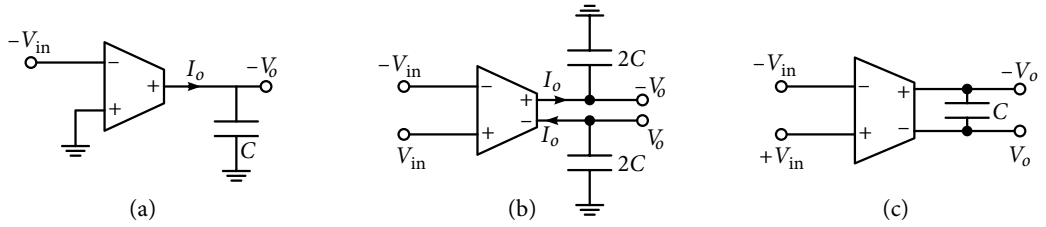

Figure 15.18 (a) Mirror image of the lossless integrator shown in Figure 15.4(a); (b) differential lossless integrator with two grounded capacitors and alternatively; (c) with one floating capacitor.

The lossy non-inverting integrator of Figure 15.4(b) can be converted into differential forms, with two grounded capacitors, and another with one floating capacitor, as shown in Figures 15.19(a) and (b), respectively. The corresponding transfer functions are the same as before in equation (15.5).

Example 15.6: Design a first-order LPF using the differential mode non-inverting amplifier shown in Figure 15.19(b) with the following specifications: cut-off frequency of 100 kHz with a dc gain of 1.6.

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Solution: From equation (15.5), to get a dc gain of 1.6, if g_{m2} = 2.5 mA/V, we need g_{m1} = 4 mA/V, and for a cut-off frequency of 100 kHz, value of the capacitor C will be = 2.5×10^{-3} /$2 \times 2 \times \pi \times 10^5$ = 1.9886 nF (floating capacitance in the circuit shown in Figure 15.19(b) is halved). The circuit is simulated and the responses are shown in Figure 15.19(c). The simulated dc gain is 1.6 and the cut-off frequency is 98.945 kHz. The small deviation in the cut-off frequency is due to the parasitic components as effective value of capacitance increases due to C_i, C_o and other capacitances. Phase response in Figure 15.19(c) shows no phase shift in the output V_o at low frequency and a phase shift of 180° for $-V_o$.

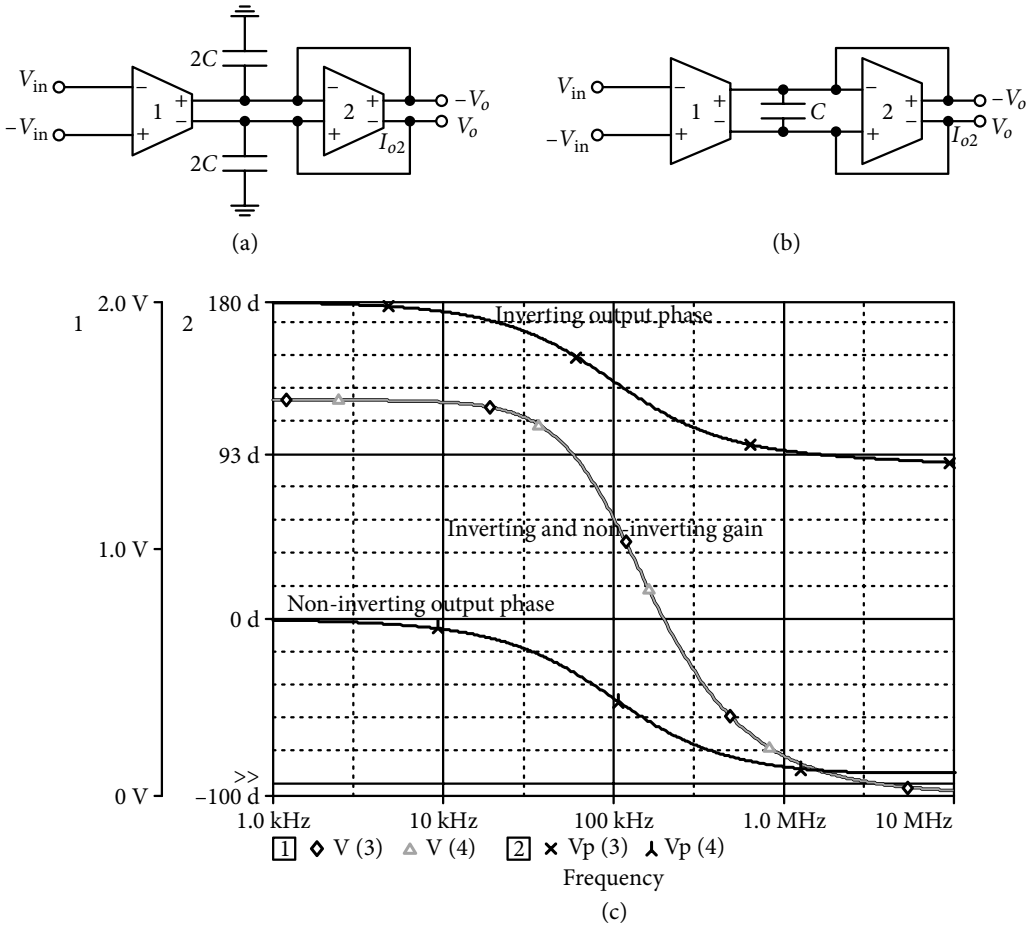

Figure 15.19 Combination of the non-ideal, non-inverting integrator shown in Figure 15.4(b) and its mirror image with (a) two grounded capacitors and (b) one floating capacitor. (c) Magnitude and phase responses of the non-inverting lossy integrator as a low pass filter from Figure 15.19(b).

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15.5 Second-order OTA-C Filters

There are different approaches through which second-order OTA-C filters are obtained. Most of these are based on the same techniques as those in the active RC synthesis using OAs. Since alternatives are available for any given filter specifications, there are certain criterion on the basis of which a particular structure or approach is preferred. Apart from the sensitivity considerations, a few other important considerations are taken into account with respect to the spread and value of capacitors and OTAs' transconductance, economy in terms of OTAs used, flexibility in obtaining as many types of responses from a single circuit and ease in tuning or programmability of the filter parameters.

15.5.1 Two-integrator loop biquads

Out of the many second-order OA-RC sections, two-integrator loop sections are quite attractive because of their low sensitivity to passive elements. A circuit based on OA-RC Tow–Thomas biquad of Figure 8.2 is shown in Figure 15.20(a). Its analysis gives the following transfer function

$$\frac{V_{o1}}{V_{\text{in}}} = \frac{N(s)}{D(s)} = \frac{-(g_{m1}g_{m4}/C_1C_2)}{s^2 + (g_{m3}/C_1)s + (g_{m2}g_{m4}/C_1C_2)} \tag{15.24}$$

$$(V_{o2}/V_{\text{in}}) = -(g_{m1}/C_1)s/D(s) \tag{15.25}$$

The circuit provides LP and BP responses having parameters as:

$$\omega_o = \sqrt{g_{m2}g_{m4}/C_1C_2},\ Q = (1/g_{m3})\sqrt{\{(g_{m2}g_{m4})(C_1/C_2)\}} \tag{15.26}$$

$$\text{Mid-band gain of the BP section} = g_{m1}/g_{m3} \tag{15.27a}$$

$$\text{Low frequency gain of the LPF} = g_{m1}/g_{m2} \tag{15.27b}$$

Hence, frequency ω_o can be tuned either by g_{m2} and/or g_{m4} and then Q can be changed through g_{m3} without effecting ω_o. The mid-band gain of the BP, or dc gain of the LP will be the last to be controlled through g_{m1}.

Example 15.7: Design a BPF, using the two-integrator loop circuit shown in Figure 15.20(a) having a center frequency of 400 krad/s, pole-Q of 2.5 and mid-band gain of 3.0.

Solution: Assuming a suitable value of 10 nF for both the capacitors C_1 and C_2, and with $g_{m2} = g_{m4}$, equation (15.26) gives their values as:

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$$g_{m2} = g_{m4} = \left\{C_1 C_2 \omega_o^2\right\}^{0.5} = \left\{\left(10^{-8}\right)^2 \times \left(4 \times 10^5\right)^2\right\}^{0.5} = 4\,\text{mA/V} \tag{15.28a}$$

$$g_{m3} = \left(g_{m2} g_{m4}\right)^{0.5} / Q = 4 \times 10^{-3} / 2.5 = 1.6\,\text{mA/V} \tag{15.28b}$$

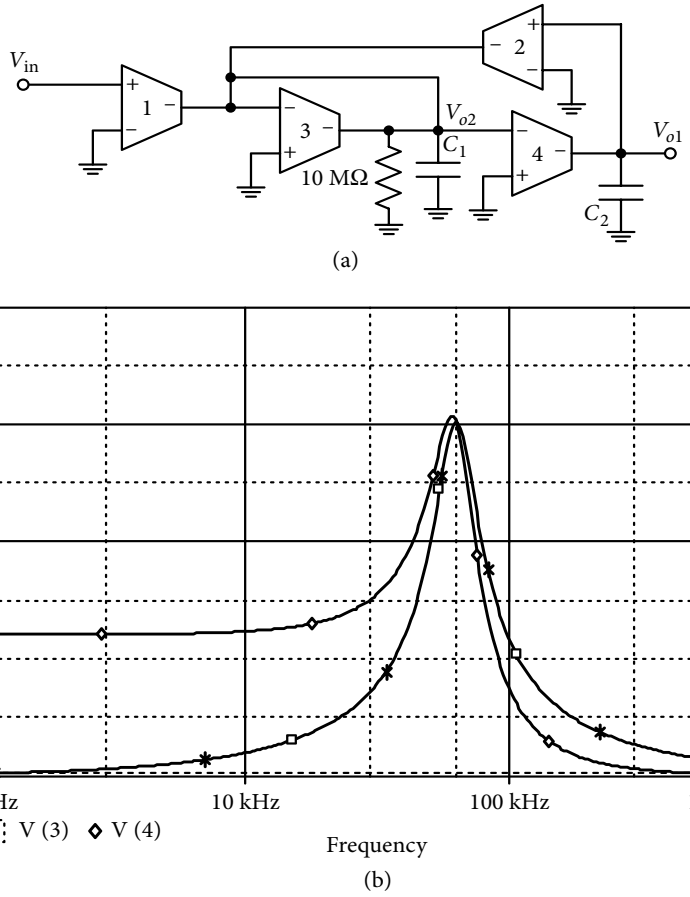

Figure 15.20 (a) Two-integrator loop-based low pass and band pass filter for Example 15.7; (b) its simulated magnitude response.

and from equation (15.27), for a mid-band gain of 3 and for the BP response

$$g_{m1} = 3 \times g_{m3} = 4.8\ \text{mA/V} \tag{15.28c}$$

The circuit shown in Figure 15.20(a) was simulated using the calculated elements and the magnitude response is shown in Figure 15.20(b). Center frequency of the BP is obtained as

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63.407 kHz (398.56 krad/s) and mid-band gain is 3.0017. With a bandwidth of 25.331 kHz, pole-Q = 2.503. Gain of the LP at low frequencies is 1.2 and a peak gain of 3.065occurs at f_{peak} of 61.108 kHz. From equation (2.46), center frequency is again obtainable as:

$$f_o = f_{peak}/\{1 - 1/2(Q_o)^2\}^{0.5} = 61.108/\{1 - 1/2 \times 6.25\}^{0.5} = 63.07 \text{ kHz}$$

KHN Biquadratic Structure: In addition to the LP and the BP responses, if it is desired to get HP and notch responses from the same circuit, OTA-C based KHN (Kerwin-Huelsman–Newcomb) biquad structures can be used which is shown in Figure 15.21(a); the circuit is derived from the one shown in Figure 8.1/8.2. Analysis shows the following relations.

$$\frac{V_o}{V_{in}} = \frac{1}{D(s)} \frac{g_{m1}\, g_{m5}\, g_{m6}\, (g_{m3} + g_{m4})}{g_{m4}(g_{m1} + g_{m2}) C_1 C_2} \tag{15.29a}$$

$$D(s) = s^2 + \left\{ \frac{g_{m2}\, g_{m5}(g_{m3} + g_{m4})}{g_{m4}(g_{m1} + g_{m2}) C_1} \right\} s + \frac{g_{m3}\, g_{m5}\, g_{m6}}{g_{m4} C_1 C_2} \tag{15.29b}$$

Output voltage V_o gives LP response as shown in equation (15.29). Its parameters will be:

$$\omega_o = \sqrt{\left(\frac{g_{m3}\, g_{m5}\, g_{m6}}{g_{m4} C_1 C_2} \right)}, \; Q = \frac{(g_{m1} + g_{m2})}{g_{m2}(g_{m3} + g_{m4})} \sqrt{\left(\frac{g_{m3}\, g_{m4}\, g_{m6} C_1}{g_{m5} C_2} \right)} \tag{15.30}$$

With the same expressions for ω_o and Q, voltages V_2, V_4 and V_5 provide a notch, HP and BP responses respectively, as shown by the following expressions.

$$V_2 = \frac{1}{D(s)} \frac{g_{m1}}{(g_{m1} + g_{m2})} \left(s^2 + \frac{g_{m3}\, g_{m5}\, g_{m6}}{g_{m4} C_1 C_2} \right) \tag{15.31}$$

$$V_4 = \frac{1}{D(s)} \frac{g_{m1}(g_{m3} + g_{m4})}{g_{m4}(g_{m1} + g_{m2})} s^2 \tag{15.32}$$

$$V_5 = \frac{1}{D(s)} \frac{g_{m1} g_{m5}(g_{m3} + g_{m4})}{g_{m4}(g_{m1} + g_{m2})} \frac{s}{C_1} \tag{15.33}$$

In equation (15.31), poles and zeroes of the filter are the same for the notch response. If a general notch and AP responses are to be obtained, the process discussed in Chapter 8 can be followed. Output voltages V_o, V_2 and V_4 are to be added employing an adder circuit like that in Figure 8.8(a).

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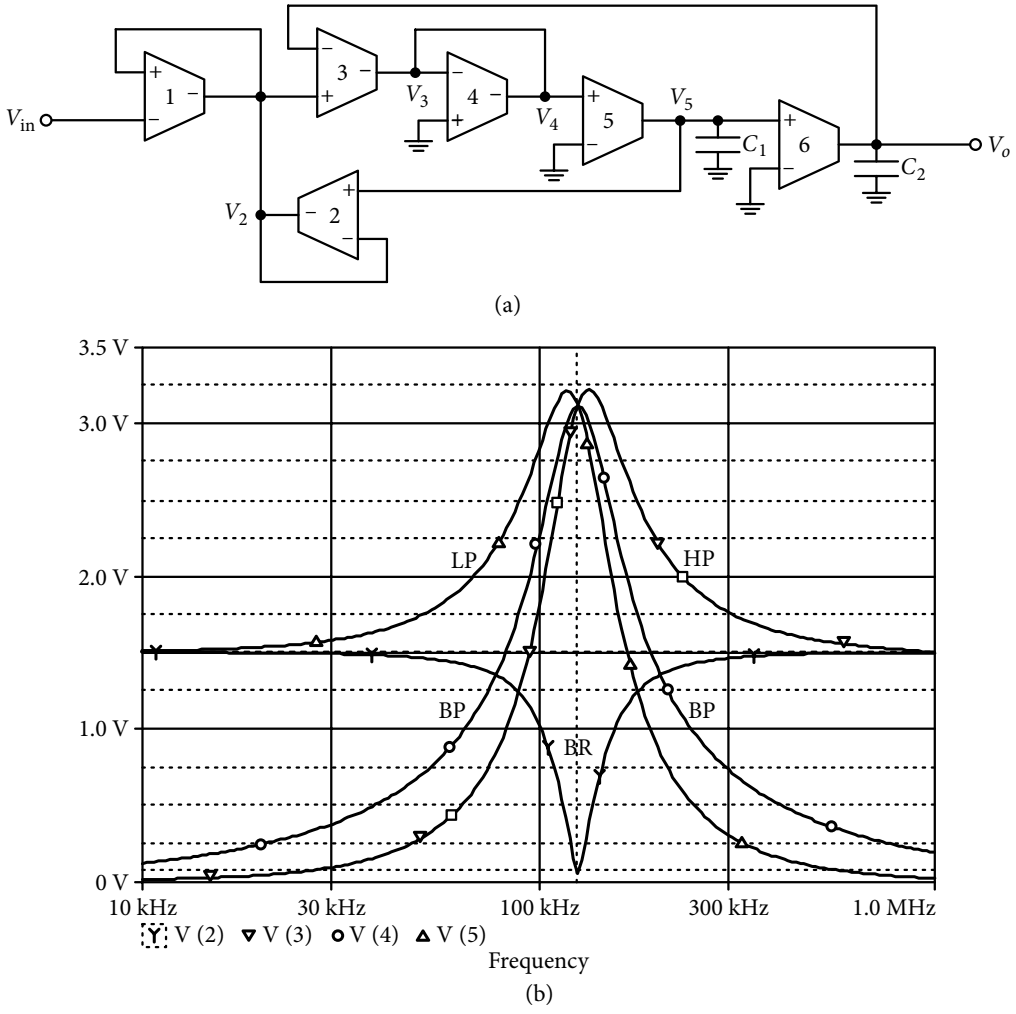

Figure 15.21 (a) KHN biquadratic configuration using six OTAs and (b) magnitude response of low pass, band pass, high pass and notch functions.

Example 15.8: Design the KHN based biquad shown in Figure 15.21(a) having the following specifications: center frequency = 800 krad/s, pole-Q = 2 and notch frequency will also be 800 krad/s.

Solution: As there are six OTAs and two capacitors, a few assumptions can be made in the beginning.

Let $g_{m3} = g_{m4} = g_{m5}$ and $C_1 = C_2 = 1$ nF, then from equation (15.30):

$$g_{m3} = \omega_o C_1 = 8 \times 10^5 \times 10^{-9} = 0.8\text{mA/V} = g_{m4} = g_{m5}$$

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To get the notch frequency same as the center frequency, from equation (15.31), g_{m6} will also be 0.8 mA/V and value of the other transconductance will be obtained as:

$$Q = (1 + g_{m1}/g_{m2}) \times 0.5 \rightarrow g_{m2} = 1\text{mA/V}, g_{m1} = 3\text{ mA/V}$$

With these elements, the circuit was simulated and the magnitude response is as shown in Figure 15.21(b); following are the observations:

The voltage V_o provides notch, which occurs at 126.005 kHz;

The voltage V_3 gives an LP response having a peak gain of 3.213 at 117.877 kHz;

The voltage V_4 gives a HP response which has a peak at 134.453 kHz with a peak gain of 3.221;

The voltage V_5 provides a BP response with a center frequency of 123.839 (778.4 krad/s) and a bandwidth of 60.289 kHz, resulting in $Q = 2.054$. Difference in the peaking of LP, HP or BP is due to $Q = 2$, in conformity with equation (2.46).

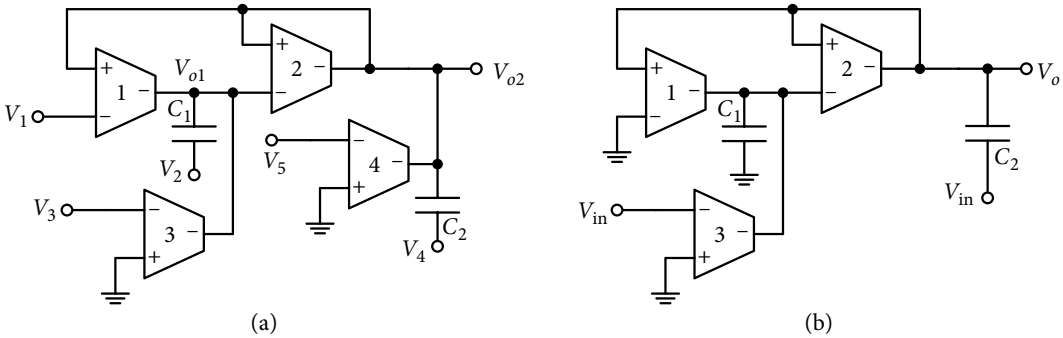
A two-integrator loop structure can be used in a different way, with more input voltages applied to some OTA terminals which were earlier grounded. For example, as shown in Figure 15.22(a), five input voltages are applied and outputs are taken as V_{o1} and V_{o2} having the following expressions.

$$V_{o1}\, D(s)\, C_1\, C_2 = C_1\, C_2\, V_2\, s^2 + (g_{m2}\, C_1\, V_2 + g_{m3}\, C_2\, V_3 + g_{m1}\, C_2\, V_4 + g_{m1}\, C_2\, V_1)s + (g_{m1}\, g_{m2}\, V_1 + g_{m2}\, g_{m3}\, V_2 + g_{m1}\, g_{m4}\, V_5) \quad (15.34a)$$

$$V_{o2}\, D(s)\, C_1\, C_2 = C_1\, C_2\, V_4\, s^2 + (g_{m4}\, C_1\, V_5 + g_{m2}\, C_2\, V_2)\text{s} + (g_{m1}\, g_{m2}\, V_1 + g_{m2}\, g_{m3}\, V_3) \quad (15.34b)$$

$$D(s) = s^2 + (g_{m2}/C_2)\text{s} + (g_{m1}\, g_{m2})/(C_1\, C_2) \quad (15.34c)$$

It is obvious that a suitable choice of input voltages and transconductance will provide all general type of transfer functions.



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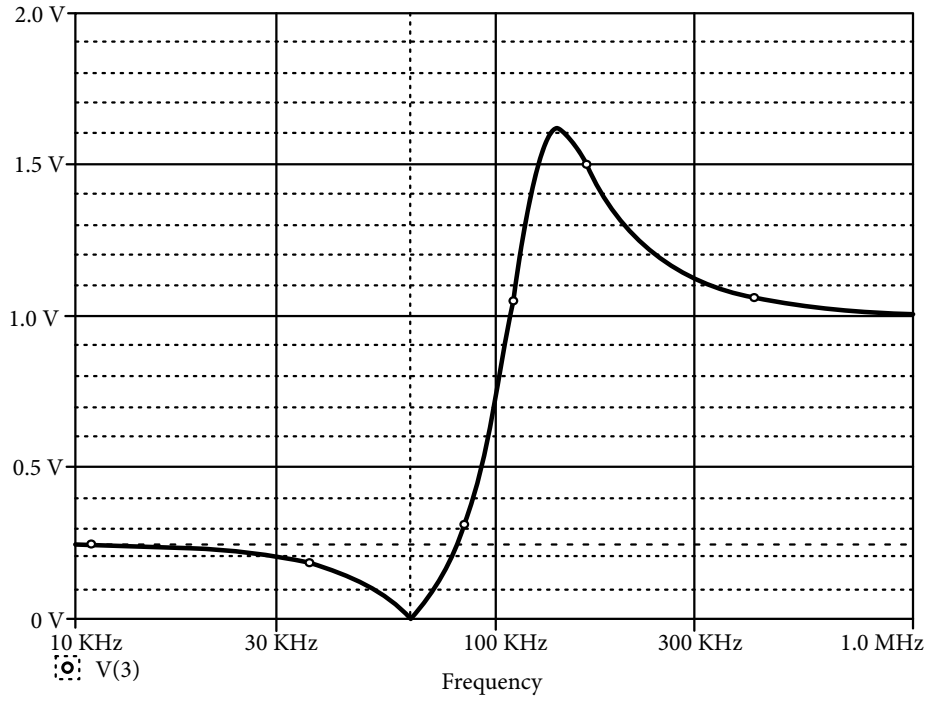

Figure 15.22 (a) Two-integrator loop-based biquad with multiple inputs, (b) modified form to get a high pass notch response. (c) A high pass notch from a general two-integrators based biquadratic section with three OTAs for Example 15.9.

Example 15.9: Obtain an HP notch at 400 krad/s using the circuit shown in Figure 15.22(a) with pole frequency at 800 krad/s and pole-Q = 2.

Solution: To get a HP notch, from equation (15.34b), $V_4 = V_3$, $V_2 = V_5 = 0$ and V_1 can also be zero. For $g_{m1} = g_{m2}$ and selecting $C_1 \times C_2 = 4(\text{nF})^2$. It gives:

$$g_{m1} = 8 \times 10^5 \times 2 \times 10^{-9} = 1.6 \text{ m A/V} = g_{m2} \tag{15.35 a}$$

Equation (15.34c) is used to find values of capacitors C_1 and C_2 with $Q = 2$:

$$Q = \left(\frac{g_{m1}C_2}{g_{m2}C_1}\right)^{0.5} = 2 \rightarrow C_2 = 4C_1 \text{ or for } C_1 = 1 \text{ nF}, C_2 = 4 \text{ nF} \tag{15.35b}$$

Combining equations (15.34b) and (15.34c), for $\omega_z = \omega_o/2$, $g_{m3} = g_{m2}/4 = 0.4$ m A/V and V_3 as input, substitution of these element values and input voltages in the circuit shown in Figure 15.22(a) modifies it to Figure 15.22(b), which is simulated using PSpice. The simulated

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magnitude response in Figure 15.22(c) shows notch frequency at 63.61 kHz (399.83 krad/s), gain at low frequencies of 0.25 and gain at high frequencies reaching near unity.

15.5.2 OTA-C biquads derived from active RC circuits

Resistors can directly be replaced in OA-RC circuits using the circuits shown in Figure 15.2 and 15.3 for grounded and floating resistor, respectively, resulting in mixed OA-OTA-C circuits. In the case of floating resistance, transconductance g_{m1} and g_{m2} needs to be matched; the circuit shown in Figure 15.16(a) can also be used for floating resistance saving one OTA. Fortunately, many a times, the RC combination of integration can be replaced by the simple OTA-C integrator shown in Figure 15.18(a) resulting in an OTA-C circuit.

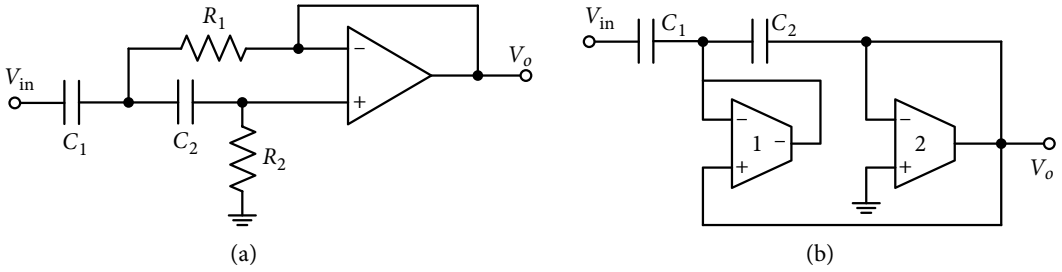

Figure 15.23 (a) Sallen and Key high pass filter section, (b) its OTA version.

Sometimes, the action of the OA may be easily substituted by a circuit using OTA; though it may not be practical economically in some cases, which makes it necessary to use OAs also in OTA-C circuits. Figures 15.23(a)–(b) and Figures 15.24(a)–(b) illustrate the point. OA in the HP Sallen–Key circuit and resistor R_1 in Figure 15.23(a) can be combined and replaced by OTA1; the resistance R_2 is realized using OTA2, resulting in all OTA HP filters, whereas in the LP case, only resistor R_1 is simulated; OA replacement would involve more components.

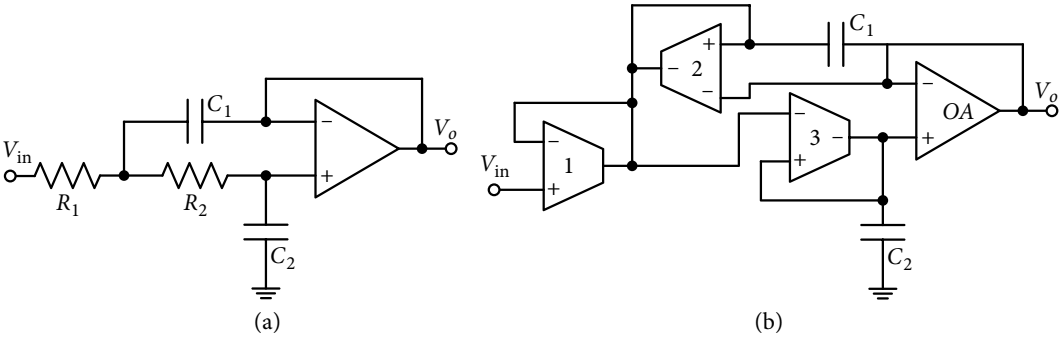

Figure 15.24 (a) OA-RC and (b) OTA with OA version of the Sallen and Key low pass filter.

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15.6 OTA-C Filters Derived from LC ladders

Lossless doubly terminated ladders have been extensively studied and used because of their low sensitivities in passive as well as in active form. OTA-C filters based on these ladder structures also enjoy the same advantages and almost the same techniques are applied as in the OA-RC case. Hence, filter realization approaches making use of ladder structures will be discussed in this section.

15.6.1 Element substitution scheme

In a doubly terminated LC ladder, it is the inductance in the grounded and floating form which is replaced using OAs and R C elements. In the OTA-C filter realizations, in addition to the inductors, resistors are also to be simulated. It is also preferable to replace even floating capacitors by circuits using only grounded capacitors as will be described now.

Gyrators were found to be very successful in impedance conversion and hence, extensively used for inductance simulation. They essentially act as an interconnection of an inverting and a non-inverting voltage amplifier terminated in an impedance. The same idea is used here and it is found out that in the OTA-C case, it is much simpler compared to the OA-RC case, as shown in Figure 15.25(a), for which

$$I_{o1} = I_2 = g_{m1}\, V_1,\ I_{o2} = I_1 = g_{m2}\, V_2, \text{ and } V_2 = ZI_2 \tag{15.36a}$$

$$\text{It gives } V_1/I_1 = Z_{\text{in}} = 1/\{g_{m1}\, g_{m2}\, (Z)\} \tag{15.36b}$$

If $Z(s) = 1/sC$, the input behaves like an inductor having its expression as: $L = C/(g_{m1}g_{m2})$. For OTAs considered ideal, gyrator simulates the pure inductor. However, as simulation of inductors finds wide usage, effect of the non-ideality of the OTAs needs consideration. Figure 15.25(b) shows the small signal model of the gyrator with Z being an external capacitor. Analysis shows the input admittance as:

$$Y_{\text{in}}(s) = g_o + (C_i + C_o)s + 1/\left\{\left(\frac{C + C_i + C_o}{g_{m1} + g_{m2}}\right)s + \left(\frac{g_o}{g_{m1}g_{m2}}\right)\right\} \tag{15.37}$$

The circuit represented by equation (15.37) is shown in Figure 15.25(c), with parasitic resistances r_o and r_s, and capacitance C_p. The realized inductance value and effective increased terminating capacitance, respectively, are:

$$L_{\text{eff}} = (C_i + C_o + C)/g_{m1}g_{m2} \tag{15.38a}$$

$$C_{\text{eff}} = C_i + C_o + C \tag{15.38b}$$

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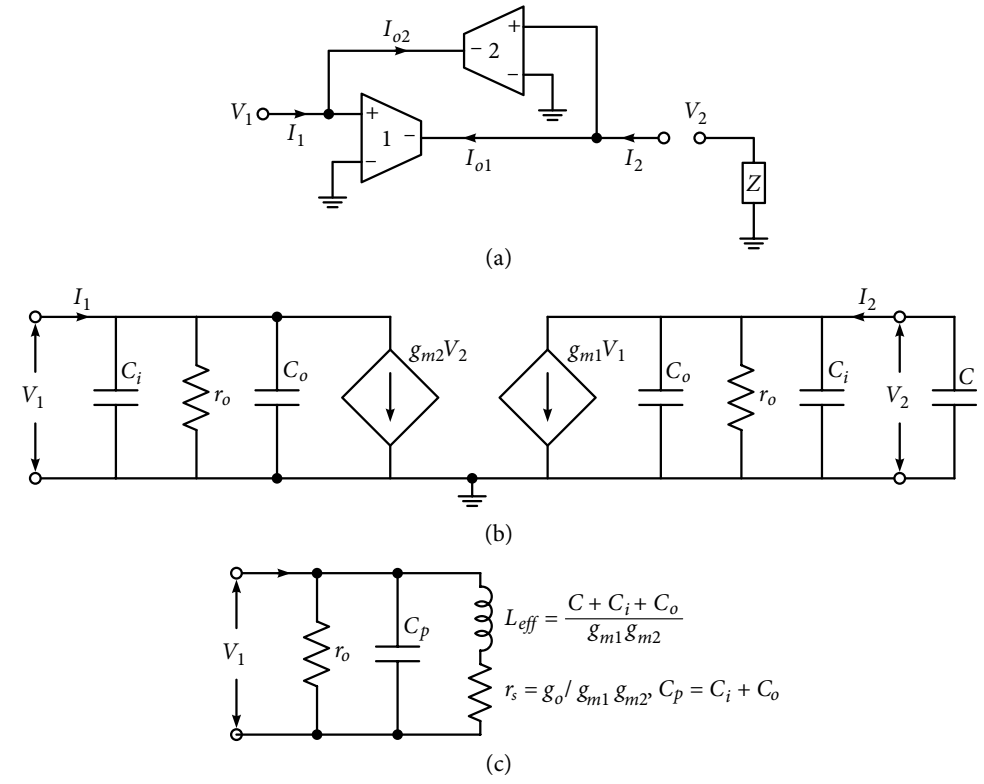

Figure 15.25 (a) OTA-based gyrator terminating in impedance Z, (b) small-signal equivalent circuit of (a) showing parameters of OTA, and (c) the resulting non-ideal grounded inductor.

Differential GI (grounded inductors) can also be realized by employing the procedure discussed in Section 15.4. Figure 15.26(a) shows a mirror image of Figure 15.25(a), and as they are combined together, it results in the circuit shown in Figure 15.26(b).

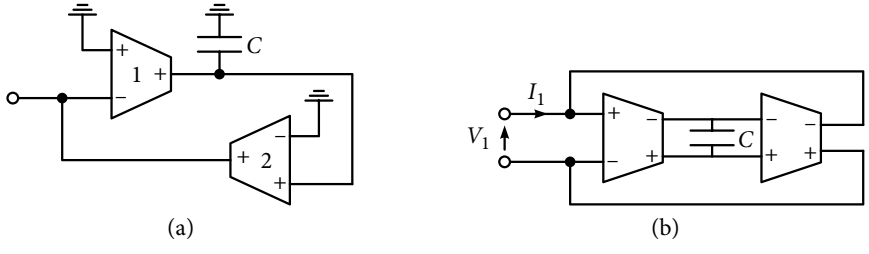

Figure 15.26 (a) Mirror image of the circuit in Figure 15.25(a) with Z as capacitor, (b) differential grounded inductance simulator.

Example 15.10: Verify that the circuit shown in Figure 15.25 simulates a GI by using it in a BPF with center frequency of 20 krad/s and $Q = 5$.

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Solution: Figure 15.27(a) shows an RLC second-order BPF for which parameters are derived as:

$$\omega_o^2 = 1/LC_1,\ \ Q = \tfrac{1}{2}R\left(C_1/L\right)^{0.5},\ \ \text{mid-band gain} = 0.5 \text{ for } R_L = R_{\text{in}} = R$$

For the given specifications, if C_1 is selected as 4 nF, the required value of inductance will be 1.0 mH. The inductance is realized using the circuit shown in Figure 15.25(a), with $g_{m1} = g_{m2}$ = 3 mA/V and the terminating capacitor C = 9 nF. For Q = 5, needed R = 5 kΩ.

Figure 15.27(b) shows the simulated magnitude response of the BPF. Center frequency is 79.49 kHz (499.6 krad/s), bandwidth is 15.88 kHz, giving Q = 5.02 and the mid-band gain is 0.498, verifying the simulation of inductance.

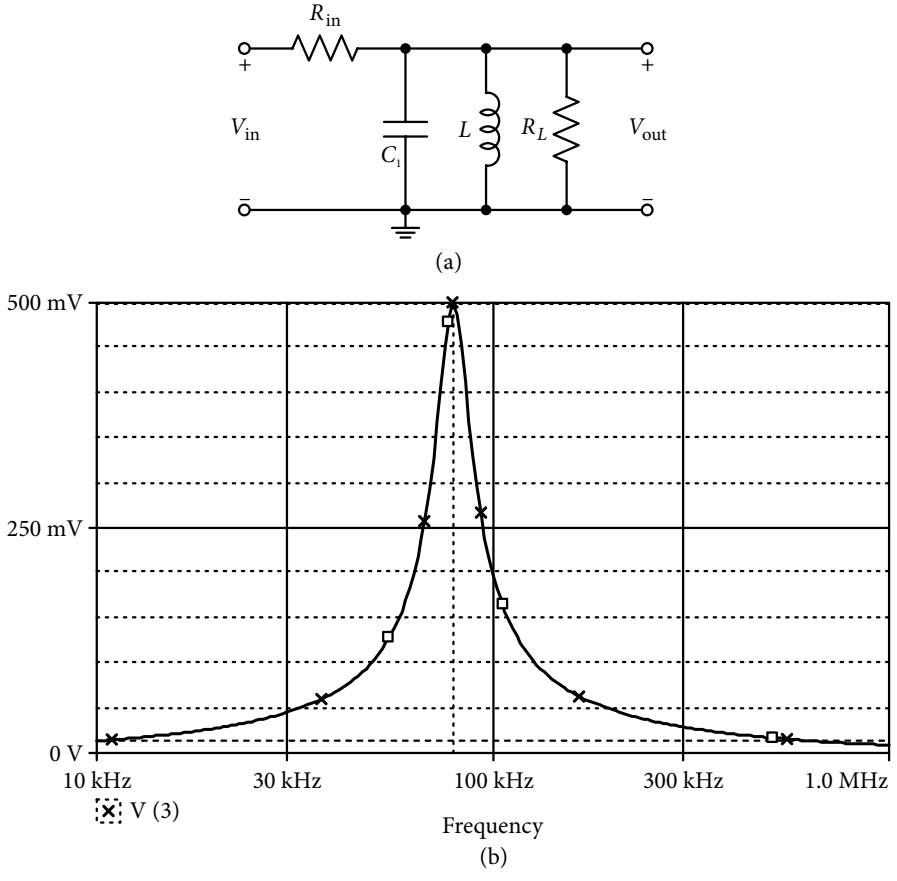

Figure 15.27 (a) Passive RLC band pass filter section for Example 15.10, (b) response of the band pass filter using the OTA simulated grounded inductor shown in Figure 15.25(a).

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15.7 Single-ended and Differential Floating Inductance

Back-to-back gyrators terminating in a capacitor realize a FI (floating inductance) in the OTA-C case as well, as it is applicable in the OA-RC case. Figure 15.28(a) shows such a scheme and Figure 15.28(b) shows its simulated form. Analysis gives:

$$I_1 = I_{o2} = g_{m2}\left(-V'\right),\ I_2 = I'_{o2} = g'_{m2}V' \tag{15.39a}$$

$$I_{o1} = g_{m1}V_1,\ I'_{o1} = g'_{m1}(-V_2) \text{ and } V' = -(I_{o1} + I'_{o1})/sC \tag{15.39b}$$

For $g'_{m1} = g_{m1}$ and $g'_{m2} = g_{m2}$, equations (15.39a) and (15.39b) result in the following matrix:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \frac{g_{m1}g_{m2}}{sC}\begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix}\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{15.40}$$

Matrix equation (15.40) represents the FI shown in Figure 15.28(b) with the expression of inductance as:

$$L = C/g_{m1}g_{m2} \tag{15.41}$$

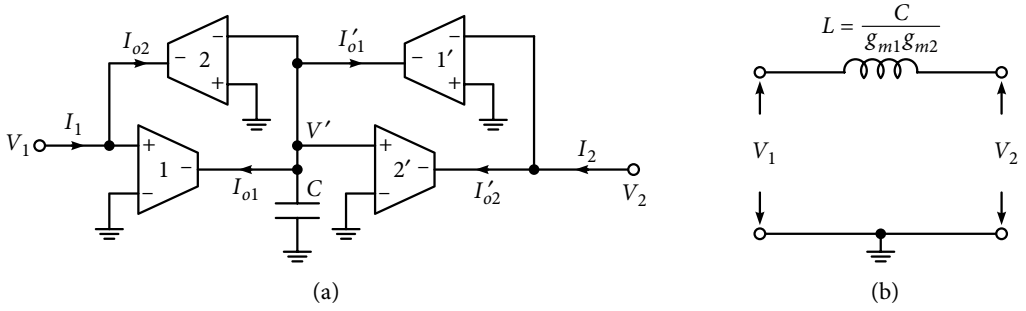

Figure 15.28 (a) Realization of floating inductance using back-to-back gyrators, (b) its equivalent circuit.

However, with non-idealities of the OTAs taken into consideration, the effective value of the simulated inductance will be the same as given by equation (15.18) for the GI, and the circuit representation will be as in Figure 15.25(c), but with both terminals ungrounded.

Example 15.11: Utilize the FI simulator shown in Figure 14.28(a) in a notch filter of Figure 15.29(a) having a notch frequency of 50 kHz.

Solution: Expression of the notch frequency will be $1/(LC)^{0.5}$. Hence, for the selected value of the capacitance C = 10 nF, required inductance is 1.0 mH. For the realization of FI, all the

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four transconductance are taken as 1 mA/V, which requires its terminating capacitor as 1.0 nF. Load resistance R decides the pole-Q. The simulated response shown in Figure 15.29(b) has a notch at 50.03 kHz.

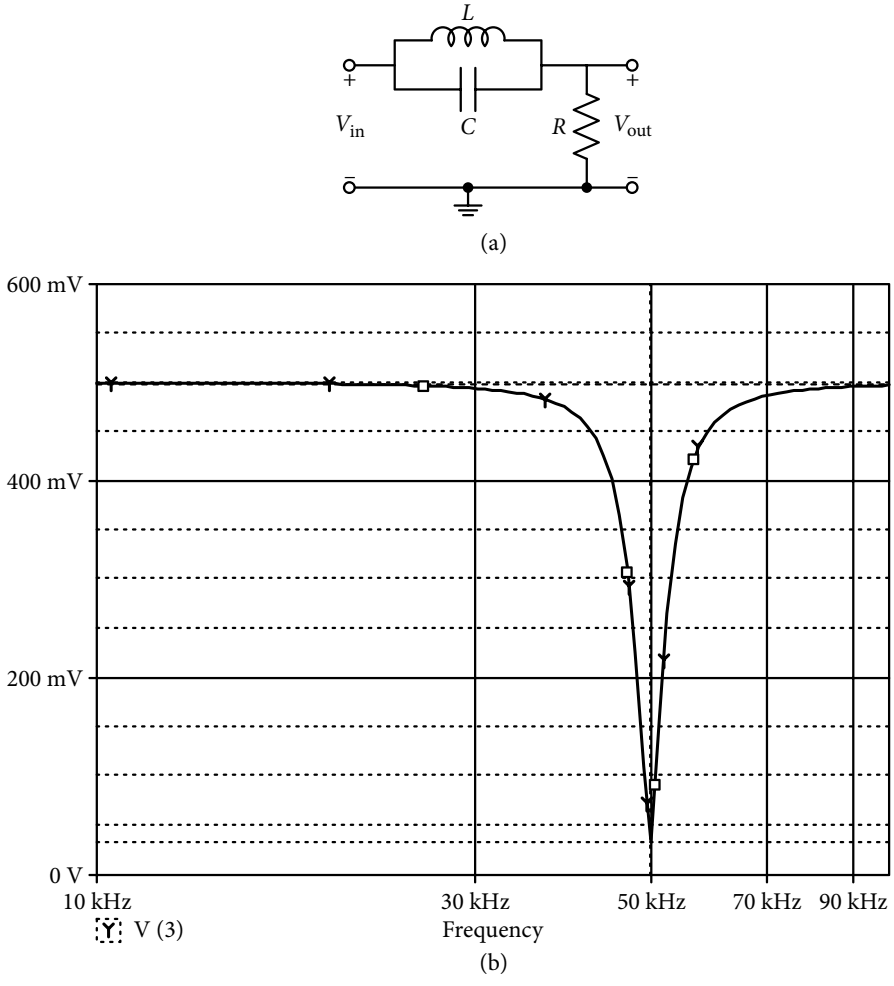

Figure 15.29 (a) Passive notch circuit for testing OTA-C floating inductor in part (a) of Figure 15.28(a), (b) magnitude response of the OTA-C notch filter.

An alternative FI using only three OTAs and a grounded capacitor is shown in Figure 15.30(a). It is obtained by combining OTA1 and OTA1′ as OTA2. With OTAs considered ideal, the simulated inductance is the same as in equation (15.41) with $g_{m1} = g_{m3}$. Students can find the simulated equivalent circuit when OTAs are considered non-ideal.

Using the mirror image of Figure 15.28(a), and combining it with its original gives a floating differential inductor using four differential output OTAs as shown in Figure 15.30(b).

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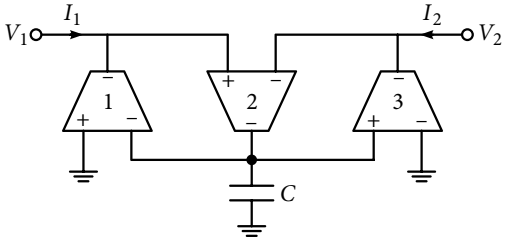
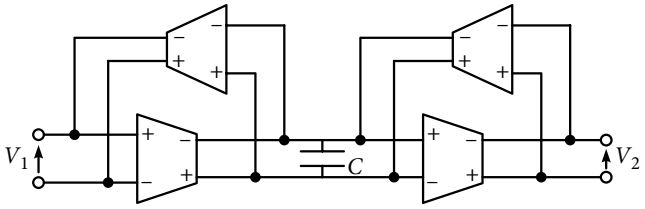
15.7.1 Floating capacitor simulation

From the circuit fabrication point of view, it is always better to use grounded capacitors, as parasitic capacitances are considerably reduced. That is why it is desirable to simulate the floating capacitor in terms of the grounded capacitor, wherever practically feasible. Tolerance is further reduced if the filter parameters are obtained in terms of the ratio of the grounded capacitors. A capacitor is simulated if the gyrator in Figure 15.25(a) terminates in a GI (or terminates in Figure 15.30(a) for FI). Using three OTA FIs of Figure 15.30(a), which terminates in a GI (using two OTAs and a grounded capacitor), a floating capacitor simulator is obtained as shown in Figure 15.31(a). With $g_{m1} = g_{m3}$, expression of the simulated capacitance is given as:

$$C = g_{m1}g_{m2}C'/g_{m4}g_{m5} \tag{15.42}$$



(a)



(b)

Figure 15.30 (a) Alternate floating inductance simulator using three OTAs. (b) Differential floating inductor from Figure 15.28(a).

It is obvious that the circuit not only simulates a floating capacitor, it also works as a capacitance multiplier with proper selection of transconductance.

Example 15.12: Figure 15.31(b) shows a passive BPF. Design and test the same using the OTA-C floating capacitor of Figure 15.31(a) for the filter to have center frequency of 500 krad/s and $Q = 10$ with a mid-band gain of 10.

Solution: For the circuit in Figure 15.31(b), expressions for center frequency and Q are:

$$\omega_o^2 = 1/LC, \text{ and } Q = (L/C)^{0.5}/R$$

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Selecting C = 5 nF, the required inductance shall be 0.8 H and R = 40 kΩ. With $g_{m1} = g_{m2} = g_{m3} = g_{m4} = g_{m5}$ = 2 mA/V grounded capacitance C'shall be 5 nF. The circuit was simulated and the response is shown in Figure 15.31(c). Simulated center frequency is 79. 49 kHz (499.65 krad/s), mid-band gain is 9.99 and with a bandwidth of 7.9489 k Hz, Q becomes 10; verifying the performance of the floating capacitor.

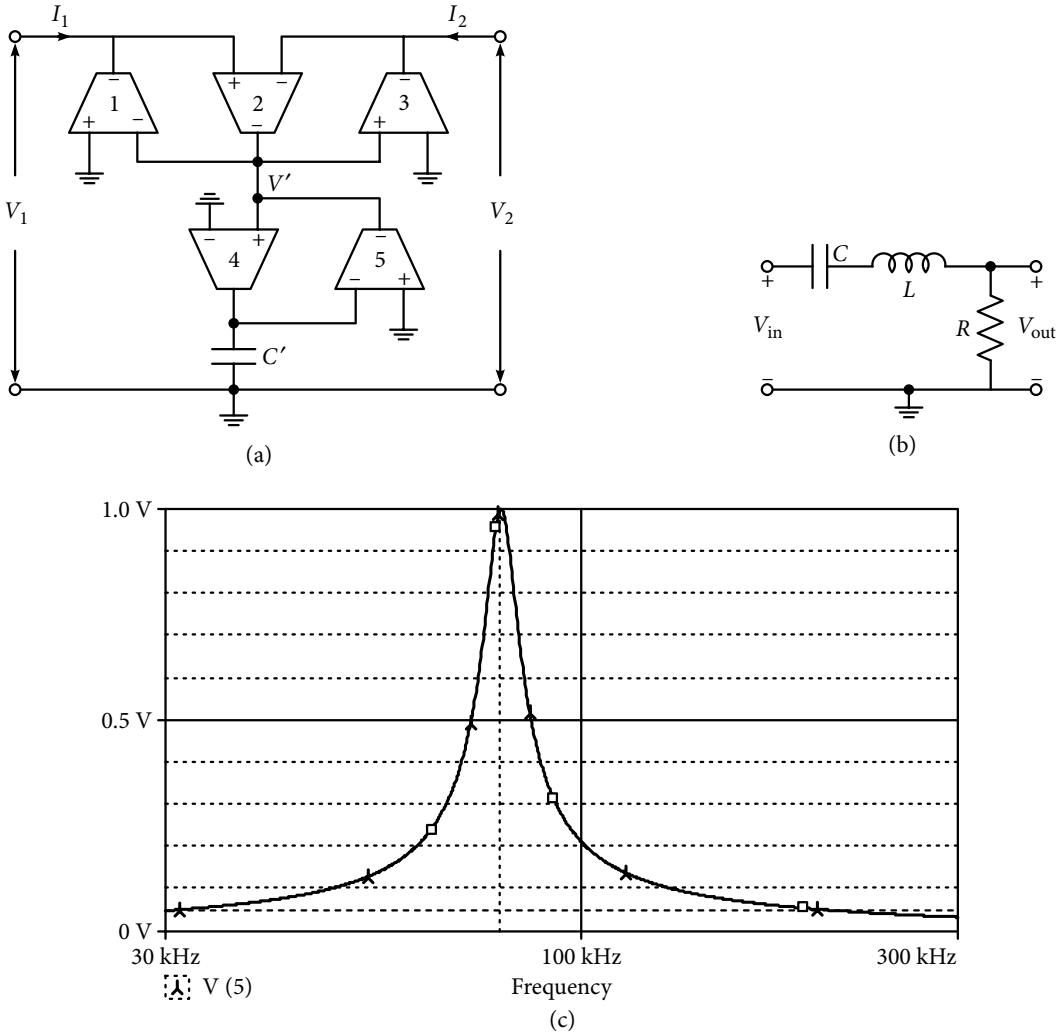

Figure 15.31 (a) Floating capacitor simulation using grounded capacitor (b) RLC band pass filter circuit and (c) simulation of the second-order band pass filter shown in part (b) while using the floating capacitor of part (a).

Example 15.13: Obtain a fifth-order Chebyshev filter employing the element substitution approach in the OTA-C form. The filter is to have a corner frequency of 800 krad/s and ripple width of 0.5 dB.

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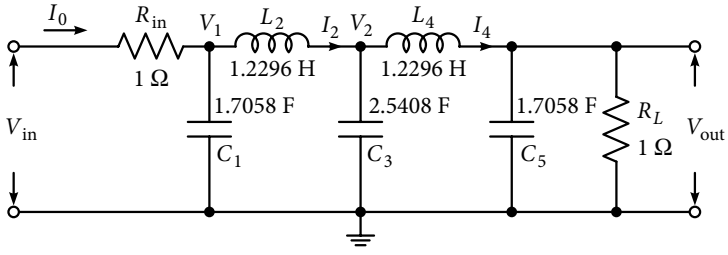
Solution: Figure 15.32(a) shows a fifth-order LP RLC ladder with normalized element values. The inductance simulator shown in Figure 15.30(a), and resistance simulators of Figures 15.2 and 15.3 can be used to obtain the OTA-C ladder shown in Figure 15.32(b). However, the circuit has been slightly modified by combining the adjacent OTAs 4 and 5, now shown as OTA45 in Figure 15.32(b). Note that the parasitic capacitances of the OTAs can be absorbed in the GCs. First, the elements are de-normalized using a frequency scaling of 8×10^5 rad/s and impedance scaling factor of 1.25 kΩ; the values become:

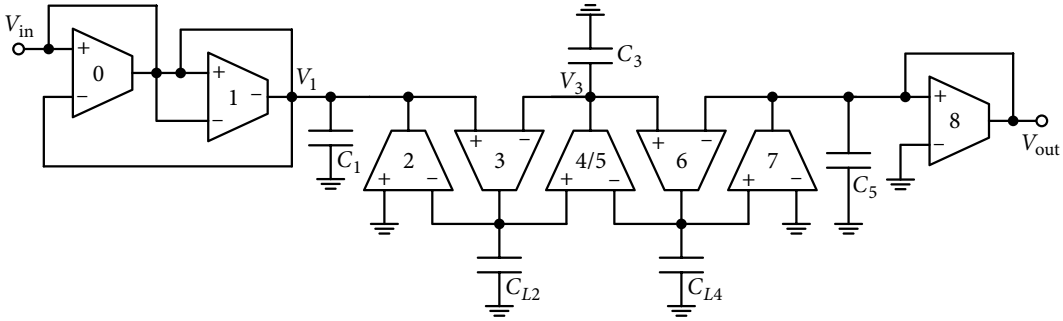
$$R_{in} = R_L = 1.25\ \text{k}\Omega,\ C_1 = C_5 = 1.7058\ \text{nF},\ C_3 = 2.5408\ \text{nF},\ L_2 = L_4 = 1.92125\ \text{mH}$$

For the realization of resistances R_{in} and R_L, use of equations (15.1) and (15.3) gives $g_{m0} = g_{m1} = g_{m8} = 1/1250 = 0.8$ mA/V. For simulating FIs, assuming $g_{m2} = g_{m3} = g_{m4/5} = g_{m6} = g_{m7} = 1.0$ mA/V, use of equation (15.41) gives $C_{L2} = C_{L4} = 1.92125$ nF. Using these element values in Figure 15.32(b), the circuit is simulated; the high value resistances (10 mega-ohm) are connected at some nodes where the path for bias current was needed.

Figure 15.32(c) shows the magnitude response having pass band edge frequency of 127.345 kHz (800.45 krad/s) and ripple width of 0.5058 dB and gain of 0.4998 at dc.



(a)



(b)

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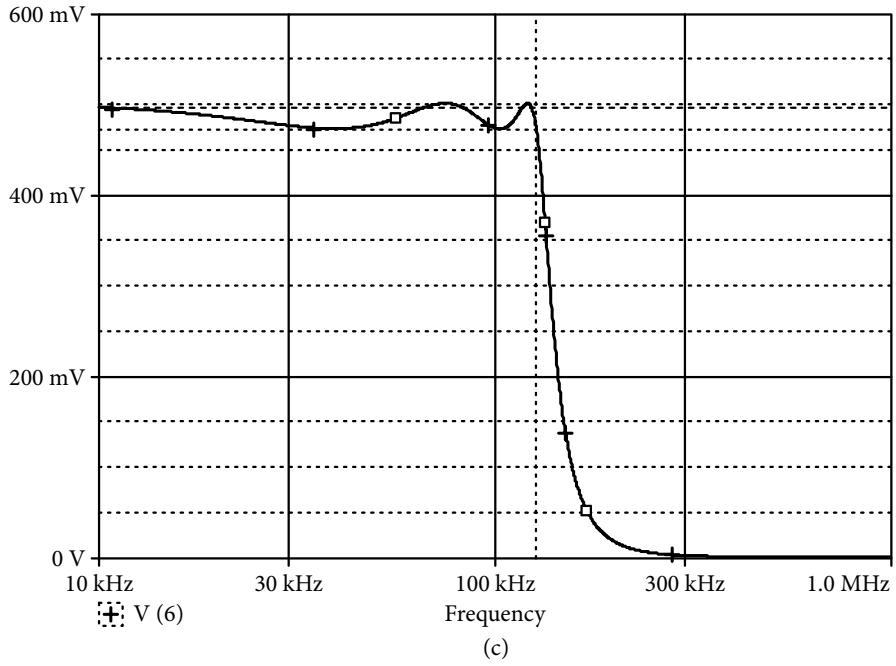

Figure 15.32 (a) Fifth-order LC ladder structure, (b) floating inductance and terminating resistances simulated OTA-C circuit and (c) simulated magnitude response of the fifth-order Chebyshev filter in (a)-example 15.13.

15.7.2 Anti-aliasing filter for an ECG detection device

A brief discussion on an analog front-end system for portable ECG (electrocardiograph) detection devices was included in Section 11.5.1 [15.1]. One of its important constituents is an anti-aliasing filter. Based on the system requirements, an OTA based filter is preferred at low frequency operation as transistors inside the OTA can be operated in the sub-threshold region to save power. To attenuate out of band interference before the ADC, a fifth-order ladder type Butterworth filter with cut-off frequency of 250 Hz was needed. As the aim was to show the utilization of OTAs in anti-aliasing, the present design of the filter is different from the filter mentioned in the reference on two counts. OTAs having transconductance of the order of mA/V are used instead of operating in the sub-threshold region, and element (floating inductance) substitution approach is used instead of operational simulation.

The structure of a fifth-order Butterworth passive filter is already shown in Figure 15.32(a). It can be used with different values of elements corresponding to the specification for this application. Normalized element values as obtained from Table 3.3 are:

$$L_2 = L_4 = 1.618 \text{ H}, C_1 = C_5 = 0.618 \text{ F}, C_3 = 2.0 \text{ F and } R_{in} = R_L = 1\Omega \tag{15.43}$$

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Applying frequency de-normalization by 250 Hz and using an impedance scaling factor of 10^3, element values modify as:

$$L_2 = L_4 = 1.029 \text{ H}, C_1 = C_5 = 0.3932 \text{ μF}, C_3 = 1.272 \text{ μF and } R_{in} = R_L = 1 \text{ kΩ} \quad (15.44)$$

The inductance simulator of Figure 15.30(a), and resistance simulators of Figure 15.2 and 15.3 are used to obtain the OTA-C ladder as shown in Figure 15.32(b).

For the realization of resistances R_{in} and R_L, use of equations (15.1) and (15.3) gives $g_{m0} = g_{m1} = g_{m8} = 1/(1000 = 1.0 \text{ mA/V})$. For simulating FIs, assuming $g_{m2} = g_{m3} = g_{m4/5} = g_{m6} = g_{m7} = 1.0$ mA/V, use of equation (15.41) gives $C_{L2} = C_{L4} = 0.9718$ nF. Using these element values in Figure 15.32(b), the circuit is simulated, while connecting high value resistances (10 mega-ohm) at some nodes where path for bias current was needed.

Figure 15.33 shows the magnitude response having a pass band edge frequency of 258 Hz, and its attenuation of 46.5 dBs occurs at three times its cut-off frequency; this satisfies the requirements.

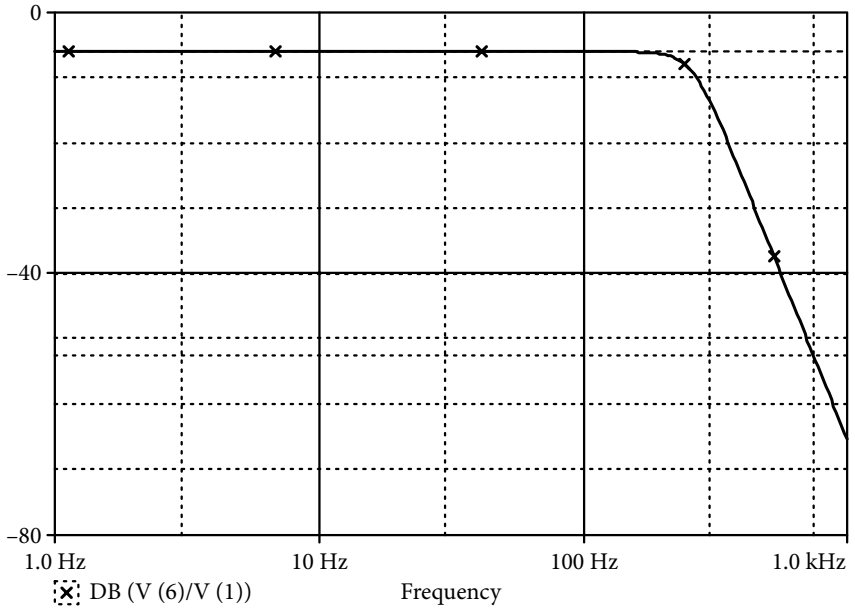

Figure 15.33 Response of a fifth-order anti-aliasing filter.

15.8 Operational Simulation Process

The process follows exactly the same steps as in OA based active RC circuits. Only inverting and non-inverting integrators are required for the RLC ladder. Lossless and lossy integrators

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of Figures 15.4(a) and (b), respectively are employed, while keeping in mind that alternate inverting/non-inverting modes are used. The RLC fifth-order low pass section of Figure 15.32(a) can be described by the following equations.

$$V_1 = \frac{I_o - I_2}{sC_1 + G_{\text{in}}},\ I_2 = \frac{V_1 - V_3}{sL_2},\ V_3 = \frac{I_2 - I_4}{sC_3} \tag{15.45a}$$

$$I_4 = \frac{V_3 - V_{\text{out}}}{sL_4},\ V_{\text{out}} = \frac{I_4}{sC_5 + G_L} \tag{15.45b}$$

Input series resistance R_i has been replaced by its equivalent shunt resistance in parallel with capacitor C_1 as depicted in equation (15.45a). All currents are to be converted as voltages through resistance scaling; hence, the following relations are obtained:

$$V_1 = \frac{RI_o - RI_2}{sRC_1 + RG_{\text{in}}} \rightarrow v_1 = \frac{v_{I\text{in}} - v_{I2}}{sc_1 + g_{\text{in}}} \tag{15.46a}$$

Here, subscript I with v indicates a current signal converted to voltage through scaling. The remaining expressions are:

$$RI_2 = \frac{V_1 - V_3}{sL_2 / R} \rightarrow v_{I2} = \frac{v_1 - v_3}{sl_2} \tag{15.46b}$$

$$V_3 = \frac{RI_2 - RI_4}{sRC_3} \rightarrow v_3 = \frac{v_{I2} - v_{I4}}{sc_3} \tag{15.46c}$$

$$RI_4 = \frac{V_3 - V_{\text{out}}}{sL_4 / R} \rightarrow v_{I4} = \frac{v_3 - v_{\text{out}}}{sl_4} \tag{15.46d}$$

$$V_{\text{out}} = \frac{RI_4}{sRC_5 + RG_L} \rightarrow v_{\text{out}} = \frac{v_{I4}}{sc_5 + g_L} \tag{15.46e}$$

Using the lossless and lossy integrators of Figure 15.4, we obtain the OTA-C version in Figure 15.34(a). For $g_{m2} = g_{m1}$, $g_{m5} = g_{m4}$, $g_{m7} = g_{m6}$ and $g_{m9} = g_{m8}$, the current–voltage relations corresponding to equation (15.46) are:

$$v_1 = \frac{g_{m1}}{sc_1 + g_{m3}}\left(v_{in} - v_{I2}\right),\ v_{I2} = \frac{g_{m4}}{sc_{L2}}\left(v_1 - v_3\right) \tag{15.47a, b}$$

$$v_3 = \frac{g_{m6}}{sc_3}\left(v_{I2} - v_{I4}\right),\ v_{I4} = \frac{g_{m8}}{sc_{L4}}\left(v_3 - v_5\right),\ v_{\text{out}} = \frac{g_{m10}}{sc_5 + g_{m11}} v_{I4} \tag{15.47c, d, e}$$

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Equation (15.47) can be used as a design equation for finding the values of the capacitors and trans-conductance.

In case a floating capacitor is also present in the series branch in parallel with inductor L_2 or L_4, it needs no special consideration. The capacitor is to be placed between the same two terminals where the inductor is in the original RLC ladder, without any change. For example, if there is a capacitance C' in parallel with L_4, current through it will be $(V_3 - V_{out})sC'$. As these two node voltages V_3 and V_{out} are available in the OTA-C circuit and if C' is connected between them, it will carry the same current.

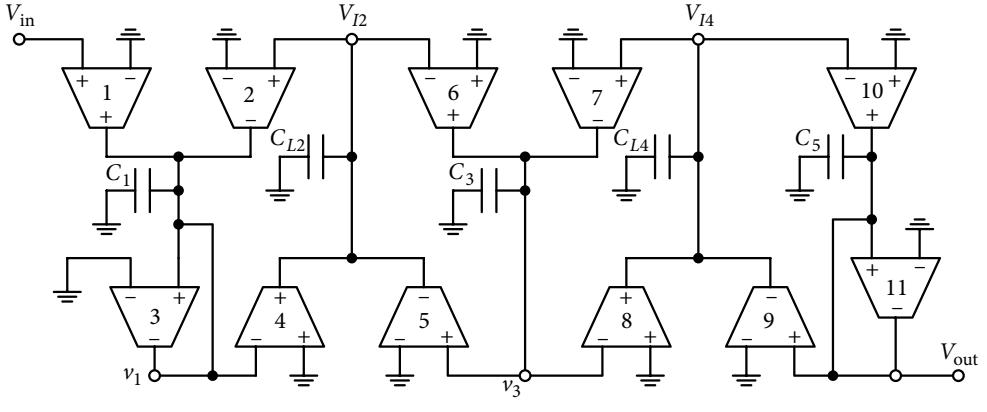
Example 15.14: Re-design the fifth-order ladder of Figure 15.32(a) using the operational simulation technique.

Solution: Figure 15.34(a) shows the operationally simulated OTA-C version of the filter ladder of Figure 15.32(a). Two non-ideal integrators simulating equations (15.46a–e) and three ideal integrators simulating equations (15.47b–d) have been joined as discussed in the text.

Application of the frequency scaling by 800 krad/s and impedance scaling of 1.25×10^3 yield the following element values for the ladder structure of Figure 15.32(a).

$$R_{in} = R_L = 1.25\ k,\ L_2 = L_4 = 1.92125 \text{ mH},\ C_1 = C_5 = 1.7058 \text{ nF and } C_3 = 2.5408 \text{ nF}$$

All integrators simulating equation (15.46) and (15.47) employ OTAs with transconductance $g_m = 1.0$ mA/V. It results in the value of capacitances $C_{L2} = C_{L4} = 1.9215$ nF. However, OTA1 and OTA11, which are simulating resistors have $g_m = 0.8$ mA/V.



(a)

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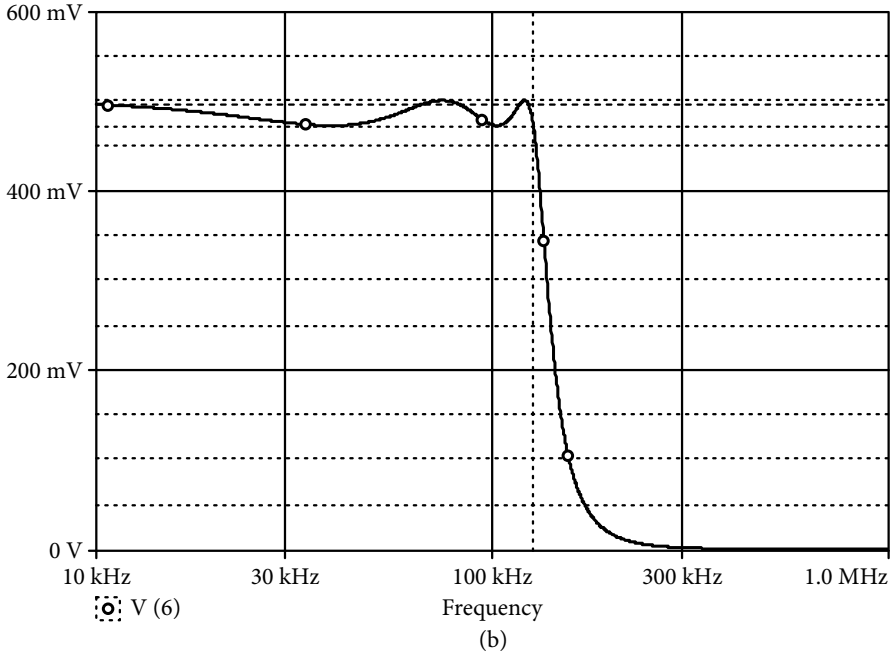

Figure 15.34 (a) Fifth-order Chebyshev filter through operational simulation technique. (b) Operationally simulated fifth-order Chebyshev filter response for Example 15.14.

The simulated response is shown in Figure 15.34(b), which is in close conformity with the design having a pass band edge frequency of 127.47 kHz (801.24 krad/s) and a ripple width of 0.495 dB.

References

[15.1] Lee, Shuenn-Yuh, Jia-Hua Hong, Jin-Ching Lee, and Qiang Fang. 2012. 'An Analog Front-End System with a Low-Power On-Chip Filter and ADC for Portable ECG Detection Devices'. *Advances in Electro-Cardiogram-Methods and Analysis*. ISBN:9789533079233.

Practice Problems

15-1 Determine the output voltage in the circuit of Figure P15.1 at 1 MHz, with resistor being 10 k Ohm and applied voltages and trans-conductance are: $V_1 = 2V, V_2 = 3V$, $g_{m1} = 0.2\frac{m\mathcal{A}}{V}$ and $g_{m2} = 0.3\frac{m\mathcal{A}}{V}$.

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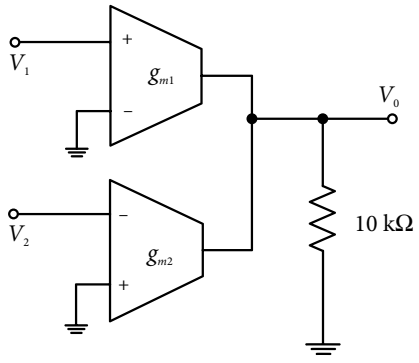

Figure P15.1

15-2 Derive the expression in equation (15.5). Design a non-inverting integrator having cut-off frequency of 10^6 rad/s and a dc gain of 2 using ideal OTAs. Find the percentage deviation in the cut-off frequency if the following values for the non-ideal model of the OTAs are used: input capacitance = 4 pF, output resistance = 1 MΩ and output capacitance = 10 pF.

15-3 Repeat Problem 15-2, for required dc gain of 20.

15-4 Determine the kind of function generated by the circuit in Figure P15.2

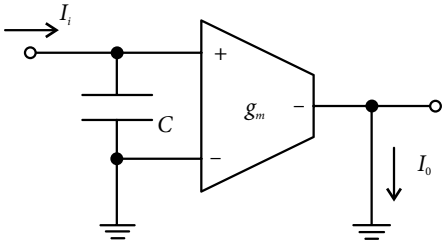

Figure P15.2

15-5 Design an inverting amplifier using OTAs for a gain of 10. Find its useful frequency range if the OTAs have parasitic input capacitance = 5 pF, output resistance = 1 MΩ and output capacitance = 8 pF.

15-6 In Figure 15.14, C = 5 nF, α = 0.2 and $g_{m1} = 2\ g_{m2}$ = 4mA/V. Sketch the voltage ratio transfer function equation (15.21) and give its dc gain and gain at high frequencies, if the OTAs are considered ideal.

15-7 Design and test an HP filter for a cut-off frequency of 300 krad/s using the circuit in Figure 15.10(b) when OTAs are considered ideal, and when OTAs have parasitic C_i = 3.6 pF, R_o = 1.5 MΩ and C_o = 5.6 pF.

15-8 Design and test an HP filter for a cut-off frequency of 400 krad/s and high frequency gain of 2, using the circuit in Figure 15.11 when OTAs are considered ideal, and when OTAs have parasitic C_i = 3.6 pF, R_o = 1.5 MΩ and C_o = 5.6 pF.

15-9 Realize an AP filter using the circuit of Figure 15.13(a), such that it has a phase shift of 90° at 500 krad/s. OTAs have the following non-idealities: C_i = 4 pF, R_o = 2 MΩ and C_o = 6 pF.

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15-10 Test the circuit of Figure 15.15(c) as an AP filter such that its phase shift of 90° occurs at 100 kHz for both the outputs. How much variation takes place in magnitude when the signal frequency changes from dc to 100 kHz.

15-11 Design and test an LP filter using the differential mode inverting amplifier from Figure 15.19(b) for cut-off frequency of 120 kHz and dc gain of 2.

15-12 Design a BP filter using the two-integrator loop circuit in Figure 15.20(a) having a center frequency of 80 kHz and $Q_o = 2$ and mid-band gain of 5. What is the peak gain of the simultaneously obtained LP response and the frequency at which the peak gain occurs?

15-13 Repeat Problem 15-12 for the following specifications:

$\omega_o = 300$ krad/s, $Q = 5$ and mid-band gain = 10.

15-14 Derive the relation in equation (15.29a) and design an LP filter having the following specifications:

$\omega_o = 250$ krad/s and $Q = 1.5$

15-15 Derive the relation in equation (15.32) and design a HP filter having the following specifications:

$\omega_o = 200$ krad/s and $Q = 1.25$

15-16 Derive the relation in equation (15.33) and design a BP filter having the following specifications:

$\omega_o = 300$ krad/s, $Q = 5$ mid-band gain = 10.

15-17 Design the KHN based biquad in Figure 15.21(a) for a notch frequency of 600 krad/s and $Q = 2$.

Note: For Problems 15-18 to 15-23, use circuit in Figure 15.22(a)

15-18 Obtain the signal V_{o1} as the LP response having a cut-off frequency of 500 krad/s, $Q = 2$ and dc gain of 5. What kind of response becomes available as V_{o2}?

15-19 Obtain the signal V_{o2} as the HP response having a cut-off frequency of 500 krad/s and $Q = 2$. What kind of response becomes available as V_{o1}?

15-20 Obtain the signal V_{o2} as the BP response having center frequency of 400 krad/s, $Q = 5$ and mid-band gain of 10. What kind of response becomes available as V_{o1}?

15-21 Obtain the signal V_{o1} as the BP response having center frequency of 500 krad/s, $Q = 5$ and mid-band gain of 5. What kind of response becomes available as V_{o2}?

15-22 Obtain the signal V_{o1} as an LP notch response having center frequency of 200 krad/s, and notch frequency of 500 krad/s.

15-23 Obtain the signal V_{o1} as an HP notch response having center frequency of 400 krad/s, and notch frequency of 200 krad/s.

15-24 Use the floating inductance of Figure 15.28(a) for the normalized fifth-order LP filter of Figure 15.32(a). Design and test it for pass band edge frequency of 100 kHz with values of the elements being:

$R_1 = R_L = 1\Omega$, $C_1 = C_5 = 1.1468$ F, $C_3 = 1.975$ F and $L_2 = L_4 = 1.3712$ H.

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15-25 Obtain the expression of the floating capacitor of equation (15.42).

15-26 Design and test the notch filter of Figure 15.29(a) having a notch frequency of 60 kHz. Employ OTA based floating inductance as well as floating capacitance.

15-27 Repeat Problem 15-26 using operational simulation technique.

15-28 Design and test a fourth-order OTA based Butterworth filter having cut-off frequency of 80 kHz using operational simulation method.

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