Chapter 9

Direct Form Synthesis: Element Substitution and Operational Simulation

9.1 Introduction

In the previous chapters, we studied realization of first-order and second-order filter sections. Though these filter sections are used as such, they are also used to generate higher-order filters employing different processes including the cascade process. However, a common alternate process for realizing second- or higher-order filter section is the *direct form* of synthesis. There are two broad categories in the direct form of synthesis: (i) element substitution method and (ii) operational simulation method. Though the filter realization procedures in the aforementioned categories differ, the starting point is the same. Initially, a passive structure with element values (mostly frequency and impedance normalized) is obtained. It is then converted into its active form. Although they have the same starting point, the construction and characteristics of the active circuit obtained through the direct form and that obtained through the cascade form differ on many counts, as shall be illustrated later.

The most common passive structure that is used to realize passive filters is the doubly terminated lossless ladder. A typical lossless ladder is shown in Figure 9.1 where R_{in} and R_L are the terminating resistors and the ladder contains only lossless elements, that is, inductors and capacitors; each series and shunt branch of the ladder can be any combination of inductors/capacitors.

We will first discuss the *element substitution* type of direct form synthesis procedure, which is mainly the avoidance of the use of inductors. Therefore, simulation of inductors forms an

https://doi.org/10.1017/9781108762632.010 Published online by Cambridge University Press

important part of the chapter. Inductance simulation, configurations for inductance simulation and active filter realizations without using an inductor are discussed in Sections 9.2–9.5. Section 9.6 deals with the simulation of a floating inductance, mainly through using two circuit structures of grounded inductances. Another method in which the inductor can be eliminated from the general lossless ladder is through scaling of the structure by the complex frequency variable *s*. This method generates a new type of element called the *frequency dependent negative resistance* (FDNR). As simulation of inductors and FDNR requires impedance conversion configurations, it is important to study the basics of these concepts. The technique is included in Section 9.8.

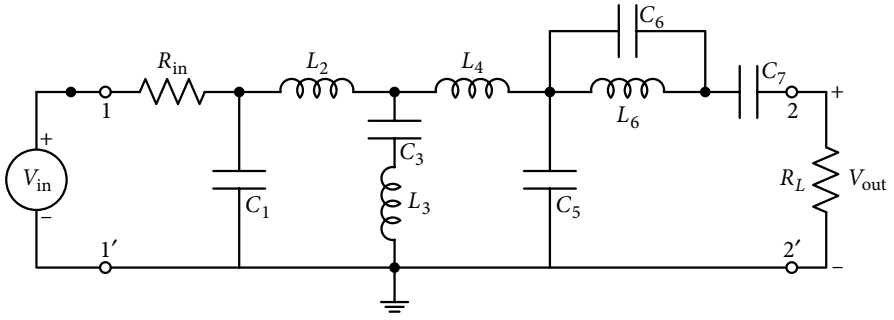


Figure 9.1 A typical doubly terminated lossless ladder structure with input resistance R_{in} and load resistance R_L.

An alternate method applied on ladders is based on the modeling of circuit equations and current–voltage relations of the circuit elements instead of direct element substitution. The electronic circuit is represented by a signal flow graph containing directional branches and nodes where branching takes place. It can also be represented in block diagram form with branches comprising blocks representing current–voltage relations of passive elements. Often, the employed blocks are integrators (or differentiators) interpreting inductors and capacitors. These blocks also incorporate summation of voltages and will be discussed in Section 9.9.

Once the principle of operational simulation is explained in detail, it is first utilized to get an LP (low pass) ladder and then for a BP (band pass) ladder structure in Sections 9.10 and 9.11, respectively. Since all networks may not be in as simple form as an LP or a BP, the scheme for realizing general ladders is studied in Section 9.12.

At first, the operational simulation method appears to be solving the problem in a roundabout manner compared to the element substitution method. In fact, the procedure is a bit lengthy, but it is observed that the method has certain advantages. In general, it employs a lesser number of active devices and deals well especially with floating inductors/FDNRs realizations as it does not require back-to-back matching circuits. As shall be shown later, a proper selection of integrators helps in considerable reduction in the non-ideal effect of OAs used, making the circuit useful in a comparatively larger frequency range.

Lossless Ladders: The lossless ladder structure is very popular among filter circuit designers because of its excellent property of very low sensitivity to component tolerances [9.1]. When

https://doi.org/10.1017/9781108762632.010 Published online by Cambridge University Press

such a ladder is converted to its active form, the property of low component tolerance sensitivity is transferred to it, which makes the structure attractive even at lower frequencies (audio or even up to a few hundred kHz; depending on the kind of active device used); whereas passive ladders continue to be used at higher frequency applications where active filtering is not suitable or where power supply is not available for active devices.

One important advantage in using lossless terminated ladders for active filters is that a large amount of literature is available in the form of filter structures, detailed description in terms of their transfer functions, pole locations and normalized element values from low to high-order filters [1.2]. Such available literature is of great help for active filter design. One of the main reasons for converting LC lossless ladders to their active forms is, as mentioned earlier, the non-availability of good quality inductors in most of the operating frequency range.

9.2 Gyrator and Inductance Simulation

As seen in Figure 9.1, inductances used in the ladder can have one terminal connected to the ground, which are known as grounded inductors (GIs), or none of their terminals connected to the ground, which are known as floating inductors (FIs). First, let us look at the simulation of a GI as shown in Figure 9.2(a). The method will be later extended to realize an FI as shown in Figure 9.2(b). For simulating a GI, it is required to find a circuit which contains only resistors, capacitors and some active device(s); moreover, its driving point impedance should appear as that of an inductance. Such a configuration is known as *impedance converter* or *gyrator*. Symbol of a simplified gyrator is shown within the dotted box in Figure 9.3, which is defined by the following equation [9.2].

$$I_1 = -(1/r)V_2 \text{ and } I_2 = -(1/r)V_1 \tag{9.1}$$

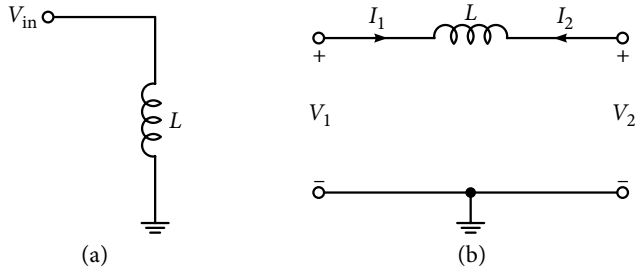


Figure 9.2 (a) Grounded inductance, and (b) a floating inductor representation.

The important parameter of a gyrator r is known as a *gyrator constant*; the constant has the units of ohm. From equation (9.1), the input impedance of the gyrator will be:

$$Z_{in}(s) = (V_1/I_1) = r^2/(1/sC) = sr^2C \tag{9.2}$$

https://doi.org/10.1017/9781108762632.010 Published online by Cambridge University Press

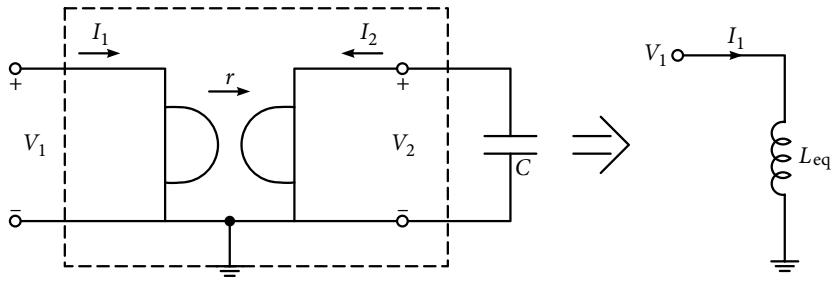


Figure 9.3 Grounded inductance simulation using a gyrator terminated in a grounded capacitor.

Therefore, a gyrator terminated in a capacitor C simulates an equivalent inductor L_{eq} given as:

$$L_{eq} = r^2 C \tag{9.3}$$

Obviously, instead of using a capacitor C, termination can be done using any general load impedance $Z_L(s)$ and in that case, the simulated input impedance will become:

$$Z_{in}(s) = r^2/\{Z_L(s)\} \tag{9.4}$$

As mentioned earlier, the current–voltage relation of a *simplified* gyrator is presented in equation (9.1). In a general gyrator, the admittances in equation (9.1) are not necessarily equal, that is

$$(I_1/V_2) = y_{12} = (-1/r_2) = g_{m2} \text{ and } (I_2/V_1) = y_{21} = (1/r_1) = -g_{m1} \tag{9.5}$$

The equivalent circuit of a general gyrator (Figure 9.4) can be obtained from equation (9.5). It is obvious that the practical realization of a gyrator is easy in terms of transconductance elements. Such a circuit, transconductance amplifier-based filter circuits, will be studied later in Chapter 15. Practical realization of gyrators using OAs will be discussed in the next section.

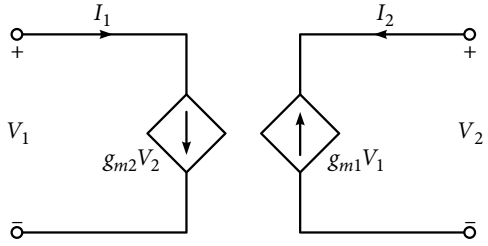


Figure 9.4 Small signal equivalent circuit of a general gyrator.

In a general ladder structure, it is also important to simulate FIs depending on the selected passive structure. Simulation of FIs is rather difficult and requires a cascade of two grounded gyrators and an embedded capacitor, as shown in Figure 9.5 [9.3]. Practical realization of an FI will be discussed after obtaining the practical realization of a GI.

https://doi.org/10.1017/9781108762632.010 Published online by Cambridge University Press

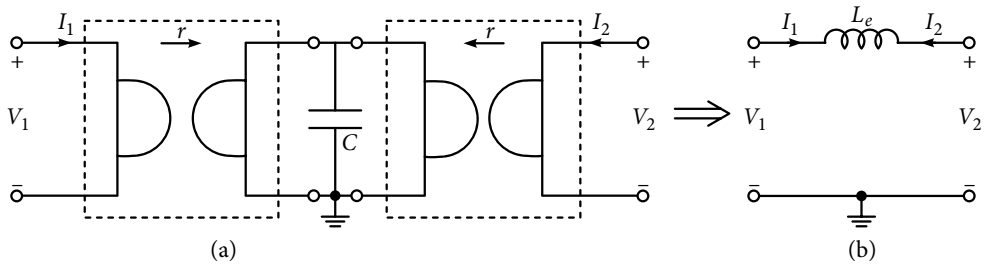


Figure 9.5 (a) Floating inductance simulation using back-to-back gyrators and (b) equivalent circuit.

9.3 Impedance Converters Using Operational Amplifiers

The terms 'gyrator' and 'impedance converter' can be used interchangeably as both convert the nature of impedance connected as termination. A general configuration which has been employed for the development of the impedance converter is shown in Figure 9.6. This configuration is found suitable for developing impedance converter circuits using OAs. In Figure 9.6, the schematic consists of R_1, a feedback resistor, and a *two-port network*, which has to be determined in order to make it an impedance converter. Assuming the two-port network has infinite input impedance and zero output impedance, it is desired to get the following voltage–current relation for simulating inductance at the input terminals.

$$(V_{in}/I_{in}) = Z_{in}(s) = sL \tag{9.5}$$

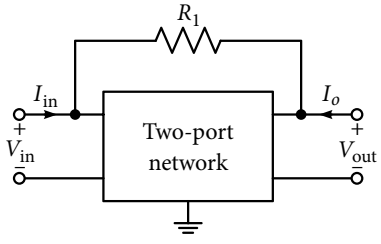


Figure 9.6 A schematic for impedance conversion.

With no current flowing into the two-port, $I_{in} = (V_{in} - V_{out})/R_1$, so substituting I_{in} in equation (9.5):

$$V_{in} = sL\frac{V_{in} - V_{out}}{R_1} \rightarrow \left(\frac{V_{out}}{V_{in}}\right) = (1 - R_1 / sL) \tag{9.6}$$

The required transfer function for the network, as shown in equation (9.6) is obtained by subtracting the gain of an integrator from a unity gain amplifier. Figures 9.7(a) and (b) show simple and known circuits for the non-inverting gain of 2 and the inverting ideal integrator with additional non-inverting input. These circuits are joined in Figure 9.7(c) for which

https://doi.org/10.1017/9781108762632.010 Published online by Cambridge University Press

$V_2 = 2V_{in}$. With both the input terminals of OA2 being at the same potential V_{in}; the current–voltage relations for OA2 and at the input terminal gives the following relations:

$$(V_2 - V_{in})/R \rightarrow (V_{in}/R) = (V_{in} - V_{out})sC \tag{9.7}$$

$$I_{in} = (V_{in} - V_{out})/R_1 \tag{9.8}$$

Elimination of V_{out} in equations (9.7) and (9.8) gives:

$$Z_{in} = (V_{in}/R) = sCRR_1 \tag{9.9}$$

Hence, the circuit shown in Figure 9.7(c), which is known as the Riordan inductance simulation circuit [9.4] simulates an inductor with value $L = CRR_1 = CR^2$ for $R = R_1$.

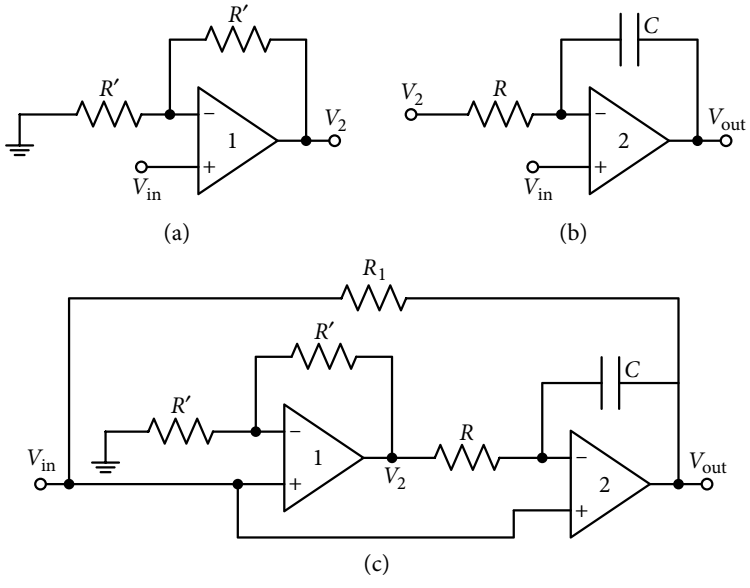


Figure 9.7 (a) Non-inverting amplifier with gain = 2, (b) Ideal non-inverting integrator and (c) Riordan inductance simulator circuit, performing impedance conversion through a combination of (a) and (b).

9.4 Antoniou's Inductance Realization

There are other possible configurations to realize the two-port network shown in Figure 9.6. A well-known configuration employs a non-inverting amplifier of Figure 9.8(a) and the inverting integrator in a differential input mode as shown in Figure 9.8(b). Here the feedback resistor of a difference amplifier is replaced by a capacitor C and the non-inverting terminal gets a potentially divided input $V_2 = V_1R_5/(R_4 + R_5) = kV_1$. Applying KVL (Kirchhoff's voltage law)

https://doi.org/10.1017/9781108762632.010 Published online by Cambridge University Press

at the input terminal of the OA2 in Figure 9.8(b) and with the knowledge that the amplifier is an ideal OA with the inverting terminal voltage being equal to V_2, we get:

$$(V_1 - V_2)/R_3 = (V_2 - V_{out})sC_2 \tag{9.10}$$

or $$(V_{out}/V_1) = k + \{(k-1)/(sC_2R_3)\} \tag{9.11}$$

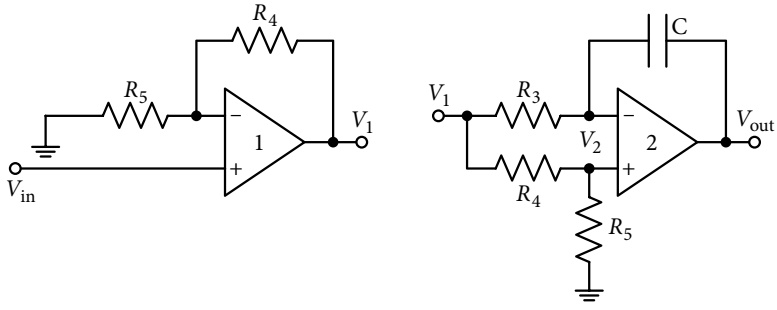


Figure 9.8 (a) A non-inverting amplifier with gain $(1 + R_4/R_5)$, and (b) inverting integrator in differential mode.

To make the circuit compatible with the relation of equations (9.6), k is to be eliminated in equation (9.11). It is done using a non-inverting amplifier with gain, $1 + (R_4/R_5) = (1/k)$ as shown in Figure 9.8(a) at the input terminal V_1 of Figure 9.8(b). However, connecting in this manner will result in a circuit containing five resistors (and one more resistor R_1 as feedback resistor). Instead, two resistors in the non-inverting amplifier can be saved by connecting the amplifier's inverting terminal directly to the inverting terminal of the OA2, whose voltage is also $V_2 = (kV_1)$ and $V_1 = (V_{in}/k)$. The resulting circuit, in addition to the feedback resistor R_1, is now shown in Figure 9.9(a). Analysis of the block inside the dotted line gives the following relation.

$$\frac{V_{out}}{V_{in}} = \left(1 - \frac{R_4}{sC_2R_3R_5}\right) \tag{9.12}$$

Comparing equation (9.12) with equation (9.6), the simulated inductance has the following expression

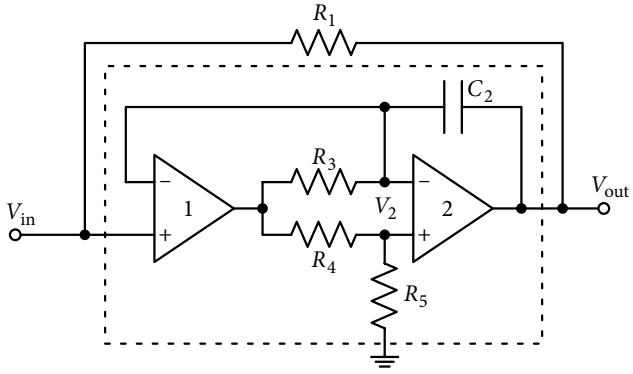
$$L_{eq} = (R_1R_3R_5C_2/R_4) \tag{9.13}$$

The circuit shown in Figure 9.9(a) is known as Antoniou's generalized impedance converter [9.5] of type I. Though presently it is shown to be simulating inductance, we will see later that its generalized form can be that of a generalized impedance converter (GIC). Type II GIC is obtained by simply interchanging R_4 with C_2, as shown in Figure 9.9(b), for which, the simulated inductance is given as:

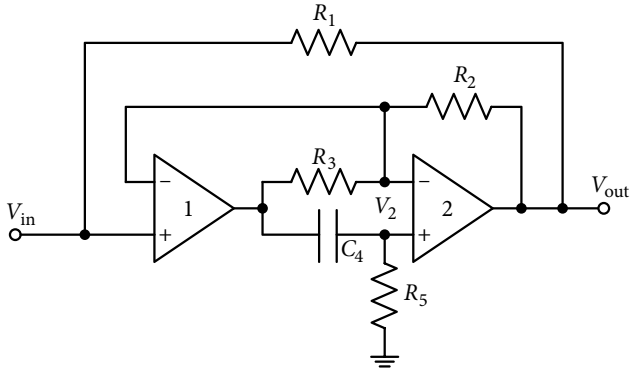
https://doi.org/10.1017/9781108762632.010 Published online by Cambridge University Press

$$L_{eq} = (R_1R_3R_5C_4/R_2) \tag{9.14}$$

If all the resistances used are selected equal in both types of GICs, the simulated inductance becomes $L_{eq} = R^2C$; the same as obtained before in equation (9.9). It is to be noted that for the GIC, comparing the constant with the gyrator-based simulator, gyration constant $r = R$.



(a)



(b)

Figure 9.9 (a) Antoniou's general impedance convertor type I. (b) Antoniou's generalized impedance converter type II.

GICs have been used extensively for element simulations. Because of their importance, GIC needs to be studied carefully. Hence, instead of restricting the study to the GICs of Figure 9.9(a) and (b), the circuit configuration is redrawn in a form which is common in use and convenient for analysis. Figure 9.10 shows a general Antoniou's GIC in dotted rectangles; it was briefly discussed in Chapter 8 as well. Assuming OAs as ideal, voltage V_1, V_3, and V_5 shall be equal and the input impedance of the GIC is easily obtained as

$$Z_{in}(s) = \{Z_1(s)Z_3(s)Z_5(s)\}/\{Z_2(s)Z_4(s)\} \tag{9.15}$$

GICs of type I and II can easily be shown to be special cases of this general configuration. The general form is called the *generalized impedance converter* because of its ability to realize many

https://doi.org/10.1017/9781108762632.010 Published online by Cambridge University Press

other types of impedances depending on the kind of elements (or combination of elements) used for Z_i, i = 1 to 5. For example, selecting $Z_i = R_i$, i = 1, 2, 3 and 5 and $Z_4 = 1/sC$, the input impedance will be the same as for equation (9.14).

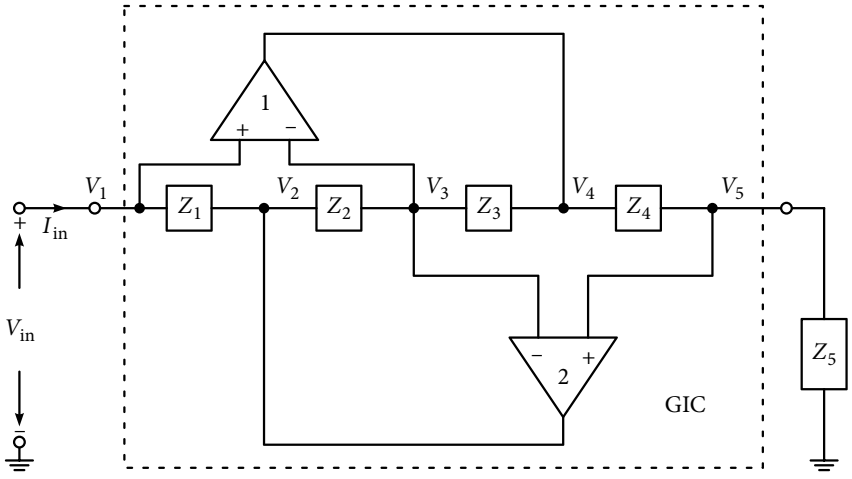


Figure 9.10 Commonly used structure for a generalized impedance converter.

9.5 Filter Realization Using Inductance Simulation

Once inductance simulation through an active RC circuit becomes available, active simulation of the LC ladder becomes simple enough. The obvious starting point is obtaining the passive filter structure and the values of the elements used. Inductances are then replaced by suitable active RC structures and the rest of the capacitors and resistors remain connected in the same position/location. Hence, the resulting overall circuit becomes an active RC structure.

Figure 9.11(a) shows the structure of a third-order HP passive filter section. This passive structure is suitable for the inductance simulation technique as it employs a GI. Hence, the structure shown in Figure 9.10 is easily used to simulate the inductor. Once the inductor is replaced, an active RC version of the third-order HP filter is conveniently obtained. It may be noted that the passive HPF is shown to have normalized terminating resistors R_1 and R_2. The element values of C_1, L_2 and C_3 are easily available from design tables [1.2]. Hence, for the given value of L_2, element values of the inductance simulator are evaluated using equation (9.14).

Example 9.1: Design a third-order HP active filter using the inductance simulation technique, having pass band ripples less than 1 dB and corner frequency of 200 krad/s. Compare its response with that of the passive filter.

Solution: For the given specifications, the circuit shown in Figure 9.11(a) will satisfy the requirements with the following normalized element values:

$$R_1 = R_2 = 1\Omega,\ C_1 = C_3 = 0.62645 \text{ F and } L_2 = 0.9118 \text{ H} \tag{9.16}$$

https://doi.org/10.1017/9781108762632.010 Published online by Cambridge University Press

Using an impedance scaling factor of 10^4 and a frequency scaling factor of 200 krad/s, the denormalized element values for the passive filter from equation (9.16) will be:

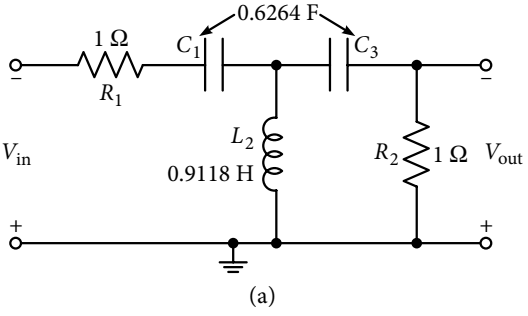
$$R_1 = R_2 = 10^4\ \Omega,\ C_1 = C_3 = 0.31322\ \text{nF and}\ L_2 = 0.04559\ \text{H} \tag{9.17}$$

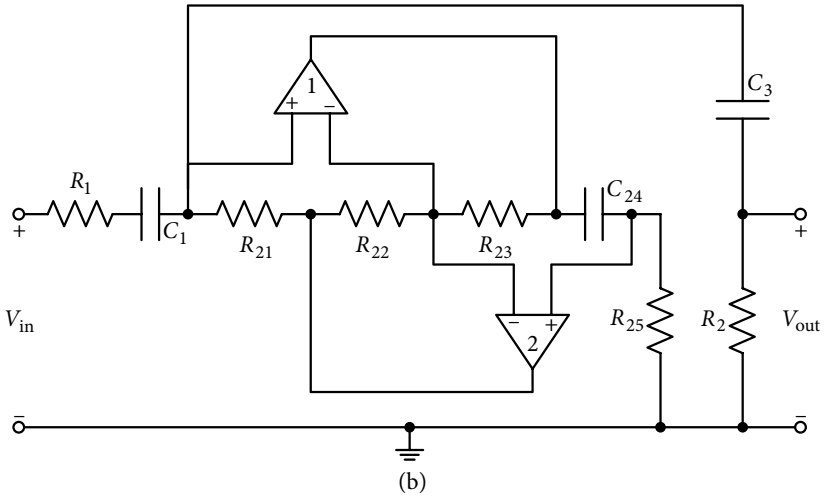
For conversion of a passive filter to an active form, inductance L_2 from equation (9.17) is simulated using the circuit shown in Figure 9.10 and equation (9.14).

$$L_2 = 0.04559\ H = CR^2 \rightarrow C = 0.4559\ \text{nF with}\ R = 10^4\ \Omega \tag{9.18}$$

The GI shown in Figure 9.10, having element values as in equation (9.18), is substituted in Figure 9.11(a), resulting in the circuit shown in Figure 9.11(b). The simulated response is shown in Figure 9.11(c) with the following important observations.

Voltage gain at high frequencies = 0.4626, peak voltage gain = 0.498, ripple width = 0.88 dB and corner frequency = 28.63 kHz (179.96 krad/s). Obviously, there is a significant difference between simulated and design value of the corner frequency (–10.02%), and the high frequency gain is dropped by nearly 7.48%, though the shape of the characteristic remains intact. Deviations in parameters are due to the effect of the frequency-dependent gain





https://doi.org/10.1017/9781108762632.010 Published online by Cambridge University Press

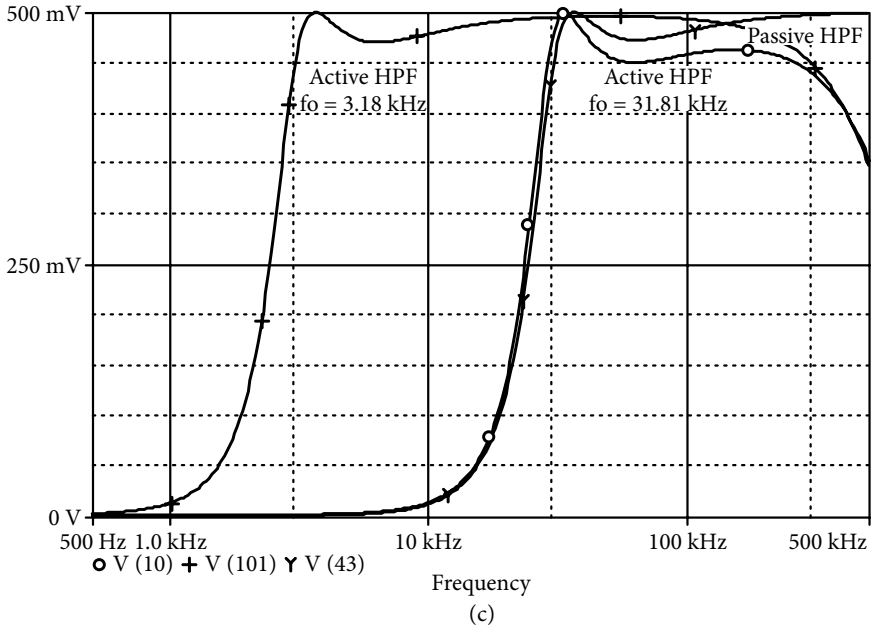


Figure 9.11 (a) A third-order normalized passive high pass filter structure for Example 9.1. (b) The active RC version of Figure 9.11(a) through simulation of grounded inductance L_2 with inductance simulation using GIC (c) Response of the active third-order high pass filter from Figure 9.11(b) at lower and higher corner frequencies, and the response of the passive filter of Figure 9.11(a).

of the OA model. The same active filter, which is simulated for a lower corner frequency of 20 krad/s, had the following element values:

$$C_1 = C_2 = 3.132 \text{ nF}, L_2 = 0.4559 \text{ H} \rightarrow C_{24} = 4.554 \text{ nF} \tag{9.19}$$

The simulated response is also shown in Figure 9.11(c) with the following observations:

Voltage gain at higher frequencies = 0.496, corner frequency = 3.15 kHz and ripple width = 0.5376 dB. Error in the corner frequency is now only –1% and gain deviates only by 0.8%.

Figure 9.11(c) also shows the PSpice simulated response of the passive filter which we can compare with that of the response of the active filter. The following are the observations.

Voltage gain = 0.5, ripple width = 0.5086 dB and corner frequency = 31.83 kHz (200.1 krad/s). The filter's voltage gain remains constant even at much higher frequencies, as it is not affected by the limitation of the OA.

9.6 Floating Inductance Simulation

In the last section, we saw an example of a GI simulation in a simple passive circuit. Quite often, a floating inductor (FI) also becomes a necessity and it has to be simulated as well. The FI shown in Figure 9.5(b) being a two-port structure is represented in terms of *y* parameters as:

https://doi.org/10.1017/9781108762632.010 Published online by Cambridge University Press

$$[y]=\frac{1}{sL_{eq}}\begin{bmatrix}1 & -1\\ -1 & 1\end{bmatrix} \tag{9.20}$$

For the simulation of an FI, two gyrators in back-to-back form are to be joined as shown in Figure 9.5(a). In order to obtain a circuit realization of an FI using two back-to-back gyrators, the well-known technique of *lifting the element terminal from the ground* [9.6] is used on a GI circuit like that used in the circuit in Figure 9.10. The resulting configuration is shown in Figure 9.12. It is important to note that while using any circuit involving OAs, care has to be taken that a path for the flow of bias current remains available. Hence, for the circuit realization of the FI shown in Figure 9.12, a resistance each may be connected in parallel with the capacitors to enable the flow of biasing current. However, these extra resistors have to be of high value so that the parasitic inductance introduced due to these resistances is not significant.

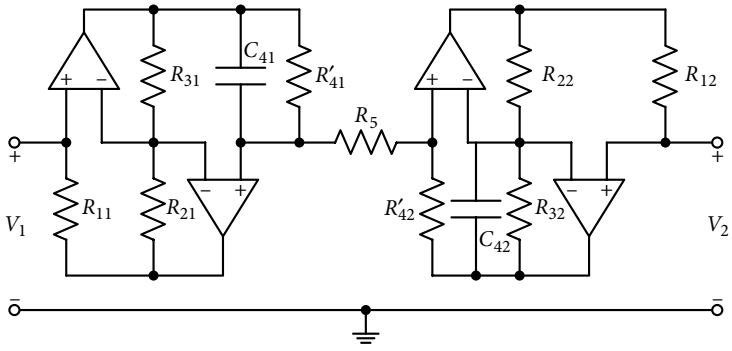


Figure 9.12 Floating inductance realization using back-to-back gyrator based grounded inductance simulators.

The major limitation of the process is that an FI simulator uses a large number of passive and active elements. Another significant issue crops up when the two gyrators are connected back-to-back. The gyrator constants need to be the same; otherwise, there will be a mismatch and the unity element in equation (9.20) will not be exactly unity, resulting in some parasitic elements. Obviously, it is not practically possible to exactly match the component values even in the IC form (mismatch can be minimized). This is a drawback in using such a configuration for FI. Hence, we need to look at other techniques of obtaining an FI circuit which do not require component matching. An alternative is to select a circuit which needs a lesser number of FIs. It is to be noted that L_{eq} in equation (9.20) will have the same expression as L_{eq} in equation (9.13) or (9.14) for GI.

Example 9.2: For the passive BPF shown in Figure 9.13(a), obtain an active RC filter using the inductance simulation method. Find the element values used with the center frequency of the filter as 20 kHz and bandwidth as 2 kHz.

Solution: The transfer function of the BPF of Figure 9.13(a) is obtained as:

$$(V_2/V_1) = (R/L)s/\{s^2 + (R/L)s + (1/LC)\} \tag{9.21}$$

https://doi.org/10.1017/9781108762632.010 Published online by Cambridge University Press

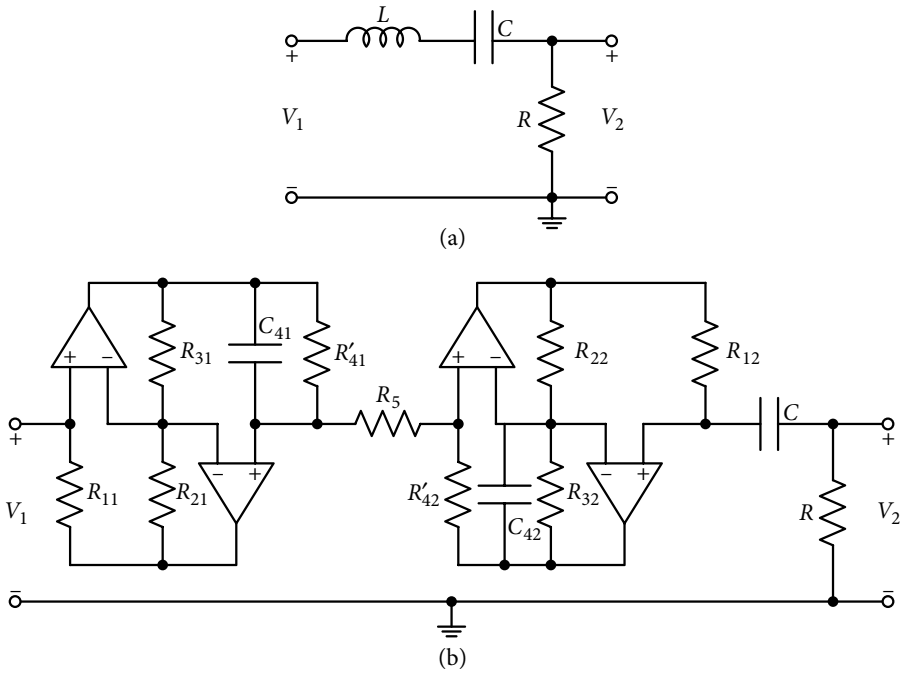


Figure 9.13 (a) Second-order prototype passive band pass filter, (b) its active RC version while simulating a floating inductor using the circuit shown in Figure 9.12. All resistances = 10 kΩ, but R = 1 kΩ and $R'_{41} = R'_{41}$ = 10 MegΩ, $C_{41} = C_{42} = C$ = 0.795 nF.

The important parameters of the filter are as follows:

$$\omega_o = \frac{1}{(LC)^{1/2}}, Q = \frac{1}{R}\left(\frac{L}{C}\right)^{1/2} \text{ and mid-band gain} = 1.0 \tag{9.22}$$

For ω_o =1 rad/s, the normalized element values from equation (9.22) are:

$$L = 1 \text{ H}, C = 1 \text{ F and as } Q = (20/2) = 10, R = 0.1\ \Omega \tag{9.23}$$

For the passive filter, an impedance scale factor of 10^4 and a frequency scaling factor of $20(2\pi)$ krad/s is used; this gives the following de-normalized element values:

$$R = 1\ \text{k}\Omega, C = 0.7954 \text{ nF and } L = 0.07954 \text{ H} \tag{9.24}$$

For the floating inductance, L = 0.07954 H, the circuit shown in Figure 9.12 is inserted in Figure 9.13(a) and application of equation (9.14) to find the element values for inductance gives an active filter circuit as shown in Figure 9.13(b). Resistances R_1, R_2 and R_3 in both the gyrators are 10 kΩ, and capacitances C_{41} and C_{42} are equal to 0.7954 nF. It is important to note that R_5 is $10^4\ \Omega$ and not the summation of two R_5s while connecting two back-to-back circuits, as one resistor acts as the terminating resistor for both sides. Bypass resistors R'_{41} and

https://doi.org/10.1017/9781108762632.010 Published online by Cambridge University Press

R'_{42} are selected as 10 megΩ each, sufficient to allow the passage of bias current, and large enough so that their effect is minimal on the filter performance. The circuit is simulated and the response shown in Figure 9.14.

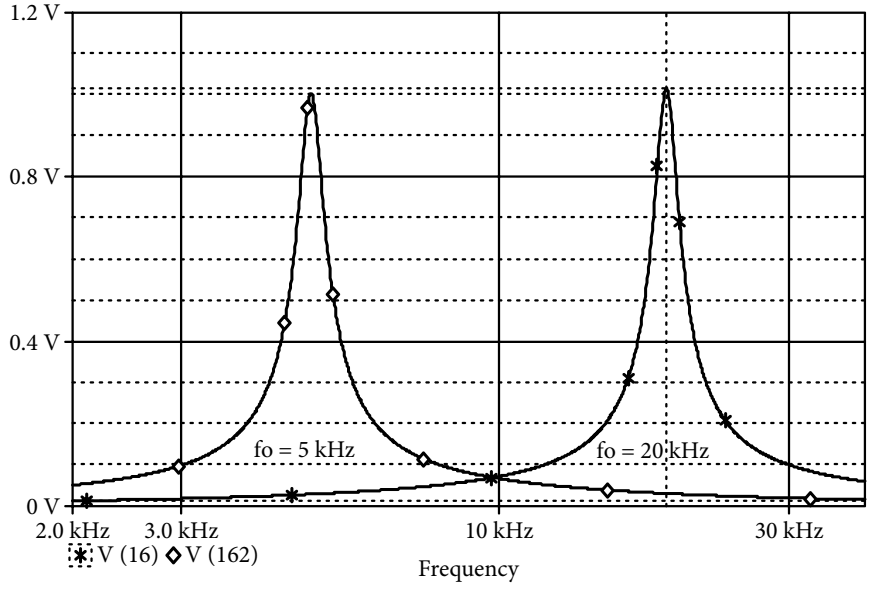


Figure 9.14 Magnitude response of the active band pass filter shown in Figure 9.13(b) at lower and higher center frequencies.

The simulated value of the mid-band gain is 1.017, center frequency is 18.889 kHz, upper and lower cut-off frequencies are 19.778 kHz and 18.027 kHz, respectively. Bandwidth being 1.756 kHz, Q becomes 10.75. Obviously, the main reason for deviation in the parameters is due to the frequency dependence of the OAs gain.

The same BPF was simulated for a lower center frequency of 5 kHz. All the calculated resistances remain the same but all the capacitances are now 3.1818 nF. The simulated magnitude response in this case is also shown in Figure 9.14. Mid-band gain was found to be 0.9987 at a center frequency of 4.927 kHz. The upper and lower cut-off frequencies of 5.177 kHz and 4.690 kHz, respectively gave Q = 10.11; this is now, a much smaller deviation in filter parameters, because of lower working frequency.

9.7 Generalized Inductance Simulation

The inductance simulation method is more useful for the circuit having inductances in grounded forms. Whenever FI is to be simulated, it involves a large number of components and their matching as well. It becomes a little confusing when a circuit contains both GIs and FIs. However, a technique known as the Gorski-Popiel (GP) embedding technique [9.7] is

https://doi.org/10.1017/9781108762632.010 Published online by Cambridge University Press

of great help in simulating a combination of GIs and FIs, which will require a lesser number of elements compared to the case of conventional direct simulation of GIs and FIs. In this technique, instead of simulating individual inductors, a complete sub-network comprising inductors (any number) is simulated through a GIC. This simulated network then simply replaces the original sub-network of the inductors.

To understand the generalized inductance simulation (GIS) technique, consider the GIC circuit shown in Figure 9.10 in the form of a two-port network, as shown in Figure 9.15(a). Assuming the OAs to be ideal means $V_2 = V_1$, and with $R_2 = R_3$ and Z_5 of Figure 9.10 replaced by (V_2/I_1), we get the driving point impedance at port 1 as

$$(V_2/I_1) = (sC_4R_1)(V_2/I_2) \tag{9.25}$$

Obviously, when the simplified block form of GIC shown in Figure 9.15(b) is terminated in a resistance R_1, the input will be an inductance as before, with the inductor expression as:

$$L_{eq} = (C_4R_1)R = L'R \tag{9.26}$$

The GIC in the block form, terminated in a resistance as shown in the dotted rectangle in Figure 9.15(b), yields the following from equation (9.25):

$$I_2 = (sC_4R_1)I_1 = (sL')I_1 \tag{9.27}$$

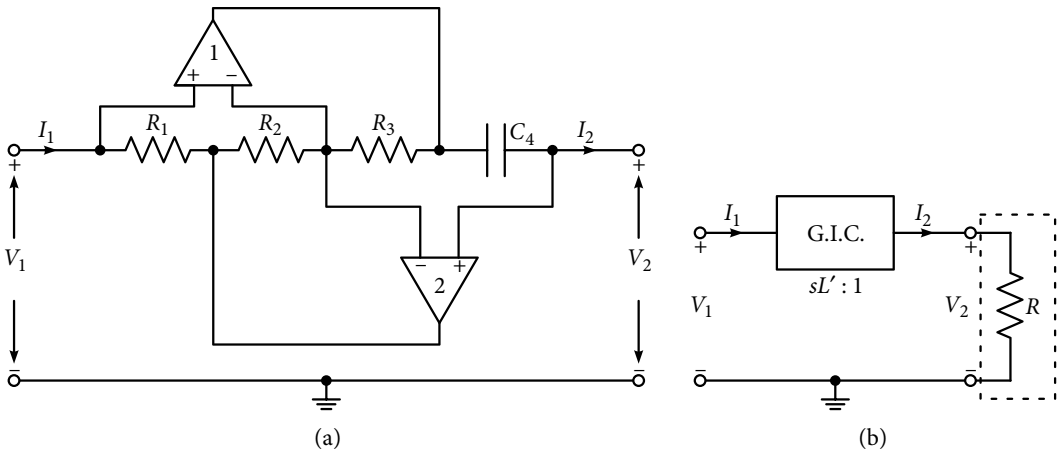


Figure 9.15 (a) Generalized impedance convertor as a two-port network and (b) representation of the GIC in a block form.

The important conclusion of the exercise is that if a GIC is placed at the input branch of a resistor, the resistor gets converted into an inductor. According to the generalized inductor simulation scheme, any number of branches of a network can have a GIC at its input which

https://doi.org/10.1017/9781108762632.010 Published online by Cambridge University Press

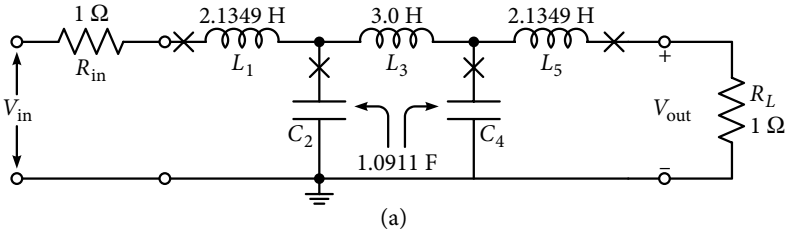
will convert all terminating resistors as inductors. In order to simulate an inductor L_{eq}, the terminating resistor value will be:

$$(L_{eq}/L') \rightarrow (L_{eq}/C_4R_1) \tag{9.28}$$

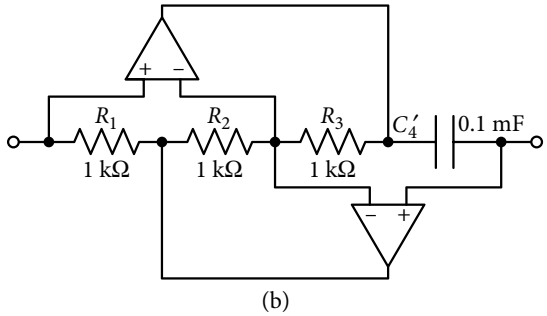
From the point of view of IC fabrication of the active filter, it is preferable to use the same GICs with varying terminating resistors for the simulation of inductors with different values. However, if it results in a situation where the terminating resistor value becomes unsuitable for IC fabrication, a different GIC can be used.

Example 9.3: Realize a fifth-order Chebyshev LPF having a maximum of 1 dB ripples in the pass band. Let the corner frequency be 10 krad/s; use the GP technique.

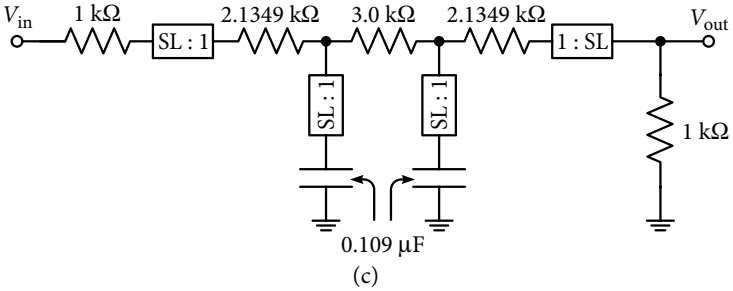
Solution: Figure 9.16(a) shows the ladder structure and the normalized element values of the filter for the given specifications from Table 3.5. Cross points have also been shown in the figure for the application of the GP technique, where terminated GIC circuits will be inserted.



(a)



(b)



(c)

https://doi.org/10.1017/9781108762632.010 Published online by Cambridge University Press

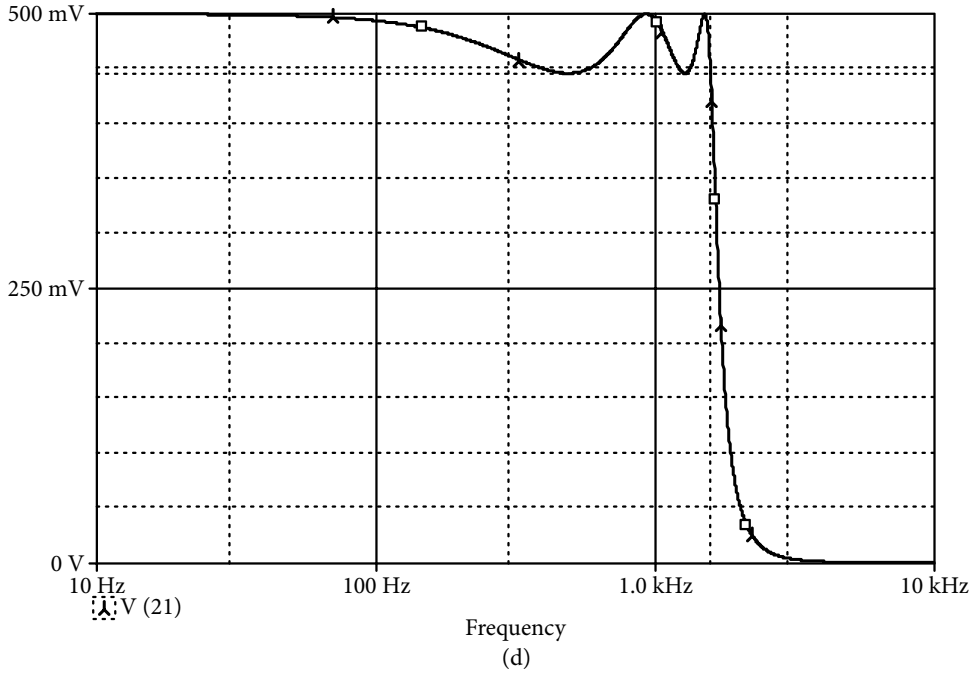


Figure 9.16 (a) Fifth-order passive Chebyshev filter for Example 9.3 (b) GIC circuit, with elements values, which is to be terminated and (c) the active version of the filter using the Gorski-Popiel ladder embedding technique. (d) Magnitude response of the filter in Figure 9.16(c).

Application of the frequency scaling factor of 10 krad/s and an impedance scaling factor of 10^3 results in the following element values:

$$R_{in} = R_L = 1\ \text{k}\Omega,\ L_1 = L_5 = 0.21349\ \text{H},\ L_3 = 0.3\ \text{H},\ \text{and}\ C_2 = C_4 = 0.10911\ \mu\text{F} \tag{9.29}$$

Since for the realization of inductances, terminated GICs are to be used at the cross point, Figure 9.16(b) shows a GIC in which resistances $R_1 = R_2 = R_3 = 1\ \text{k}\Omega$ each. If C_4' is selected as 0.1 μF, the terminating resistances for the inductors L_1 and L_5 of equation (9.29) will be calculated using equation (9.14) as:

$$R_{L1} = R_{L5} = \frac{10^3 \times 0.21349}{10^3 \times 10^3 \times 10^{-7}} = 2.1349\,\text{k}\Omega \text{ and } R_{L3} \text{ will be } 3.0\ \text{k}\Omega$$

Figure 9.16(c) shows the structure of the active ladder, where the GIC circuit of Figure 9.16(b) will be substituted at the four places as indicated; for the rightmost GIC, the inverted direction needs to be noted. The circuit was simulated and the magnitude response is shown in Figure 9.16(d), for which dc gain is 0.5, ripple width is 0.995 dB and pass band edge frequency are 1.584 kHz (9.956 krad/s); very close to the design values.

https://doi.org/10.1017/9781108762632.010 Published online by Cambridge University Press

9.8 Filter Realization Using FDNR

Instead of replacing inductors through an active RC simulator, an alternate scheme was given by *L*. Bruton in 1969 [9.8]. In this scheme, all the elements are multiplied by a factor $(1/s)$. Such a transformation converts an inductive impedance (sL) to a resistor element of value L ohms. At the same time, it converts a resistor (R) to a capacitive element (R/s), that is, a capacitor with value $(1/R)$ farad. However, the capacitive impedance $(1/sC)$ gets converted to $(1/s^2C)$; not a conventional element. For $s = j\omega$, this converted impedance is:

$$Z_c' = (1/s^2C)\Big|_{s=j\omega} = -1/\omega^2C \tag{9.30}$$

Equation (9.30) shows that the impedance is negative, real and frequency dependent; hence, an appropriate name would be *frequency dependent negative resistance* (FDNR). Sometimes, it is also called a *super capacitor* as it is converted from a capacitor, and a usual symbol for it is three parallel lines. It is necessary to note that the transformation of element impedances by $1/s$ does not affect the transfer function of the network as it is a ratio of two polynomials in s.

After the transformation, RLC circuit now comprises resistors, capacitors and FDNRs (an RCD network). Obviously, to convert an RLD network to an active RC form, the FDNRs have to be simulated in the same way as the inductances were simulated, be it in the grounded or in the floating form. Fortunately, a large number of active RC circuits are available in literature for simulating FDNRs. One such circuit is obtained through the use of the GIC shown in Figure 9.10, for which the input impedance is given as

$$Z_{in}(s) = Z_1Z_3Z_5/Z_2Z_4 \tag{9.31}$$

Selecting $Z_1 = 1/sC_1$, $Z_5 = 1/sC_5$, $Z_3 = R_3$, $Z_2 = R_2$ and $Z_4 = R_4$, as shown in Figure 9.17(a), the circuit provides a grounded FDNR with the expression of its impedance as given here.

$$Z_{in}(s) = \frac{R_3}{s^2C_1C_5R_2R_4} = \frac{1}{s^2D} \text{ with } D = \frac{C_1C_5R_2R_4}{R_3} \tag{9.32}$$

Figure 9.17(b) shows the capacitor's symbolic representation of three parallel lines. Different values for the capacitors C_1 and C_5 and R_2 and R_3 can be chosen, but it does not give any specific advantage. Since equal value capacitors are desirable in integration, we prefer to select $C_1 = C_5 = C$. It has been shown that for a GIC, it is better to use $R_2 = R_3 = R$, hence, a simplified expression of input impedance from equation (9.32) will be as follows:

$$Z_{in}(s) = \frac{1}{s^2C^2R_4} \text{ or } D = C^2R_4 \tag{9.33}$$

Application of the FDNR technique is obviously preferred for those networks which use more grounded capacitors, as such networks will have FDNRs in the grounded mode. At the same time, the floating inductance gets converted to resistors. For simulating FDNR in floating form, the method of realization and limitations are exactly the same as those in the case of FIs.

https://doi.org/10.1017/9781108762632.010 Published online by Cambridge University Press

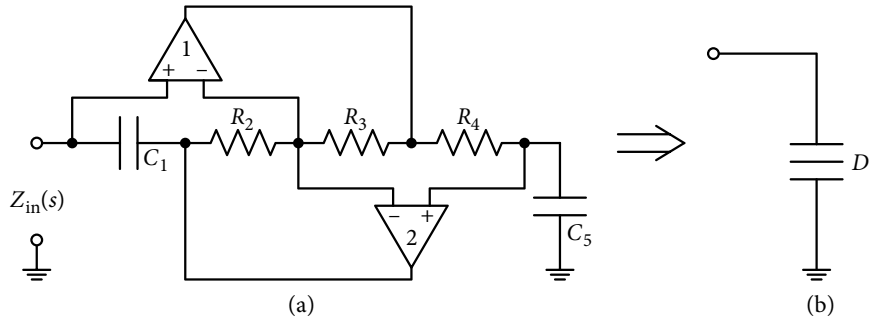


Figure 9.17 (a) Circuit diagram of a grounded FDNR obtained through GIC and (b) its symbolic representation.

While using the FDNR technique of converting passive RLC circuits to an active RC, there are certain practical glitches that need to be removed. For a doubly resistor-terminated ladder, the source resistor and the load resistor also get transformed to capacitors. The following example will help in designing an FDNR based filter and also illustrate the conversion of the two aforementioned resistors. The method of overcoming the practical glitches mentioned here will be discussed after the example.

Example 9.4: Obtain an active RC filter structure using FDNRs from a passive fifth-order Chebyshev LP filter having a cut-off frequency of 100 krad/s, a ripple width of 1 dB with source and load terminating resistors of 10 kΩ.

Solution: The structure and element values of a normalized fifth-order LP passive filter obtained from the standard design table or through the method described in Chapter 3 is shown in Figure 9.16(a). It is a minimum inductance configuration, and its normalized element values are already given in equation (9.29) and repeated here:

$$R_{in} = R_{out} = 1\ \Omega,\ L_1 = L_5 = 2.1349\ \text{H},\ L_3 = 3\ \text{H and}\ C_2 = C_4 = 1.0911\ \text{F}$$

Application of $(1/s)$ transformation on the elements converts it to the circuit elements as shown in Figure 9.18(a).

If we use a normalizing frequency of 100 krad/s, the normalized pass band edge frequency will be at $\omega = 1$.

Once the passive filter structure and its element values are obtained/designed and $(1/s)$ transformation has been performed, the following are the next steps to design the converted FDNR(s).

Using equations (9.33), we get the element values for both FDNRs as:

$$D = 1.0911 \times R_4\ C^2 \rightarrow C = 1.04455\ \text{F for}\ R_4 = 1\ \Omega$$

https://doi.org/10.1017/9781108762632.010 Published online by Cambridge University Press

Inductances converted as resistances will have normalized values as:

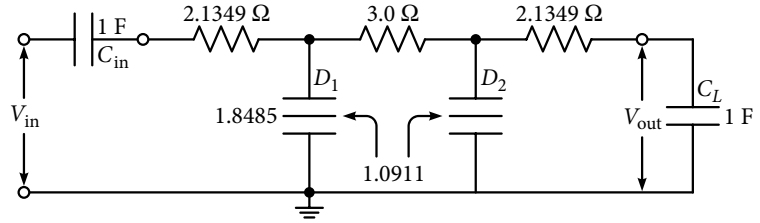
$R_{L1} = R_{L2} = 2.135\ \Omega$ and $R_{L1} = 3.0\ \Omega$.

Active FDNRs are then put in place of D_1, D_2 shown in Figure 9.18(a). The values of the resistor R_2 and R_3 are not selected so far; they are arbitrary and can also be selected after frequency and impedance de-normalization. The frequency de-normalization factor being 100 krad/s, we select an impedance normalization factor of 10 kΩ. The final circuitry of the active RC fourth-order LPF is shown in Figure 9.18(b) with the de-normalized value of the elements as follows:

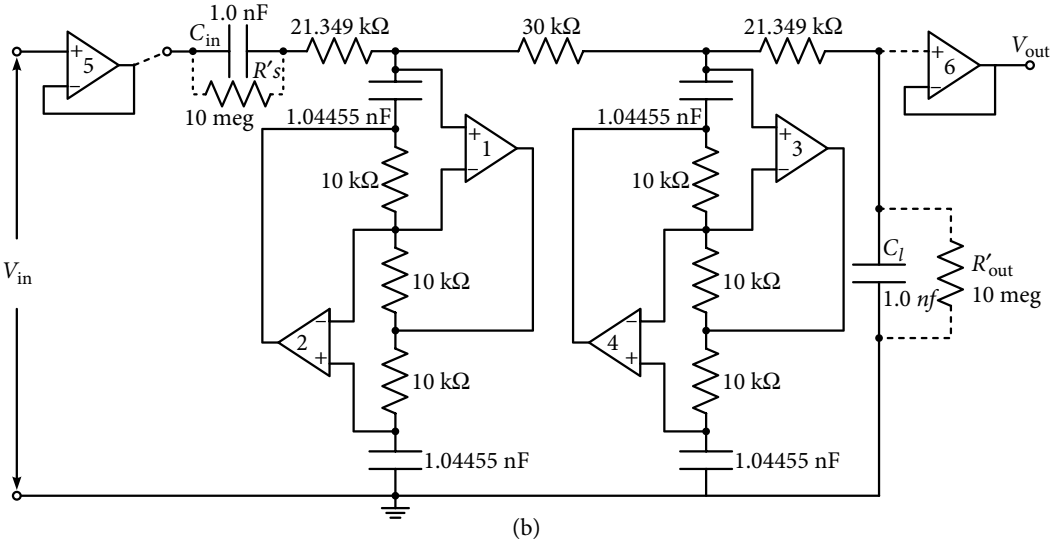
$C_{11} = C_{51} = C_{12} = C_{52} = 1.04455$ nF, $R_{41} = R_{42} = 10$ kΩ

$R_{L1} = R_{L3} = 21.349$ kΩ and $R_{L2} = 30$ kΩ

Resistors R_2 and R_3 in each FDNR are selected as 10 kΩ, an arbitrary value; this equals resistor values already used in the circuit.



(a)



(b)

https://doi.org/10.1017/9781108762632.010 Published online by Cambridge University Press

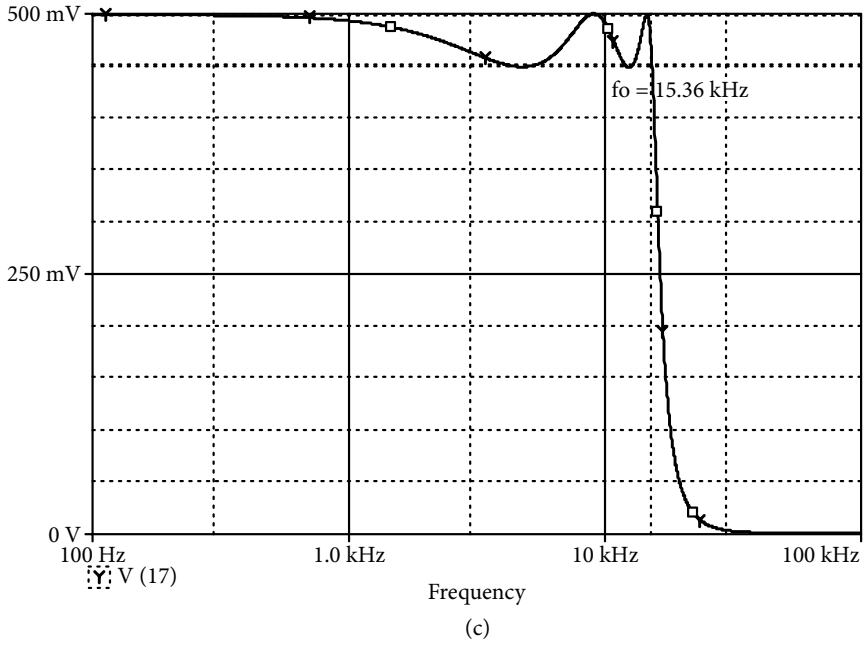


Figure 9.18 (a) Fifth-order passive doubly terminated low pass filter structure after ($1/s$) transformation and (b) active RC configuration using FDNRs after de-normalization of elements. (c) Response of the filter shown in Figure 9.18(b) while using grounded FDNRs.

Due to the conversion of terminating resistors as capacitors, it can be seen from Figure 9.18(b) that the input biasing current cannot flow in the non-inverting terminal of OA1 and 3 in the same way as in the case of inductance simulation. Using the same remedy in this case as well, the terminating capacitors C_{in} and C_L (1 nF each) are bypassed by large value resistors R'_{in} and R'_{out}, as shown linked through dotted lines in Figure 9.18(b). Obviously, the bypass resistors (which are equivalent to inductors in the original passive RLC circuit) have to be high enough, so as not to significantly affect the response of the filters.

Another issue to be resolved for the practical implementation of the filter is that the termination resistors which have been transformed as capacitors, have to be re-inserted in the circuit as these were not part of the lossless filter structure. The problem is solved through the use of non-inverting buffers at the input and output terminals as shown in Figure 9.18(b).

Figure 9.18(c) shows the PSpice simulated response of the active filter of Figure 9.18(b). Voltage gain at low frequencies is 0.4984, corner frequency is 15.368 kHz (96.6 krad/s) and ripple width is 0.947 dB, with gain at 40 kHz dropping by 62 dBs; a sufficiently good response.

9.9 Principle of Operational Simulation

To begin our discussion on the operational simulation technique, a ladder structure is selected for its simplicity and due to the fact that it is a common structure for filter realizations. Figure 9.19 shows a sixth-order ladder structure in block form along with the currents in the

https://doi.org/10.1017/9781108762632.010 Published online by Cambridge University Press

branches and voltage levels across branch immittances. The block diagram is valid for single or doubly terminated ladders. The circuit can be described in terms of the following currents and voltages.

$$V_1 = V_s - V_2,\ V_3 = V_2 - V_4,\ V_5 = V_4 - V_6 \tag{9.34}$$

$$I_2 = I_1 - I_3,\ I_4 = I_3 - I_5,\ I_6 = I_5 \text{ as } I_7 \text{ is zero} \tag{9.35}$$

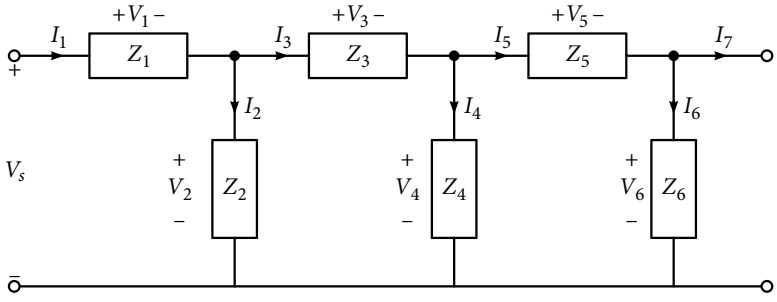


Figure 9.19 Block form representation of a sixth-order doubly terminated ladder. V_s is the source voltage and Z_1 contains the source resistance R_1. Z_6 contains the terminating resistor R_2.

In addition, the current–voltage relation for the series and shunt branches can be written as:

$$I_1 = (V_1/Z_1) = V_1Y_1,\ I_3 = (V_3/Z_3) = V_3Y_3,\ I_5 = (V_5/Z_5) = V_5Y_5 \tag{9.36}$$

$$V_2 = I_2Z_2 = (I_2/Y_2),\ V_4 = I_4Z_4 = (I_4/Y_4),\ V_6 = I_6Z_6 = (I_5/Y_6) \tag{9.37}$$

For the development of the procedure in which current–voltage relations of the branches can be simulated operationally, the aforementioned four equations can be combined in the following form.

$$I_1 = Y_1(V_s - V_2),\ V_2 = Z_2(I_1 - I_3) \tag{9.38a, b}$$

$$I_3 = Y_3(V_2 - V_4),\ V_4 = Z_4(I_3 - I_5) \tag{9.39a, b}$$

$$I_5 = Y_5(V_4 - V_6),\ V_6 = Z_6I_5 \tag{9.40a, b}$$

Apart from the realization of the elements Z_i(or Y_i), which will be taken up later in the chapter, operational simulation faces the following two problems if the circuit is to be realized using OAs.

The first problem is that in equations (9.38) to (9.40), if the output side is in terms of voltage, the input is current or vice versa, whereas in the OAs, both input and output are in terms of voltages. The second problem is that summation of voltages is easier while using OAs, but differencing them is a bit involved. Both the problems are solved step by step.

https://doi.org/10.1017/9781108762632.010 Published online by Cambridge University Press

The first of the two problems is solved by scaling equations (9.38) to (9.40) by a resistor R' and changing their way of representation. Hence, for equation (9.38a), we can write:

$$R'I_1 = R'Y_1\,(V_s - V_2) \tag{9.41a}$$

In equation (9.41a), $R'I_1$ becomes a voltage, which we will denote using a lower case voltage symbol with a subscript I as v_{I1}. Use of the lower case symbol is to identify that it was obtained after normalization through R' and subscript I denotes that, initially, this voltage was in the form of current. Another important point is that the term $R'Y_1$, which becomes dimensionless and is the ratio of two voltages as $v_{I1}/(v_s - v_2)$, will also become a transfer function h_{Y1}. Hence, in the modified form, equation (9.41a) is written as:

$$v_{I1} = h_{Y1}(v_s - v_2) \tag{9.41b}$$

In equation (9.41b), subscript $y1$ on the transfer function indicates that it was obtained from admittance Y_1.

Following the same notation, equations (9.38) to (9.40) are written as follows, where both sides of the equation are in terms of voltages.

$$V_2 = (Z_2/R')(R'I_1 - R'I_3) \rightarrow v_2 = h_{z2}\,(v_{I1} - v_{I3}) \tag{9.42}$$

$$R'I_3 = R'Y_3(V_2 - V_4) \rightarrow v_{I3} = h_{Y3}(v_2 - v_4) \tag{9.43}$$

$$V_4 = (Z_4/R')(R'I_3 - R'I_5) \rightarrow v_4 = h_{z4}(v_{I3} - v_{I5}) \tag{9.44}$$

$$R'I_5 = R'Y_5(R'V_4 - R'V_6) \rightarrow v_{I5} = h_{Y5}(v_4 - v_6) \tag{9.45}$$

$$V_6 = (Z_6/R')(R'I_5) \rightarrow -v_6 = h_{z6}(-v_{I5}) \tag{9.46}$$

In the transformed equations (9.41b) to (9.46), only v_{I1} is positive, v_6 has a negative sign and the rest of the voltages v_2, v_{I3}, v_4, and v_{I5} appear in both inverting and non-inverting form and in the voltage differencing form. Since differencing of the voltage is a bit involved, this differencing in voltages is to be avoided; in its place, voltage summation is used. In this case, at least four inverters are needed to get both inverting and non-inverting voltages v_2, v_{I3}, v_4, and v_{I5}. Use of these extra inverters will make the circuit complex and uneconomical. A better alternative is to make those transfer functions, which became available in these equations from the impedances Z_2, Z_4 and Z_6, inverting; h_{zi} is replaced by $-h_{zi}$. Under such a condition, the transformed equations (9.41b) to (9.46) will modify to the following:

$$v_{I1} = h_{y1}\{v_s + (-v_2)\},\ (-v_2) = -h_{z2}\{v_{I1} + (-v_{I3})\} \tag{9.47a, b}$$

$$-v_{I3} = h_{y3}\{(-v_2) + v_4\},\ v_4 = -h_{z4}\{(-v_{I3}) + v_{I5}\} \tag{9.47c, d}$$

https://doi.org/10.1017/9781108762632.010 Published online by Cambridge University Press

$$v_{I5} = h_{y5}\{v_4 + (-v_6)\}, -v_6 = -h_{z6}(v_{I5}) \quad (9.47e, f)$$

Equation (9.47) can be implemented operationally using the symbolic notations shown in Figure 9.20. Now inverters are not required since v_2, v_{I3}, and v_6 are only negative, whereas voltages v_{I1}, v_4 and v_{I5} are only positive. The operational representation of equation (9.47) is shown in Figure 9.21, where only summers are needed. According to convention, signals originating due to current are placed on the upper line in the diagram and signals originating from voltages are placed in the bottom line. Figure 9.21 can be re-drawn as shown in Figure 9.22. It may be noted that every loop in both Figures 9.21 and 9.22 comprise one positive and one negative transfer function; this is important from the stability point of view.

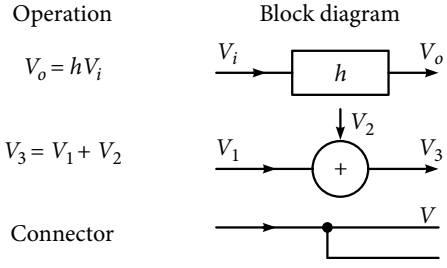


Figure 9.20 Block diagram symbols for the operational equations.

Use of alternate inverting and non-inverting transfer functions in the loop avoid the use of extra inverters, but it creates the possibility of the output being out of phase by 180°; this is not of much significance.

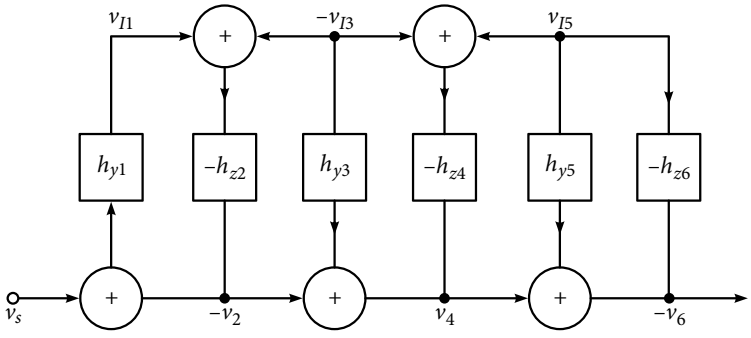


Figure 9.21 Operational representation of equation (9.47).

Avoidance of inverters is achieved by selecting the impedance-based transfer function as negative, resulting in equation (9.47) and its circuit representation in block form is shown in Figures 9.21 and 9.22. Alternatively, in the same way, admittance-based transfer functions

https://doi.org/10.1017/9781108762632.010 Published online by Cambridge University Press

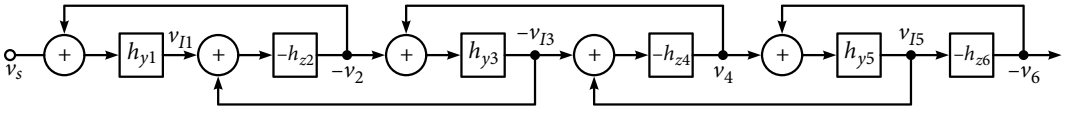


Figure 9.22 An alternate form of presentation of Figure 9.21.

may be made negative. Keeping in mind the negative sign, the transformed parts of equations (9.41) to (9.46) will modify as equations (9.48):

$$-v_{I1} = -h_{y1}\{v_s + (v_2)\},\ -v_2 = h_{z2}\{(-v_{I1}) + v_{I3}\} \tag{9.48a, b}$$

$$v_{I3} = -h_{y3}\{(-v_2) + v_4\},\ v_4 = h_{z4}\{v_{I3} + (-v_{I5})\} \tag{9.48c, d}$$

$$-v_{I5} = -h_{y5}\{v_4 + (-v_6)\},\ -v_6 = h_{z6}\,(-v_{I5}) \tag{9.48e, f}$$

Like in the previous case, equation (9.48) is represented in block form in Figures 9.23 and 9.24. Once the block form of the equations is available, each of the transfer functions is to be realized, which will depend on the element(s) used in a particular series and shunt branch.

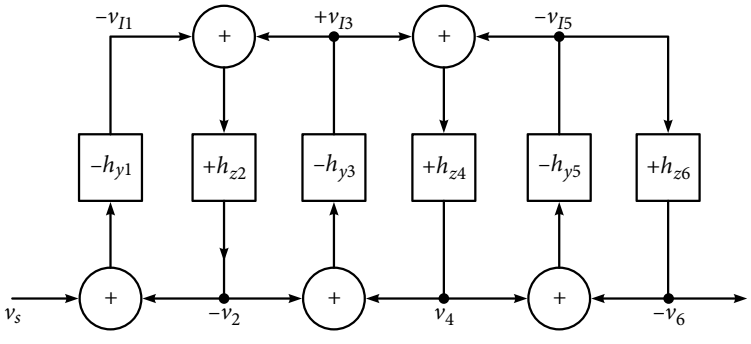


Figure 9.23 Operational block diagram or relationship for equation (9.48).

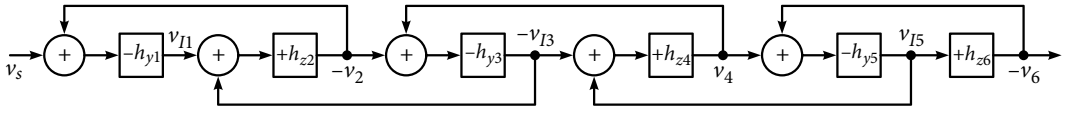


Figure 9.24 An alternate form of Figure 9.23.

The operational simulation method of particular types of ladders will now be discussed while applying the procedure just described.

https://doi.org/10.1017/9781108762632.010 Published online by Cambridge University Press

9.10 Operational Simulation of a Low Pass Ladder

Even when a high pass (HP), band pass (BP) or band stop active or passive filter is to be realized, the procedure begins with a low pass (LP) structure. Later, it is transformed to the desired characteristics. Hence, the general block form structure shown in Figure 9.19 is now taken up to develop a procedure for an operationally simulated LP ladder. Figure 9.25 shows the structure of a sixth-order doubly terminated LPF, for which equations (9.36) and (9.37) will become the branch equations as shown here:

$$I_1 = \frac{V_1}{sL_1 + R_1},\ I_3 = \frac{V_3}{sL_3},\ I_5 = \frac{V_5}{sL_5} \tag{9.49}$$

$$V_2 = \frac{I_2}{sC_2},\ V_4 = \frac{I_4}{sC_4},\ V_6 = \frac{I_5}{sC_6 + G_2} \tag{9.50}$$

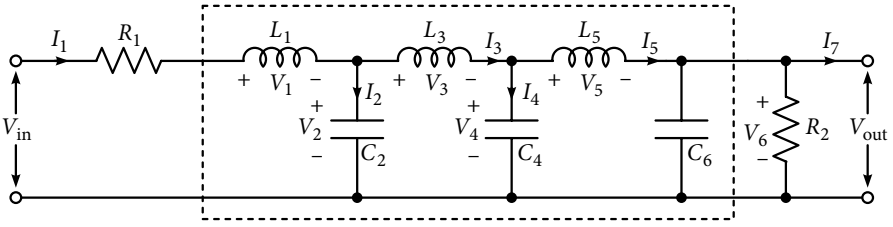


Figure 9.25 A sixth-order doubly terminated low pass ladder structure.

In order to convert the passive ladder into the form of operational representation shown in Figure 9.21 (or 9.22), we need to find the transfer functions h_{Y1}, h_{Y3}, h_{Y5}, h_{Z2}, h_{Z4} and h_{Z6}. To get these transfer functions, all branch immittances are scaled by a resistor R', as it was done in the previous section, and the transfer functions based on impedances, h_{Z2}, h_{Z4}, h_{Z6} are multiplied by (–1) in conformity with equation (9.47) and the block figures in Figure 9.21 or 9.22. Hence, we get:

$$h_{Y1} = R'Y_1 = \frac{R'}{(sL_1 + R_1)} = \frac{1}{\left(\frac{sL_1}{R'} + \frac{R_1}{R'}\right)} = \frac{1}{s\tau_1 + r_1'} \tag{9.51}$$

$$-h_{Z2} = -\frac{Z_2}{R'} = -\frac{1}{sC_2R'} = -\frac{1}{s\tau_2} \tag{9.52}$$

$$h_{Y3} = \frac{1}{sL_3 / R'} = \frac{1}{s\tau_3} \tag{9.53}$$

$$-h_{Z4} = -\frac{1}{sC_4R'} = -\frac{1}{s\tau_4} \tag{9.54}$$

https://doi.org/10.1017/9781108762632.010 Published online by Cambridge University Press

$$h_{Y5} = \frac{1}{sL_5 / R'} = \frac{1}{s\tau_5} \tag{9.55}$$

$$-h_{Z6} = -\frac{1}{sC_6R' + G_LR'} = -\frac{1}{(s\tau_6 + 1/r_L')} \tag{9.56}$$

In equations (9.51) to (9.56), τ_i is the time constant as C_iR' or L_i/R', and $r_i' = R_i / R'$. It is observed that the realization requires a non-ideal non-inverting integrator for equation (9.51), two lossless inverting integrators for equations (9.52) and (9.54), two lossless non-inverting integrators for equations (9.53) and (9.55) and a finite gain inverting integrator for equation (9.56). It may be noted that had it been a case of fifth-order filter without C_6, an inverter would have sufficed for operationally simulating the resistor R_L for equation (9.56).

Hence, the problem boils down to the selection of proper, ideal and non-ideal, inverting integrators and non-inverting integrators. For the integrators, each integrator should have two inputs so that along with integration, it sums two voltages like v_s and $(-v_2)$ and v_{I1} and $(-v_{I3})$. In Chapter 8, a number of inverting and non-inverting integrators have been discussed. Figures 8.5 and 8.6 show inverting integrators, with and without active compensation, and Figure 8.7(a) shows a non-inverting integrator using an inverter. However, all the circuits have one input. We know from the circuit of an OA summer that addition of another resistor at the inverting input will do the job. Another important point is that all these integrators are lossless, and to make them non-ideal, a resistor (like QR) is to be connected in parallel with the feedback capacitor as in the Ackerberg–Mossberg biquadratic circuit shown in Figure 8.7(a). Based on this brief discussion, Figure 9.26(a) shows a two input non-ideal inverting integrator without any compensation and Figure 9.26(b) shows a two input inverting integrator with active compensation. Though any configuration can be used, the choice of this combination has the advantage that in any of the loops, the negative *quality* of the inverting integrator almost cancels the positive *quality* of the non-inverting integrator, making the combination better for an extended frequency range. Feedback resistance R_f has to be made open to realize ideal inverting and non-inverting integrators, as shown in Figures 9.26(a) and (b), respectively.

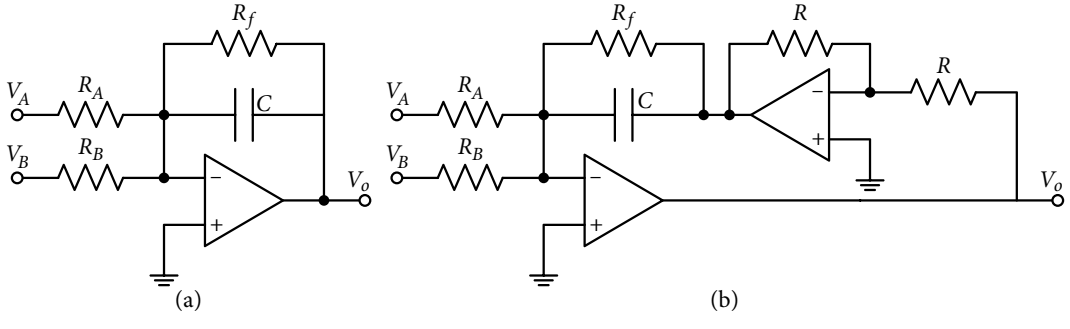


Figure 9.26 (a) A two input non-ideal inverting integrator without compensation and (b) a two input non-ideal non-inverting integrator with active compensation.

https://doi.org/10.1017/9781108762632.010 Published online by Cambridge University Press

For Figure 9.26(a), with OA assumed as ideal:

$$V_o = -\frac{1}{sC + G_f}\left(\frac{V_A}{R_A} + \frac{R_B}{R_B}\right) \tag{9.57}$$

For the active integrator, a scaling factor R_s is used, which is independent of other branch constraints and values in order to provide flexibility in selecting proper component values. Hence, equation (9.57) modifies for the non-ideal integrator as:

$$V_o = -\frac{1}{sCR_s + G_f R_s}\left(\frac{R_s}{R_A}V_A + \frac{R_s}{R_B}V_B\right) = -\frac{1}{s\tau + r_s}(a_1 V_A + a_2 V_B) \tag{9.58}$$

With $G_f = 0$, equation (9.58) will reduce to the following for an ideal integrator:

$$V_o = -\frac{1}{sCR_s}\left(\frac{R_s}{R_A}V_A + \frac{R_s}{R_B}V_B\right) = -\frac{1}{s\tau}(a_1 V_A + a_2 V_B) \tag{9.59}$$

Analysis of the circuit in Figure 9.26(b), taking OAs as ideal gives:

$$V_o = +\frac{1}{sC + G_f}\left(\frac{V_A}{R_A} + \frac{V_B}{R_B}\right) \tag{9.60}$$

Once again scaling it by resistor R_s, equation (9.60) modifies as:

$$V_o = +\frac{1}{sCR_s + G_f R_s}\left(\frac{R_s}{R_A}V_A + \frac{R_s}{R_B}V_B\right) = +\frac{1}{s\tau + r_s}(a_1 V_A + a_2 V_B) \tag{9.61}$$

With $R_f = \infty$, expression for a two-input ideal non-inverting integrator will become:

$$V_o = +\frac{1}{s\tau}(a_1 V_A + a_2 V_B) \tag{9.62}$$

Now the results of the aforementioned equations for non-ideal and ideal cases can be applied on equations (9.51) to (9.56) along with equation (9.47). First, those three equations are taken which are based on admittance-based transfer functions, as these will be realized using the non-inverting integrator shown in Figure 9.26(b) with (or without feedback) resistor R_f.

$$v_{I1} = \frac{1}{\frac{sL_1}{R'} + \frac{R_{\text{in}}}{R'}}\left\{v_s + (-v_2)\right\} = \frac{v_s + (-v_2)}{s\tau_1 + r'_{\text{in}}} \tag{9.63a}$$

$$-v_{I3} = \frac{1}{sL_3 / R'}\left\{(-v_2) + v_4\right\} = \frac{(-v_2) + v_4}{s\tau_3} \tag{9.63b}$$

https://doi.org/10.1017/9781108762632.010 Published online by Cambridge University Press

$$v_{I5} = \frac{1}{sL_5 / R'}\left\{v_4 + \left(-v_6\right)\right\} = \frac{v_4 + (-v_6)}{s\tau_5} \tag{9.63c}$$

Next, two equations involving impedance-based transfer functions are taken up, which shall be realized using the inverting integrators shown in Figure 9.26(a) without R_f.

$$\left(-v_2\right) = -\frac{1}{sC_2R'}\left\{v_{I1} + \left(-v_{I3}\right)\right\} = -\frac{v_{I1} + (-v_{I3})}{s\tau_2} \tag{9.64a}$$

$$v_4 = -\frac{1}{sC_4R'}\left\{v_{I1} + \left(-v_{I3}\right)\right\} = -\frac{v_{I1} + (-v_{I3})}{s\tau_4} \tag{9.64b}$$

The last factor corresponds to equation (9.56), which will be realized using an inverting integrator.

$$\left(-v_6\right) = -\frac{1}{G_LR' + sC_6R'}\left\{v_{I5}\right\} = -v_{I5}/\{(1/r'L) + sC_6R'\} \tag{9.65a}$$

whereas, if C_6 is absent, it becomes a fifth-order LP filter. Then, the last factor corresponding to equation (9.56) will be realized using an inverter as:

$$\left(-v_6\right) = -\frac{1}{G_LR'}\left\{v_{I5}\right\} = -v_{I5}(r_L') \tag{9.65b}$$

Combining the results of the aforementioned equations, the realized circuit for the fifth-order LP active filter through operational simulation is given in Figure 9.27. In this realization, three non-inverting, two inverting integrators and one inverter will be used; hence, a total of nine OAs were needed. If the block forms of Figure 9.23 or 9.24 are used, it will require three inverting and two non-inverting integrators and an inverter, which would need a total of eight OAs.

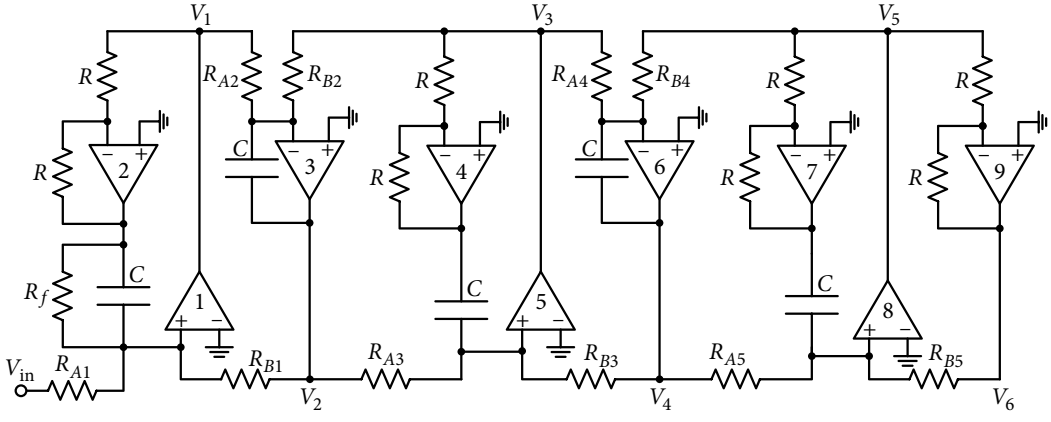


Figure 9.27 Realization of the fifth-order low pass ladder through operational simulation employing integrators of Figure 9.26.

https://doi.org/10.1017/9781108762632.010 Published online by Cambridge University Press

In brief, operational simulation of an LPF can be completed in the following steps.

i. After choosing an approximation method, a lossless LC ladder along with its element values and terminating resistances is obtained.

ii. All the branch elements are scaled by a resistor to convert the immittances to transfer functions.

iii. Either of the signal flow diagrams of Figure 9.22 or 9.24 can be selected; generally, the block diagram requiring lesser number of non-inverting integrators is chosen as it saves one OA.

iv. Blocks of integrating transfer functions are then replaced by active integrators, with each block having an independent impedance scaling factor for additional flexibility in selecting element values suitable for IC fabrication.

The following example will illustrate the procedure.

Example 9.5: For the given specifications, it was calculated that a fifth-order LP Chebyshev filter with pass band ripples of 0.5 dB will be suitable. Find an active filter using the operational simulation method which will have an LP cut-off frequency of ω_o = 10^5 rad/s and a source resistance of 1 kΩ.

Solution: Figure 9.28 shows the structure and element values for a passive LP fifth-order Chebyshev filter having 0.5 dB ripples. The normalized element values, with cut-off frequency ω_o = 1 rad/s and normalized input terminating resistance R_{in} = 1 Ω are as follows:

$L_1 = L_5 = 1.7058$ H, $C_2 = C_4 = 1.2296$ F, $L_3 = 2.5408$ H and $R_L = 1$ Ω

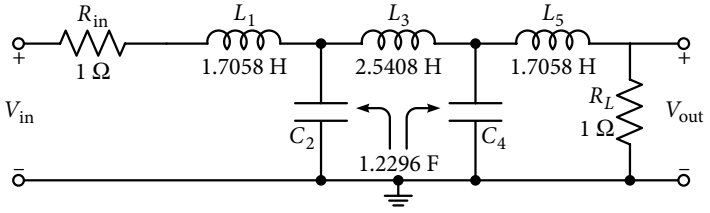


Figure 9.28 Fifth-order low pass filter with normalized element values having 0.5 dB ripples in the pass band.

Equations (9.51) to (9.56) can be written for these element values, wherein R' is the scaling resistance:

$$h_{Y1} = 1/\left(\frac{1.7058s}{R'} + \frac{1}{R'}\right), \quad -h_{Z2} = -1/1.2296sR' \tag{9.66a, b}$$

$$h_{Y3} = 1/(2.5408s/R'), -h_{Z4} = -1/1.2296sR' \tag{9.67a, b}$$

$$h_{Y5} = 1/(1.7058s/R'), -h_{Z6} = -1/R' \tag{9.68a, b}$$

https://doi.org/10.1017/9781108762632.010 Published online by Cambridge University Press

Transfer functions of the equations (9.66)–(9.68) are now compared with equations (9.63)–(9.65) and depending upon which transfer function is to be realized with an inverting or a non-inverting integrator or an inverter (or buffer), element values for each circuit will be obtained.

For the first transfer function h_{Y1} from equations (9.63a) and (9.66a):

$$v_{I1} = \frac{1}{\left(1.7058s / R'\right) + (1 / R')}\left\{v_s + \left(-v_2\right)\right\} \tag{9.69}$$

When it is compared with equation (9.61), it gives the following relation for a non-inverting integrator:

$$v_{I1} = \frac{1}{(sCR_s + G_{f1}R_s)}\left\{\frac{R_s}{R_A}v_s + \frac{R_s}{R_B}(-v_2)\right\} \tag{9.70}$$

Since in the block diagram of Figure 9.21, v_s and $(-v_2)$ are added with equal weightage, the selection can be made such that $R_A = R_B = R_s$. Comparison of equations (9.69) and (9.70) gives:

$$1/(1.7058s/R') + (1/R') = 1/(sCR_s + G_{f1}\,R_s) \tag{9.71}$$

Individual terms on the right-hand side of equation (9.71) are compared with respective terms on the left-hand, and application of the block impedance scaling factor R_1 and the frequency normalization factor ω_o results in:

$$CR_s = \frac{1.7058(R_1 / \omega_o)}{R'} \text{ and } \frac{R_s}{R_{f1}} = \frac{R_1}{R'} \tag{9.72}$$

In equation (9.72), there are two scaling factors, R' and R_1 which give enough flexibility in selecting practical values for the passive components. Selecting the value for capacitor C = 1 nF, and R_1 = 2.5 kΩ, equation (9.72) gives:

$$R_s R' = \frac{1.7058(R_1 / \omega_0)}{C} = \frac{1.7058 \times 2.5\,\text{k}\Omega}{1 \times 10^{-9} \times 10^5} = 42.645 \times 10^6\,\Omega^2$$

$$R_{f1} = \frac{R_s R'}{R_1} = \frac{42.645 \times 10^6}{2.5 \times 10^3} = 17.058\,\text{k}\Omega$$

If we select R_s = 5 kΩ = R_{A1} = R_{B1}, the aforementioned equations give R' = 8.529 kΩ and with this, all the components of the non-inverting integrator have been obtained.

For the next integrator, which is inverting and ideal, equation (9.64a) will be used.

$$\left(-v_2\right) = -\frac{1}{1.2296sR'}\left\{v_{I1} + \left(-v_{I3}\right)\right\} \tag{9.73a}$$

https://doi.org/10.1017/9781108762632.010 Published online by Cambridge University Press

Equation (9.73a) is compared with equation (9.59) (with $G_f = 0$).

$$\left(-V_2\right) = -\frac{1}{sCR_s}\left\{\frac{R_s}{R_A}V_{I1} + \frac{R_s}{R_B}\left(-V_{I3}\right)\right\} \tag{9.73b}$$

Since the scale factor of the two summing voltages V_{I1} and $-V_{I3}$ is unity, we select $R_s = R_A = R_B$. Then, the same impedance scaling and frequency de-normalization used in the first case is applied, which gives:

$$CR_s = 1.2296\, R'/R_1\omega_o$$

For a selected value of $C = 1$ nF as before:

$$\frac{R_s}{R'} = \frac{1.2296}{R_1 C\,\omega_o} = \frac{1.2296}{2.5\times10^3 \times 1\text{nF} \times 10^5} = 4.9184$$

It is important to note that since all integrators are independent of each other, the active scaling factor R_s in each case may be different, whereas the rest of the ladder will be scaled by the same factor $R' = 8.529$ kΩ which was obtained while designing the first integrator.

Hence, for the inverting integrator $R_s = R_{A2} = R_{B2} = (4.918 \times 8.529) = 41.94$ kΩ.

For the third integrator, from equation (9.63b):

$$\left(-v_{I3}\right) = \frac{1}{2.5408s / R'}\{\left(-v_2\right) + v_4\}.$$

Comparing this with equation (9.61), with $G_f = 0$:

$$\left(V_{I3}\right) = \frac{1}{sCR_s}\left\{\frac{R_s}{R_A}\left(-V_2\right) + \frac{R_s}{R_B}V_4\right\} \tag{9.74}$$

This provides the following relation after impedance and frequency scaling:

$$CR_s = \frac{2.5408(R_1/\omega_o)}{R'}$$

If C is selected as 1 nF, $R_s = \dfrac{2.5408\times2.5\times10^3}{8.529\times10^3\times10^5\times10^{-9}} = 7.447\,\text{k}\Omega$.

Hence, having unity gain for $(-V_2)$ and (V_4), $R_s = R_{A3} = R_{B3} = 7.447$ kΩ.

For the fourth integrator from equation (9.64a), selecting the value of $C_2 = C_4$, the inverting integrator will be exactly the same as the second inverter.

For the fifth integrator, which is non-inverting, from equation (9.63c) $L_5 = 1.7058$ H, the same as L_1; hence, its circuit realization will be the same as that of the first non-inverting integrator; with R_f open since it needs a lossless integrator.

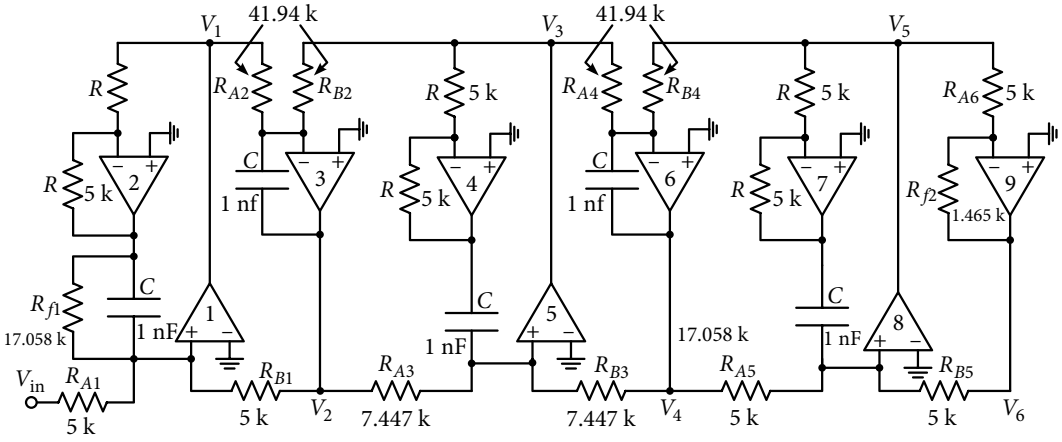
https://doi.org/10.1017/9781108762632.010 Published online by Cambridge University Press

The last unit being an inverter, equation (9.61) reduces to the following:

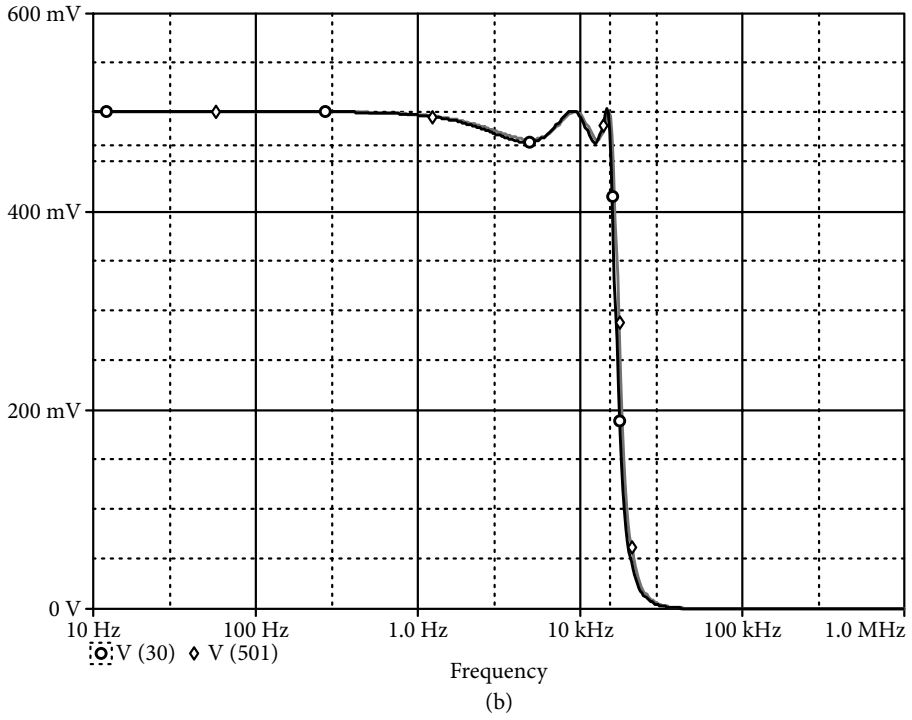
$$\left(-v_6\right) = -\frac{1}{G_{f2}R_s}\left\{\frac{R_s}{R_A}\left(v_{I5}\right)\right\} \tag{9.75}$$

Using equations (9.65b) and comparing $-v_6 = -\frac{R_1}{R'}(v_{I5})$ with equation (9.75):

For R_{A6} = 5 kΩ, $R_L = R_{\text{in}}$ = 2.5 kΩ, R_{f2} = 5 k × 2.5 k/8.529 k = 1.465 kΩ



(a)



(b)

Figure 9.29 (a) Circuit realization for the low pass filter of Example 9.5. (b) Frequency response of the operationally simulated filter shown in Figure 9.29(a) and the passive filter shown in Figure 9.28.

https://doi.org/10.1017/9781108762632.010 Published online by Cambridge University Press

Figure 9.27 is redrawn as Figure 9.29(a) with all calculated element values and Figure 9.29(b) shows the simulated magnitude response of the operationally simulated filter. Its corner frequency is 15.6 kHz (98.05 krad/s), voltage gain is 0.4998 and the ripple width is 0.555dB. At 200.8 krad/s (31.953 kHz), attenuation is 43.8 dBs. For comparison sake, the passive filter shown in Figure 9.28 was also simulated and its response is also shown in Figure 9.29(b). Its corner frequency is 15.902 kHz (99.95 krad/s), ripple width is 0.5061 dB and an attenuation of 42.53 dBs is at 31.888 kHz (200.4 krad/s). It can be easily observed that the operationally simulated response almost overlaps the passive response except that the ripple width is slightly more.

9.11 Operational Simulation of the Band Pass Ladder

In many cases, a BPF is designed using an initial design of a prototype LPF and then transforming it as discussed in Section 5.4 of Chapter 5. The effect of such a transformation is that the lossless inductance and capacitances get converted as series LC and parallel LC branches, respectively. Figure 9.30(a) shows a simple LP ladder and its converted BP form in Figure 9.30(b); the series resistor with the inductor gets converted into an RLC branch whose impedance is given as:

$$Z_1 = (R_{in} + SL_1) \rightarrow R_{in} + L_1 Q(s + 1/s) = R_{in} + sQL_1 + L_1\, Q/s$$

$$= R_{in} + sL_{1BP} + 1/sC_{1BP} \tag{9.76}$$

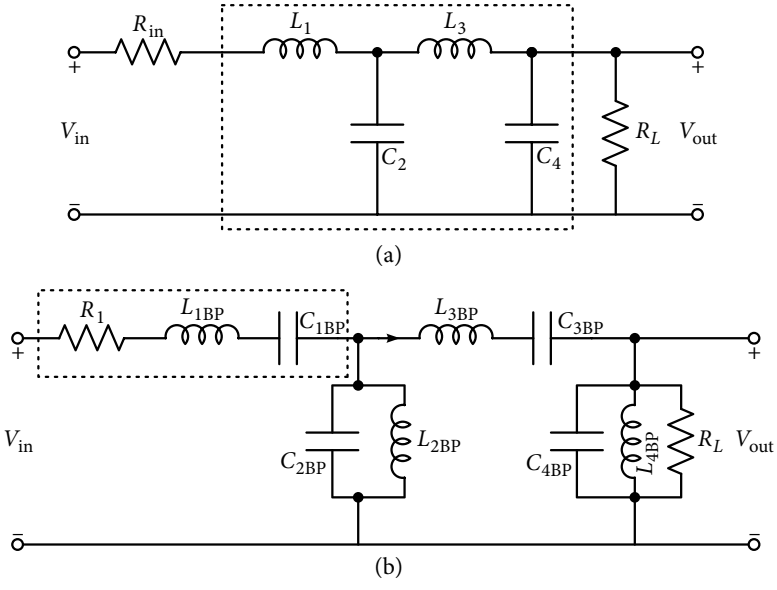


Figure 9.30 (a) Doubly terminated fourth-order lossless low pass ladder and (b) the band pass ladder obtained from (a) through low pass to band pass transformation.

https://doi.org/10.1017/9781108762632.010 Published online by Cambridge University Press

The lossy capacitance at the output end gets converted into a shunt RLC branch having admittance as:

$$Y_4 = G_L + SC_4 \rightarrow G_L + C_4Q(s + 1/s) = G_L + sC_4Q + C_4Q/s$$

$$= G_L + sC_{4BP} + 1/sL_{4BP} \tag{9.77}$$

whereas the lossless branches have been shown to be, respectively:

$$Y_2 = sC_{2BP} + 1/sL_{2BP} \text{ and } Z_3 = sL_{3BP} + 1/sC_{3BP} \tag{9.78}$$

In equations (9.76) and (9.77), elements of the normalized BP section are:

$$L_{1BP} = QL_1,\ C_{1BP} = 1/QL_1,\ L_{4BP} = 1/QC_4, \text{ and } C_{4BP} = QC_4 \tag{9.79}$$

Admittance of the series arm of equation (9.76) and the impedance of the shunt arm of equation (9.77) can be written as:

$$Y_{1BP} = \frac{(1/L_{1BP})s}{s^2 + (R_{in}/L_{1BP})s + 1/(L_{1BP}C_{1BP})} \tag{9.80}$$

$$Z_{4BP} = \frac{(1/C_{4BP})s}{s^2 + (G_L/C_{4BP})s + (1/L_{4BP}C_{4BP})} \tag{9.81}$$

For the operational simulation of the BPF shown in Figure 9.30(b) in the form of the block diagram shown in Figure 9.23 or 9.24, equations (9.80) and (9.81) are scaled by R', in order to convert them into the form of the following voltage ratio transfer functions

$$-Y_{1BP}R' = -h_{Y1}(s) = -\frac{(R'/L_{1BP})s}{s^2 + (R_{in}/L_{1BP})s + 1/(L_{1BP}C_{1BP})} \tag{9.82}$$

$$Z_{4BP}G' = h_{Z4}(s) = \frac{(G'/C_{4BP})s}{s^2 + (G_L/C_{4BP})s + (1/L_{4BP}C_{4BP})} \tag{9.83}$$

Expressions in equations (9.82) and (9.83) represent inverting and non-inverting BP functions with a finite value of pole-Q.

For the internal branches, which do not contain resistors, scaling by the resistor R' gives the respective transfer functions shown here, which are inverting and non-inverting BP functions with infinite pole-Q.

$$\frac{Z_{2BP}(s)}{R'} = h_{Z2}(s) = \frac{(G'/C_{2BP})s}{(s^2 + 1/L_{2BP}C_{2BP})} \tag{9.84}$$

https://doi.org/10.1017/9781108762632.010 Published online by Cambridge University Press

$$-Y_{3BP}R' = -h_{Y3}(s) = -\frac{\left(R' / L_{3BP}\right)s}{(s^2 + 1/L_{3BP}C_{3BP})} \tag{9.85}$$

It is obvious from the aforementioned equations that a doubly terminated BPF obtained from an LPF through frequency transformation can be realized using only second-order filter sections which are able to realize finite as well as infinite Q. Such filter sections should be capable of adding two inputs, and these will be connected alternately inverting and non-inverting form; in exactly the same way as in the LPF case.

There are a number of active circuits for the realization of second-order BP functions employing one or more than one active device. Obviously, the advantages and limitations of the applied second-order section will be reflected in the overall functioning of the operationally simulated realization. Use of one OA BPF section will be economical but usually such realizations have high sensitivities, whereas multi amplifier sections may not be economical but are less sensitive. The following example will help in understanding the procedure for operationally simulating a BPF.

Example 9.6: A doubly terminated LP Butterworth approximated filter structure is shown in Figure 9.31. Using frequency transformation, convert the filter to a BPF having center frequency $\omega_o = 10^4$ rad/s, and $Q = 5$. Find a suitable active realization using the operational simulation method.

Solution: From equation (9.79), normalized value of the elements of the BPF are:

$$L_{1BP} = 5 \times 0.7645 = 3.8225 \text{ H}, \; C_{1BP} = 1/5 \times 0.7645 = 0.2616 \text{ F}$$

$$L_{2BP} = 1/5 \times 1.848 = 0.1082 \text{ H}, \; C_{2BP} = 5 \times 1.848 = 9.24 \text{ F}$$

$$L_{3BP} = 5 \times 1.848 = 9.24 \text{ H}, \; C_{3BP} = 1/5 \times 1.848 = 0.1082 \text{ F}$$

$$L_{4BP} = 1/5 \times 0.7645 = 0.2616 \text{ H}, \; C_{4BP} = 5 \times 0.7645 = 3.8225 \text{ F} \tag{9.86}$$

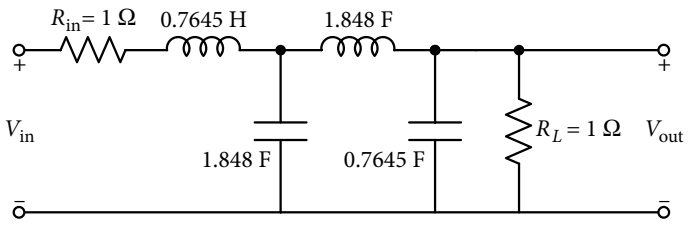


Figure 9.31 Fourth-order Butterworth filter structure with normalized elements values for Example 9.6.

After frequency normalization by $\omega_o = 10^4$ rad/s and impedance normalization by a factor of 10^3, element values become:

https://doi.org/10.1017/9781108762632.010 Published online by Cambridge University Press

$$R_{in} = 1\ \text{k}\Omega,\ L_{1BP} = 382.25\ \text{mH},\ C_{1BP} = 26.16\ \text{nF} \tag{9.87}$$

$$L_{2BP} = 10.82\ \text{mH},\ C_{2BP} = 924\ \text{nF} \tag{9.88}$$

$$L_{3BP} = 924\ \text{mH},\ C_{3BP} = 10.82\ \text{nF} \tag{9.89}$$

$$L_{4BP} = 26.16\ \text{mH},\ C_{4BP} = 382.25\ \text{nF},\ R_L = 1\ \text{k}\Omega \tag{9.90}$$

Figure 9.32 shows the transformed passive eighth-order BPF structure with de-normalized element values.

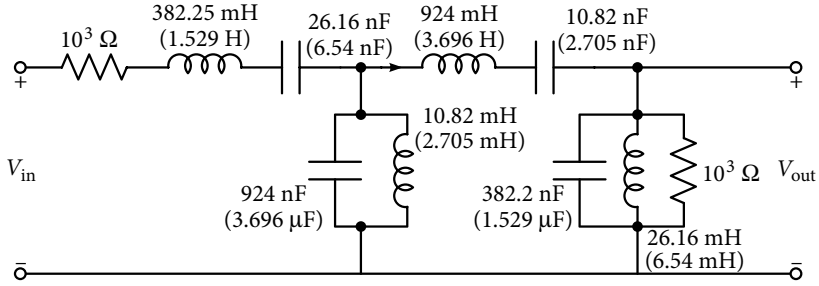


Figure 9.32 Eighth-order band pass filter with de-normalized element values from Figure 9.31 for Example 9.6.

Series and shunt branches comprising the elements in equations (9.87) and (9.90), respectively, are written like equations (9.80) and (9.81), and scaled by $R'(\text{k}\Omega)$ in order to be represented by transfer functions of equations (9.82) and (9.83). The resulting equations will be as follows:

$$-h_{y1}(s) = -\frac{\left(R'/0.38225\right)s}{s^2 + \left(10^3/0.38225\right)s + (0.38225\times 26.16\times 10^{-9})} \tag{9.91}$$

$$h_{z4}(s) = \frac{\left(G'/0.38225\times 10^{-6}\right)s}{s^2 + \left(10^{-3}/0.38225\times 10^{-6}\right)s + (0.02616 * 0.38225\times 10^{-6})} \tag{9.92}$$

Taking the same steps, equations (9.88) and (9.89) will transform into the following equations:

$$h_{z2}(s) = \frac{\left(G'/924\times 10^{-12}\right)s}{s^2 + 1/\left(0.1082\times 924\times 10^{-12}\right)} \tag{9.93}$$

$$h_{y3}(s) = \frac{\left(R'/0.924\right)s}{s^2 + 1/\left(0.924\times 10.82\times 10^{-12}\right)} \tag{9.94}$$

https://doi.org/10.1017/9781108762632.010 Published online by Cambridge University Press

There are some choices available for the realization of the four transfer functions, equations (9.91)–(9.94). Separate configurations can be chosen for the inverting and non-inverting second-order BP sections, with finite and infinite Q. In the present example, a modified Tow–Thomas biquad with two inputs as shown in Figure 9.33 is used. The important feature of the modified circuit is that both inverting and non-inverting BP responses are available at the OA outputs and infinite Q is obtained simply by open circuiting the resistor R^*. Therefore, the design of all the four transfer functions becomes modular; an attractive feature for integration. Assuming ideal OAs, analysis of the circuit of Figure 9.33 gives its transfer function as:

$$V_{\text{BP}} = \left(\frac{V_A}{R_A} + \frac{V_B}{R_B}\right) \frac{(1/C_1)s}{s^2 + (1/C_1R^*)s + (1/C_1C_2R_1R_2)} \tag{9.95}$$

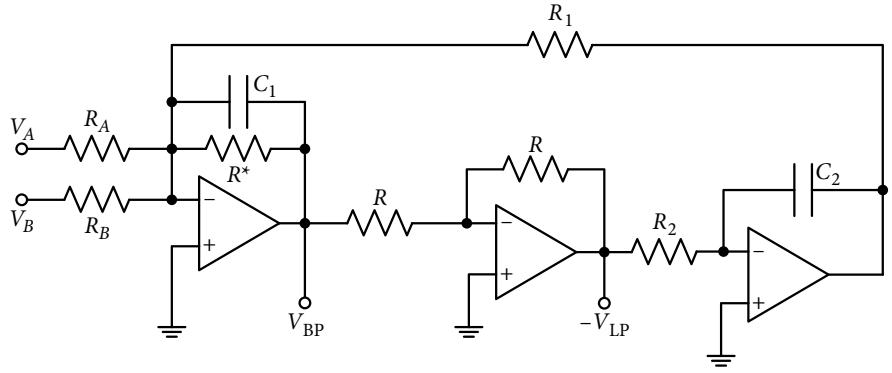


Figure 9.33 Modified Tow–Thomas biquad with two inputs.

From equation (9.95), parameters are

$$\omega_o = 1/(C_1\, C_2\, R_1\, R_2)^{0.5} \tag{9.96}$$

$$\frac{\omega_o}{Q} = \frac{1}{C_1R^*} \rightarrow Q = R^* \sqrt{\left(\frac{1}{R_1R_2}\frac{C_1}{C_2}\right)} \tag{9.97}$$

Normally, $C_1 = C_2 = C$, then the parameters are:

$$\omega_o = 1/C(R_1R_2)^{½} \text{ and } Q_{\text{BP}} = R^* \sqrt{\left(\frac{1}{R_1R_2}\right)} \tag{9.98}$$

To get infinite Q_{BP}, R^* is made open, which does not affect the expression for ω_o. Without affecting generality, $R_1 = R_2 = R$, and as the two voltages V_A and V_B is to be added with equal weightage, we select $R_A = R_B$. In the finite Q case, the simplified form of equation (9.95) becomes:

$$V_{\text{BP}} = \frac{(V_A + V_B)(1/CR_A)s}{s^2 + (1/CR^*)s + 1/(CR)^2} \tag{9.99}$$

https://doi.org/10.1017/9781108762632.010 Published online by Cambridge University Press

Selecting $C = 10^{-7}$ F, in all the four branches, from equation (9.98), it gives:

$$R = 1/10^4 \times 10^{-7} = 1\ \text{k}\Omega \tag{9.100}$$

For evaluation of the rest of the elements of branch 1, comparing the parameters of equation (9.99) with equation (9.82), we get:

$$\frac{1}{CR^*} = \frac{R_{\text{in}}}{L_{1\text{BP}}} \text{ and } \frac{R'}{L_{1\text{BP}}} = \frac{1}{CR_A} \tag{9.101}$$

$$R^* = L_{1\text{BP}}/CR_{\text{in}} = 0.38225/10^{-7} \times 10^3 = 3.8225\ \text{k}\Omega \tag{9.102}$$

With $R' = 1\ \text{k}\Omega$, we get from equation (9.101):

$$R_{A1} = L_{1\text{BP}}/CR' = 3.8225\ \text{k}\Omega = R_{B1} \tag{9.103}$$

In equation (9.103), subscript 1 indicates elements for the first branch for which all elements have been calculated. For shunt arm 2, equation (9.99) (with R^* open) is compared with equation (9.84). It gives:

$$R_{A2} = \text{C}_{2\text{BP}}/G'\ C = 9.24\ \text{k}\Omega = R_{B2} \tag{9.104}$$

For the third (series) branch, R^* is open and comparison between equations (9.99) and (9.85) gives:

$$R_{A3} = L_{3\text{BP}}/CR' = 9.24\ \text{k}\Omega = R_{B3} \tag{9.105}$$

For the fourth (shunt) arm, comparison between equations (9.99) and (9.83), we get:

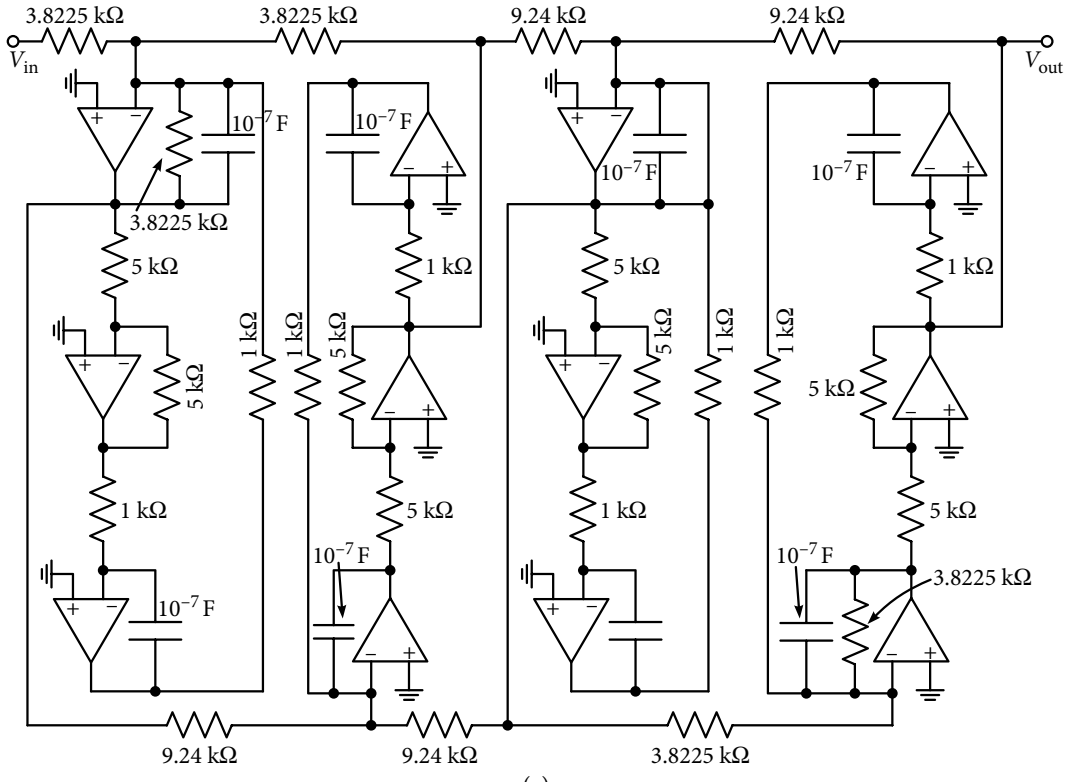
$$R^* = 3.8225\ \text{k}\Omega,\ R_{A4} = 3.8225\ \text{k}\Omega \tag{9.106}$$

Figure 9.34(a) shows the operationally simulated eighth-order BPF. Care is taken to keep alternate inverting and non-inverting blocks.

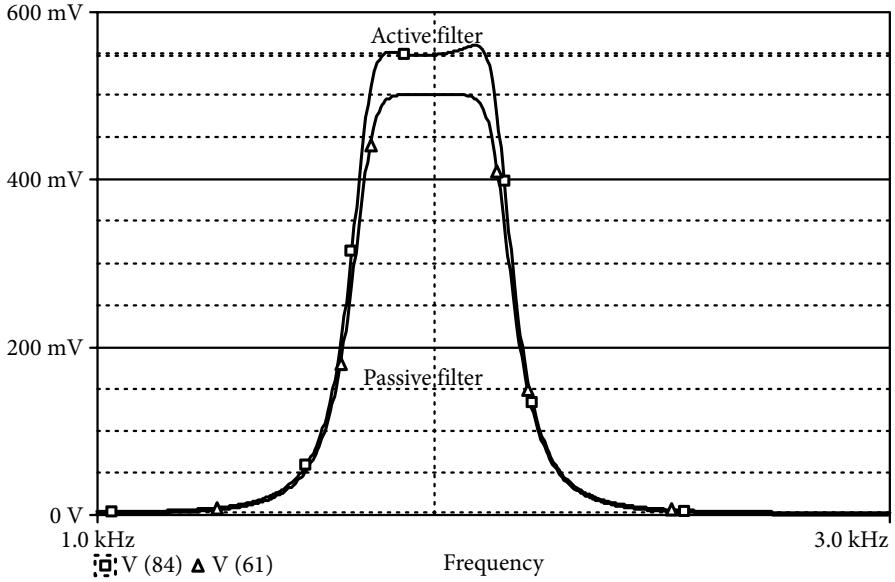
Figure 9.34(b) shows the simulated response of the active filter of Figure 9.34(a), having a center frequency of 1.5969 kHz (10.037 krad/s) with a mid-band gain of 0.547, instead of 0.5. With a bandwidth of 320.8 Hz, obtained $Q = 4.977$. It is observed that the pass band is also flat as it should be. Figure 9.34(b) also shows the simulated response at the same center frequency, with $Q = 5$, for the passive structure. With the mid-band gain as 0.5, the pass band is still flatter with $Q = 5.02$.

Figure 9.34(c) shows the simulated response at the same center frequency with $Q = 20$, for the operationally simulated as well as passive structure. De-normalized element values for the filter with $Q = 20$ are also shown in Figure 9.34(a) within brackets. The response is not flat and the mid-band gain is also increased to 0.713 instead of 0.5. The realized value of $Q = 19.6$.

https://doi.org/10.1017/9781108762632.010 Published online by Cambridge University Press



(a)



(b)

https://doi.org/10.1017/9781108762632.010 Published online by Cambridge University Press

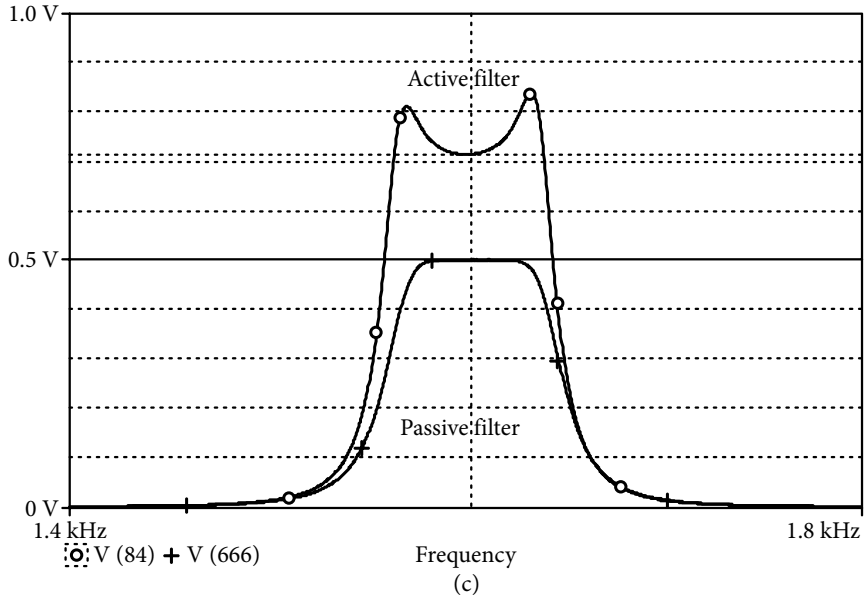


Figure 9.34 (a) Operationally simulated eight-order band pass filter for Example 9.6. (b) Simulated response of the filter with $Q = 5$, and passive filter (c) Response of the operationally simulated eighth-order band pass filter with $Q = 20$.

9.12 General Ladder Realization

LP and BP lossless ladders are very important from the point of view of filter design. From the discussion so far, it can be observed that the procedure for their realization through operation simulation is a bit long but follows a set pattern. Of course, the design depends on the kind of structure used for realizing a particular second-order transfer function for the inverting or non-inverting mode branch. However, there are many ladder configurations other than an all pole LP and BP in which the branches (series or shunt) are in a most general form. A branch can comprise inductors and capacitors in both series and parallel form and resistors as well. Figures 9.35(a) and (b) show one such general structure each in series and parallel form. Herein, in Figure 9.35(a), subscript s indicates an element in the series branch and in Figure 9.35(b), p indicates parallel (or shunt) branch elements. While operationally simulating, the series branches are expressed in admittance form and the shunt branch in impedance form, and both are scaled by the same value resistance R'. Following the same procedure and expressing them in continued expansion form, first for the series branch, we get the following expression.

$$R'Y(s) = \cfrac{1}{\cfrac{R_{s1}}{R'} + \cfrac{L_{s1}}{R'}s + \cfrac{1}{sC_{s1}R'} + \cfrac{1}{sC_{s2}R' + \cfrac{1}{\cfrac{L_{s2}}{R'}s}}} \tag{9.107}$$

https://doi.org/10.1017/9781108762632.010 Published online by Cambridge University Press

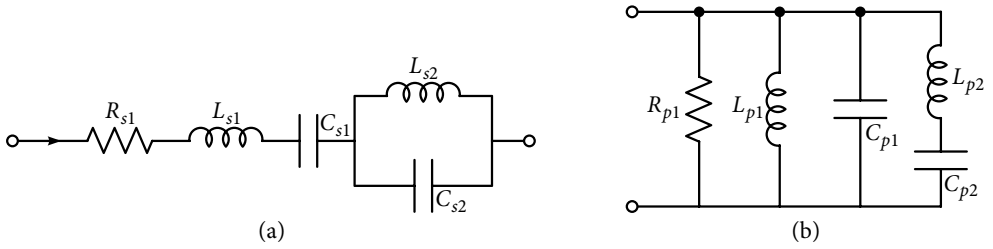


Figure 9.35 (a) Series and (b) shunt branch of a ladder with arbitrary combination of elements.

Since $R'Y(s)$ can be written as $h_Y(s)$ and the scaled elements can be written in lower case symbols, equation (9.107) modifies as:

$$h_Y(s) = \frac{1}{r_{s1} + sl_{s1} + \frac{1}{sC_{s1}} + \frac{1}{sC_{s2} + \frac{1}{sl_{s2}}}} \tag{9.108}$$

Similarly, for the shunt branch, the impedance function divided by R' and the resultant transfer function with negative sign are:

$$-\frac{Z(s)}{R'} = -\frac{1}{R'G_{p1} + sC_{p1}R' + \frac{1}{s\frac{L_{p1}}{R'}} + \frac{1}{s\frac{L_{p2}}{R'} + \frac{1}{sC_{p2}R'}}} \tag{9.109}$$

Since $Z(s)/R'$ can be written as $h_Z(s)$ and the scaled elements can be written in lower case symbols, equation (9.109) modifies as:

$$-h_Z(s) = -\frac{1}{g_{p1} + sc_{p1} + \frac{1}{sl_{p1}} + \frac{1}{sl_{p2} + \frac{1}{sc_{p2}}}} \tag{9.110}$$

Note that series branches result in a current, like $I_1 = Y_1\{V_s + (-V_2)\}$ in Figure 9.19, which gets converted to a voltage after resistance scaling, and the shunt branches result in voltages like $V_2 = Z_2\,(I_1 - I_3)$; scaled as well.

A suggested approach for the realization of the kind of transfer function of equations (9.108) and (9.110) uses a two-input summing inverter with an arbitrary transfer function $H(s) = (V_i/V_{\text{out}})$ and admittance $Y(s)$ in its feedback path as shown in Figure 9.36(a) and (b). Assuming OA as ideal, a simple analysis of Figure 9.36(a) shows that:

$$V_{\text{out}} = -\frac{1}{Y(s)H(s)}\left(V_A G_A + V_B G_B\right) = -\frac{G'}{Y(s)H(s)}\left\{\frac{G_A}{G'}V_A + \frac{G_B}{G;}V_B\right\} \tag{9.111}$$

https://doi.org/10.1017/9781108762632.010 Published online by Cambridge University Press

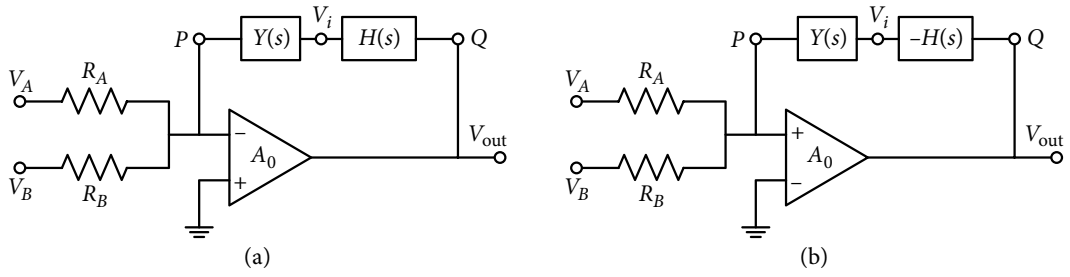


Figure 9.36 (a) A schematic realizing the transfer function for equation (9.111), with $H(s) = (V_i/V_{out})$ and (b) its dual for realization of the inverting transfer function.

Equation (9.111) shows the summation of two input voltages resulting in a voltage ratio transfer function which is inverting and proportional to the inverse of $Y(s) \times H(s)$, with $R' = 1/G'$ as the scaling resistor. Obviously, this arrangement is valid for the inverting transfer function blocks in operational simulation as represented by equation (9.110). In a dual scheme, shown in Figure 9.36(b), with two voltages connected to the non-inverting input of the OA and the inverting terminal grounded, and with transfer function $(-H(s))$, exactly the same output as in equation (9.111) results in a *non-inverting transfer function*, which is used for the non-inverting blocks in operational simulation as represented by equation (9.108). It is to be noted that, in each version, with the help of negative feedback, one inverting and one non-inverting combination of OA and $H(s)$ is maintained for the stability of the arrangement.

As mentioned earlier, $H(s)$ is an arbitrary function in s; hence, one can realize not only the transfer function of equation (9.108) and (9.110), but anything simpler or more complex than that. Presently, we will limit our discussion to the circuit realization of Figure 9.35, but it can be extended to other circuits or simplified to the LP and BP circuits, which are nothing but special simpler cases of the circuit in Figure 9.35.

9.12.1 Realization of shunt arm

To realize the inverting transfer function of equation (9.110), four feedback branches need to be connected between terminals P and Q of the circuit in Figure 9.36(a) corresponding to each branch of the circuit in Figure 9.35(b). For the realization of single elements, R_{p1}, L_{p1} and C_{p1}, the structures shown in Figure 9.37(a) will be connected between terminals P and Q, whereas, for realizing the parallel combination of L_{p2} and C_{p2}, the circuit shown in Figure 9.37(b) will be connected between terminals P and Q. Assuming both OAs as ideal, a routine analysis gives the following relations in Figures 9.37(a) and (b), respectively.

$$V_{c0} = H_0\, V_{out},\ V_{c1} = H_1\, V_{out} \text{ and } V_{c2} = H_2\, V_{out} \tag{9.112}$$

$$G_{31}\, V_{out} + \{Y_3\,(-H_3) + Y_4\,(-H_4)\}\, V_{c3} = 0 \text{ or } V_{c3} = G_{31}\, V_{out}/(Y_3\, H_3 + Y_4\, H_4) \tag{9.113}$$

https://doi.org/10.1017/9781108762632.010 Published online by Cambridge University Press

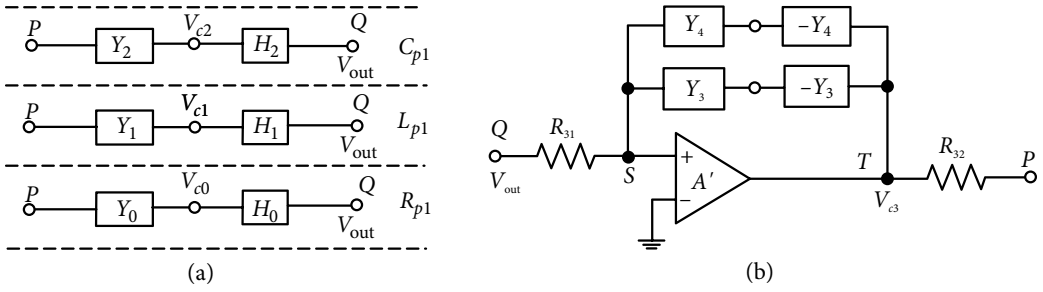


Figure 9.37 Expanded configuration for realizing (a) R_{p1}, L_{p1} and C_{p1} and (b) L_{p2} and C_{p2} of a ladder like that shown in Figure 9.35(b).

Substitution of Figures 9.37(a), (b) in Figure 9.36(a), yields the following relation:

$$G_A V_A + G_B V_B + V_{c0} Y_0 + V_{c1} Y_1 + V_{c2} Y_2 + V_{c3} G_{32} = 0 \tag{9.114}$$

Substituting V_{c0}, V_{c1}, V_{c2} and V_{c3} from equations (9.112) and (9.113) in equation (9.114) and scaling by resistor R'', the following output voltage is obtained.

$$V_{\text{out}} = -\left\{\frac{R''}{R_A}V_A + \frac{R''}{R_B}V_B\right\} \frac{1}{Y_0 H_0 R'' + Y_1 H_1 R'' + Y_2 H_2 R'' + \dfrac{1}{\dfrac{Y_3 H_3}{G_{31} G_{32} R''} + \dfrac{Y_4 H_4}{G_{31} G_{32} R''}}} \tag{9.115}$$

Equation (9.115) shows the output voltage as a function of two voltages V_A and V_B, which are being added. If these voltages are to be added directly without any weightage, then R_A and R_B will be equal to R''. If the voltage levels are to be changed, which is sometimes required for changing the dynamic range of the filter section, then it is done by opting for a proper ratio between R'' and R_A and R_B. Components of the transfer function of equation (9.115) can be compared with the inverting transfer function of equation (9.110) and a procedure can be developed for finding the nature of the transfer function $H_i(s)$ and the value (expression) of elements to be used in it in terms of the elements of the circuit shown in Figure 9.35(b).

For the shunt arm of the ladder, to realize the element R_{p1}, we select $Y_0 = G_0$ and $H_0 = 1$, which means:

$$g_{p1} = Y_0 H_0 R'' \rightarrow G_{p1} R' = G_0 R'' \text{ or } R_0 = (R''/R') R_p = k_p R_p, \text{ where } k_p = R''/R' \tag{9.116}$$

For the realization of the capacitance C_{p1}, we select $Y_1 = sC_1$ and $H_1 = 1$, which results in:

$$sc_{p1} = Y_1 H_1 R'' \rightarrow sC_{p1} R' = sC_1 R'' \text{ or } C_1 = (R'/R'') C_{p1} = C_{p1}/k_p \tag{9.117}$$

It is better to fix the value of k_p from equation (9.117) and use equation (9.116) to get the value of R_0. If R_p is not present in the shunt branch of the original ladder, then R_0 shall be

https://doi.org/10.1017/9781108762632.010 Published online by Cambridge University Press

open circuited, and similarly, if C_{p1} is absent, C_1 shall will also be absent, and k_p can be selected using equation (9.116).

For the realization of inductor L_{p1}, we select $H_2 = (1/sC_2R_{21})$, a non-inverting integrator, and $Y_2 = G_{22}$, which means that:

$$\frac{1}{sl_{p1}} = Y_2 H_2 R'' \rightarrow \frac{1}{sL_{p1}/R'} = \frac{G_{22}}{sC_2R_{21}} R'' \rightarrow R_{21}R_{22} = \frac{L_{p1}}{C} k_p \text{ for } C_1 = C_2 = C \tag{9.118}$$

Circuit structure for the realization of R_{p1}, L_{p1} and C_{p1}, corresponding to equations (9.116), (9.117) and (9.118) are shown in Figure 9.38(a).

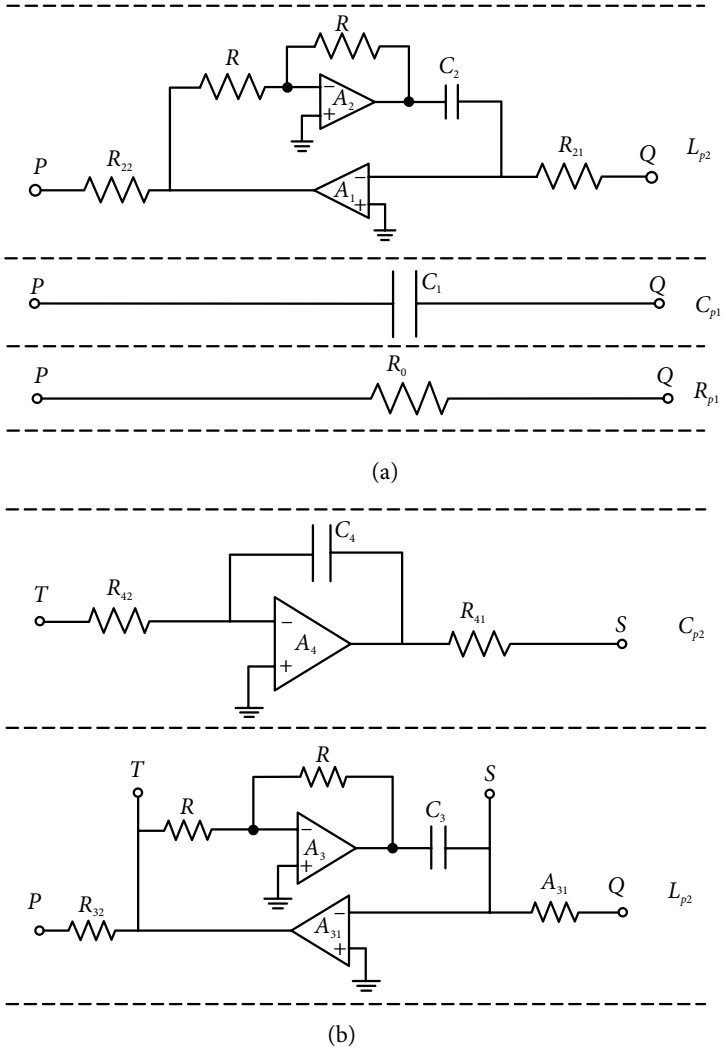


Figure 9.38 Circuit realization for (a) R_{p1}, L_{p1} and C_{p1} and (b) L_{p2} and C_{p2} of the shunt branch of a ladder like that shown in Figure 9.35(b).

https://doi.org/10.1017/9781108762632.010 Published online by Cambridge University Press

For the branch containing a series combination of L_{p2} and C_{p2}, first to find the relations for L_{p2}, we select $H_3 = 1$ and $Y_3 = sC_3$; this gives the following relations:

$$sl_{p2} = \frac{Y_3 H_3}{G_{31} G_{32} R''} \rightarrow s\frac{L_{p2}}{R'} = s\frac{C_3 R_{31} R_{32}}{R''} \rightarrow R_{31} R_{32} = \frac{L_{p2}}{C_3}\frac{R''}{R'} = \frac{L_{p2}}{C} k_p \text{ for } C_3 = C \quad (9.119)$$

For the realization of the capacitor C_{p2}, we select, $Y_4 = G_{41}$ and $H_4 = (1/sC_4R_{42})$ a non-inverting integrator, and we get:

$$\frac{1}{sc_{p2}} = \frac{Y_4 H_4}{G_{31} G_{32} R''} \rightarrow \frac{1}{sC_{p2}R'} = \frac{1}{s}\frac{G_{41} R_{31} R_{32}}{C_4 R_{42} R''}$$

Substituting for R_{31} R_{32} from equation (9.119), we get:

$$R_{41} R_{42} = \frac{C_{p2}}{C_4}\frac{R'}{R''} \times \frac{L_{p2}}{C} k_p = \frac{C_{p2} L_{p2}}{C^2} \text{ for } C_4 = C \quad (9.120)$$

The circuit structures for the realization of L_{p2} and C_{p2}, corresponding to equations (9.119) and (9.120) are shown in Figure 9.38(b), which are to be combined with Figure 9.37(a).

Equations (9.116) to (9.120) serve as the design equations for the structure and the element values. Once k_p is fixed, and $C_1 = C_2 = C_3 = C_4 = C$ are selected, the products $R_{21}R_{22}$, $R_{31}R_{32}$ and $R_{41}R_{42}$, are found out. There is no constraint and we can select:

$$R_{i1} = R_{i2} \quad (9.121)$$

The remaining input resistances R_A and R_B are decided depending on the voltage gain given to the two voltages V_A and V_B. For the usual case of summing the voltages directly,

$$R_A = R_B = R'' \quad (9.122)$$

9.12.2 Realization of series arm

Admittance of a series arm, which is shown in Figure 9.35(a), is converted to a transfer function of equations (9.107) and (9.108). Its non-inverting expression is realized by similar structures as of Figure 9.37, shown in Figure 9.39, where input voltages are applied at the non-inverting terminal of OA, A_0 of Figure 9.36(a); the rest of the inputs are given to the inverting terminal. Analysis results in exactly the same output voltage expression as in equation (9.115) without the inverting sign as desired.

Using the same procedure as was adopted for the shunt branch, the following selections were made for the elements R_{s1}, L_{s1} and C_{s1}.

$$H_0 = H_1 = -1, -H_2 = -\frac{1}{sC_2R_{21}} \quad (9.123a)$$

https://doi.org/10.1017/9781108762632.010 Published online by Cambridge University Press

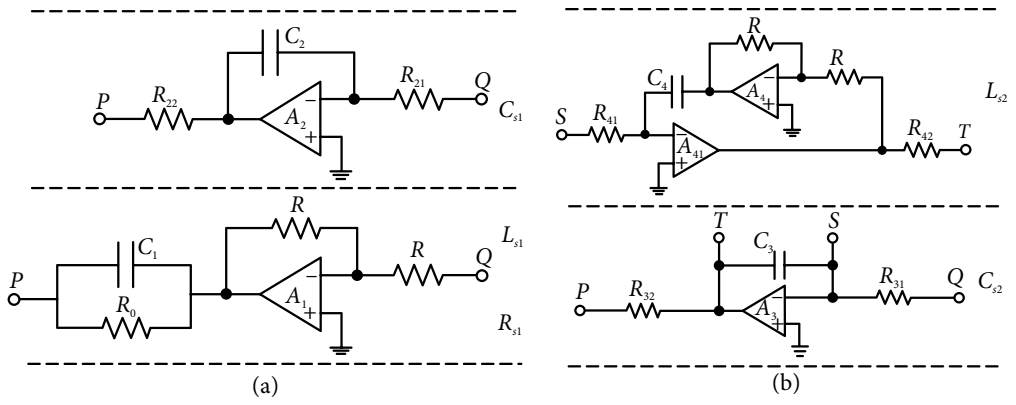


Figure 9.39 Circuit realization for (a) R_{S1}, L_{S1} and C_{S1} and (b) L_{S2} and C_{S2} of the series branch of a ladder like that of Figure 9.35(a).

Corresponding to equation (9.123a), the circuit structures to be connected between terminals P and Q of Figure 9.36(a) are shown in Figure 9.39(a). Selected components will be as:

$$Y_0 = G_0,\ Y_1 = sC_1,\ Y_2 = sC_2, \tag{9.123b}$$

The following selections were made for the elements L_{s2} and C_{s2}.

$$H_3 = 1,\ H_4 = \frac{1}{sC_4R_{41}} \tag{9.124a}$$

Corresponding to equation (9.124a), the circuit structures to be connected between terminals P and Q of Figure 9.36(b) are shown in Figure 9.39(b). Selected components will be as:

$$Y_3 = sC_3,\ Y_4 = G_4 \tag{9.124b}$$

Component values are obtained as:

$$Y_0H_0R'' = R_{s1} / R' \rightarrow R_0 = (R'R'') / R_{s1} = (k_s^2) / R_{s1} \tag{9.125a}$$

$$Y_1H_1R'' = sL_{s1} / R' \rightarrow C_1 = L_{s1} / \left(R'R''\right) = L_{s1} / k_s^2 \tag{9.125b}$$

As before, after selecting a suitable value of $C_1 = C$, k_s is fixed from equations (9.125b); then, R_0 is obtained from equation (9.125a) and the value of k_s remains constant in the next steps. In case L_{s1} is not present, then $C_1 = 0$ and the value of k_s shall will be decided by equation (9.125a).

With C_2, C_3 and C_4 chosen equal to $C(C_1)$, the remaining resistances are obtained from the following:

$$R_{21}R_{22} = \frac{C_{s1}}{C}k_s^2,\ R_{31}R_{32} = \frac{C_{s2}}{C}k_s^2,\ \ R_{41}R_{42} = \frac{L_{s2}}{C}\frac{R_{31}R_{32}}{k_s^2} = \frac{L_{s2}C_{s2}}{C^2} \tag{9.126}$$

https://doi.org/10.1017/9781108762632.010 Published online by Cambridge University Press

Once again without losing generality, we can select:

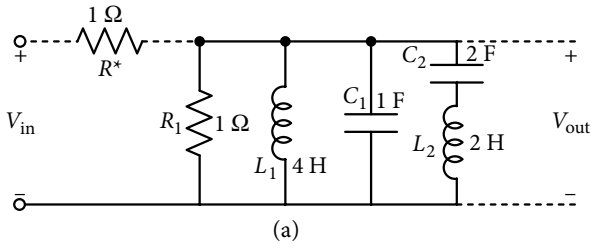
$$R_{i1} = R_{i2} = R_i \text{ and } R_{Ai} = R_{Bi} = R'' \text{ for unity gain.} \tag{9.127}$$

Example 9.7: Compare the responses of the passive circuit shown in Figure 9.40(a) and its active version as an illustration of the realization of shunt arm through operation simulation.

Solution: Impedance scaling factor R' of 1 kΩ and frequency scaling factor of 2 krad/s gives the element values as:

$$R_{p1} = 1 \text{ k}\Omega,\ L_{p1} = 0.2 \text{ H},\ C_{p1} = 0.05\ \mu\text{F},\ L_{p2} = 0.1 \text{ H and } C_{p2} = 0.1\ \mu\text{F} \tag{9.128}$$

Resistance $R^* = 1$ kΩ ($= R_{p1}$) has been connected in series to find the response in the passive case only.



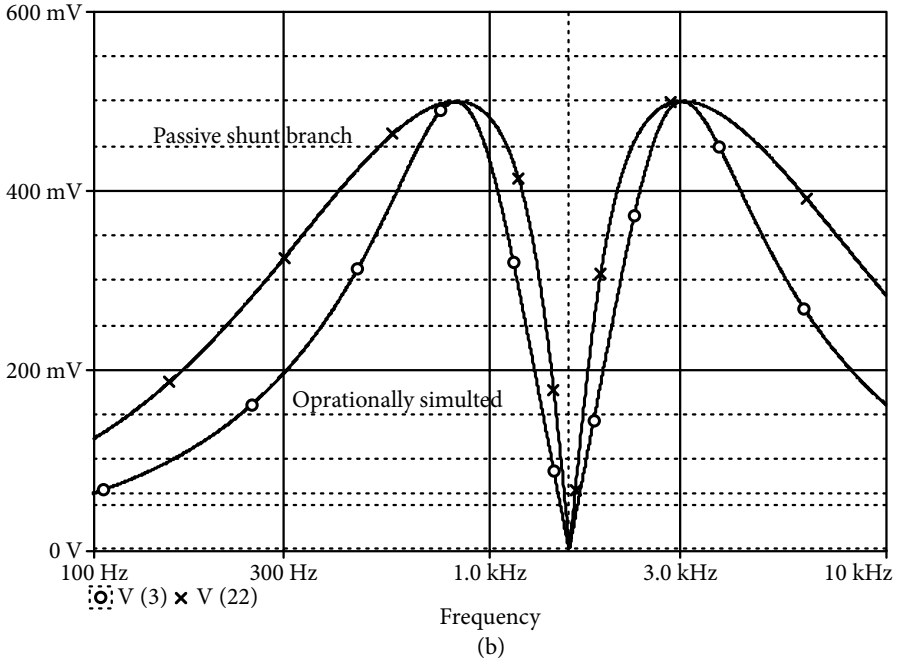


Figure 9.40 (a) Prototype normalized shunt arm for Example 9.7. (b) Simulated response of the passive and operationally simulated shunt arm of Figure 9.40(a).

https://doi.org/10.1017/9781108762632.010 Published online by Cambridge University Press

Design of the shunt arm begins with the application of equation (9.117), and selection of scaling factor R'' as 1 kΩ. As impedance scaling factor R' was 1 kΩ, factor $k_p = 1$. It results in capacitor $C = C_{p1} = 0.05$ μF. With k_p being unity, equation (9.116) gives $R_0 = 1$ kΩ.

While selecting $R_{i1} = R_{i2}$, equations (9.118)–(9.120) give $C_2 = C_3 = C_4 = 0.05$ μF, $R_{21} = R_{22} = 2$ kΩ, $R_{31} = R_{32} = \sqrt{2}\,\text{k}\Omega$ and $R_{41} = R_{42} = 2\,\text{k}\Omega$.

Input scaling resistance R_A equals R'' when voltage gain of unity is desired. In the present case, for the passive circuit, gain magnitude is 0.5; hence, R_A is doubled to 2 kΩ.

Figure 9.40(b) shows the simulated frequency response of the de-normalized passive as well as its active version which match well with a notch at 10 krad/s and peak at the same frequencies of 19.92 krad/s and 0.823 krad/s.

Example 9.8: Compare responses of the passive circuit shown in Figure 9.41(a) and its active version as an illustration of the realization of series arm through operation simulation.

Solution: In the normalized passive circuit, resistance $R_L = 1$ kΩ is connected as a load for obtaining the circuit's transfer function. Impedance scaling factor of $R' = 1$ kΩ and a frequency scaling factor of 20 krad/s was employed, resulting in the value of elements as:

$$R_L = 1\ \text{k}\Omega,\ R_{s1} = 1\ \text{k}\Omega,\ L_{s1} = 0.2\ \text{H},\ C_{s1} = 0.05\ \mu\text{F},\ L_{s2} = 0.1\ \text{H},\ C_{s2} = 0.1\ \mu\text{F} \tag{9.129}$$

From equation (9.125b), selecting $C_1 = 0.05\mu\text{F}, k_s^2 = \left(L_{s1} / C_1^2\right) = \left(0.2 / 0.05 \times 10^{-6}\right) = 4 \times 10^6$.

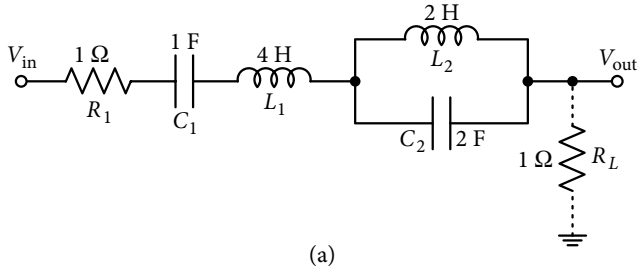
Application of equations (9.125)–(9.127) and selecting $R_{i1} = R_{i2}$ gives the element values as:

$$R_0 = 4\,\text{k}\Omega, R_{21} = R_{22} = 2\,\text{k}\Omega, R_{31} = R_{32} = 2\sqrt{2}\ \text{k}\Omega, R_{41} = R_{42} = 2\,\text{k}\Omega$$

$$C_2 = C_3 = C_4 = 0.05\ \mu\text{F} \tag{9.130}$$

Since R' was selected as 1 kΩ, R'' = 4 kΩ. Hence, to bring the output voltage equal to half at the input (same as in the case of the passive circuit), the value of the resistance $R_A = 2R''$ = 8 kΩ.

Frequency responses of the de-normalized passive circuit and the active circuit are shown in Figure 9.41(b) with notch at 1.58 kHz and peaks at 1.123 kHz and 2.248 KHz.



(a)

https://doi.org/10.1017/9781108762632.010 Published online by Cambridge University Press

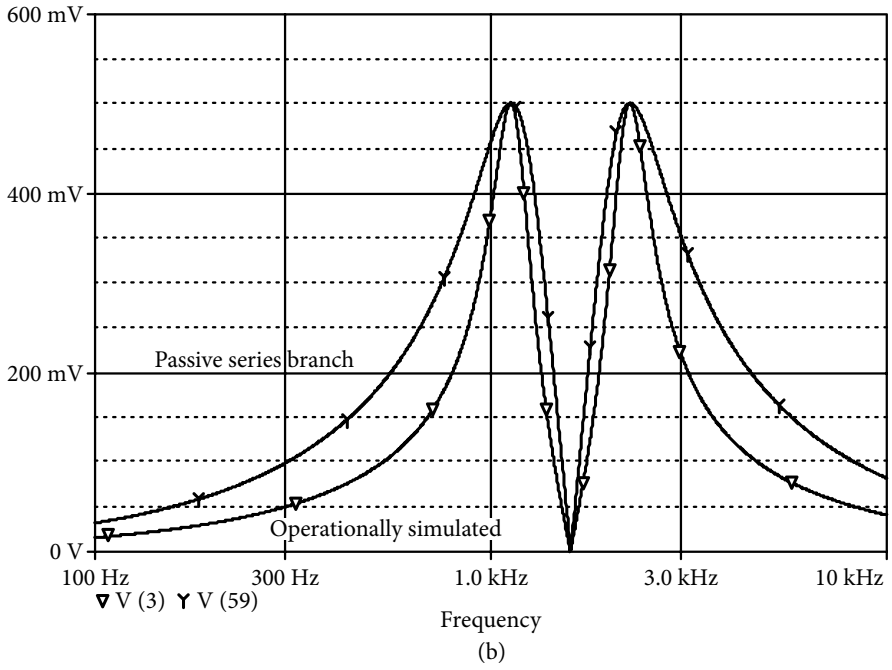


Figure 9.41 (a) Prototype normalized series arm for Example 9.8. (b) Simulated response of the passive and operationally simulated series arm of Figure 9.41(a).

Example 9.8: Redesign the eighth-order BPF of Example 9.6 using the general ladder realization approach.

Solution: Application of the frequency de-normalization by 10^4 rad/s and impedance scaling by a factor of 10^3, elements of the BPF were made available in equations (9.87)–(9.90). Now, its structure is shown in Figure 9.42(a), along with their values, which are calculated in following paragraphs. Design for the complete circuit proceeds in terms of individual branches and then they are properly interconnected.

Series branch number 1: Selecting scaling factor R'' equal to the original impedance scaling factor $R'(1\ \text{k}\Omega)$ gives the coefficient $k_s^2 = 10^6$. Assuming all capacitors to be equal for the series branch, use of equations (9.125b), (9.125a), and (9.126), respectively, give the following values of the elements:

$$C_{11} = \frac{L_{s1}}{k_s^2} = \frac{1.529}{10^6} = 1.529\mu\text{F} \tag{9.131a}$$

$$R_{01} = k_s^2 / R_s = 10^3\,\Omega \tag{9.131b}$$

$$R_{211} = R_{221} = k_s\sqrt{(C_{s1} / C_{21})} = 10^3\sqrt{\left(\frac{6.54 * 10^{-9}}{1.529 * 10^{-6}}\right)} = 65.4\,\Omega \tag{9.131c}$$

https://doi.org/10.1017/9781108762632.010 Published online by Cambridge University Press

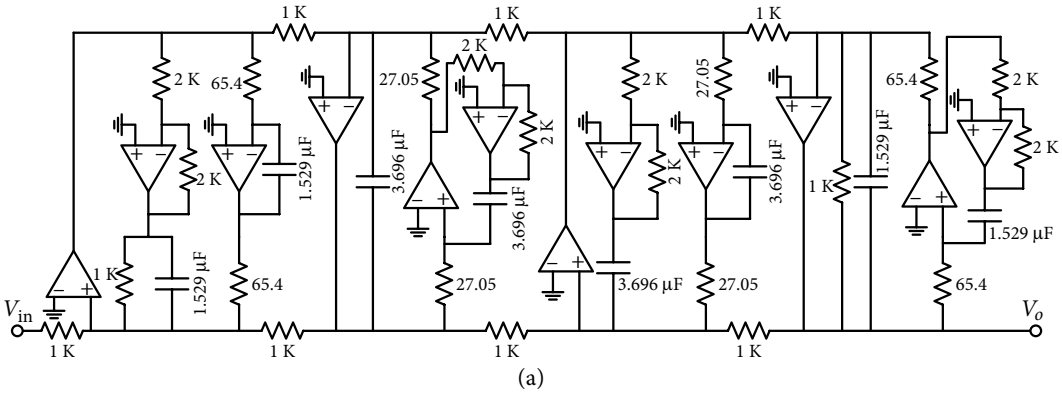


Figure 9.42 (a) Operational simulation circuit with element values for the eighth-order band pass filter of Example 9.9. (b) Response of the eighth-order band pass filter using general ladder realization approach for Example 9.9.

Assuming gain of the filter as unity, the input resistances are:

$$R_{A1} = R_{B1} = R'' = 1\ \text{k}\Omega \tag{9.132}$$

Shunt branch number 2: With all capacitors for the shunt branch taken as equal to C_{12} and $k_p = (R'/R'') = 1$, application of equations (9.117), (9.116), and (9.118), respectively, gives the following values:

$$C_{12} = C_{p1}/k_p = 3.696\ \mu\text{F}, \text{ and } R_{02} = \infty \tag{9.133a}$$

$$R_{212} = R_{222} = k_p\sqrt{\left(L_{p2}/C_{12}\right)} = \sqrt{\left(\frac{2.705\times10^{-3}}{3.696\times10^{-6}}\right)} = 27.05\Omega \tag{9.133b}$$

https://doi.org/10.1017/9781108762632.010 Published online by Cambridge University Press

Input resistances $R_{A2} = R_{B2} = R'' = 1\ \text{k}\Omega$. In fact, for the rest of the two branches, input resistances will be the same.

Series branch number 3: Similar to series branch number 1, all capacitors in the branch remaining equal:

$$C_{13} = 3.696\ \mu\text{F, and } R_{03} = \infty \tag{9.134a}$$

$$R_{213} = R_{223} = k_s\sqrt{(C_{s3}/C_{23})} = 10^3\sqrt{\left(\frac{2.705\times10^{-9}}{3.696\times10^{-6}}\right)} = 27.05\Omega \tag{9.134b}$$

Shunt branch number 4: Similar to the case of branch number 2, and capacitors remaining equal:

$$C_{14} = 1.529\ \mu\text{F and } R_{04} = k_p\,R_{p4} = 1\ \text{k}\Omega \tag{9.135a}$$

$$R_{214} = R_{224} = 10^3\sqrt{\left(\frac{6.54\times10^{-9}}{1.529\times10^{-6}}\right)} = 65.4\ \Omega \tag{9.135b}$$

Figure 9.42(a) shows the combination of all the four branches connected in operational simulation form, along with the element values. The simulated response of the filter is shown in Figure 9.42(b). The simulated center frequency is 1.5878 kHz (9.945 krad/s) with a bandwidth of 78.99 Hz, resulting in $Q = 20.1$. Value of the mid-band gain is 0.462 instead of 0.5.

References

[9.1] Orchard, H. J. 1966. 'Inductor less Filters,' *Electronics Letters* 2: 224–5.

[9.2] Tellegen, B. D. H. 1948. 'The Gyrator, A New Electric Network Element,' *Philips Research Reports* 3: 81–101.

[9.3] Holt, A. G. J., and J. R. Taylor. 1965. 'Method of Replacing Ungrounded Inductances by Grounded Gyrator,' *Electronic Letters* 1 (4): 105.

[9.4] Riordan, R. 1967. 'Simulated Inductance using Differential Amplifiers,' *Electronic Letters* 3(2): 50–1.

[9.5] Antoniou, A. 1969. 'Realization of Gyrators using Operational amplifiers and Their Use in Active Network Synthesis,' *IEE Proceedings* 16: 1838–50.

[9.6] Dutta Roy, S. C. 1974. 'A Circuit for Floating Inductance Simulation,' *IEEE Proceedings* 62: 521–3.

[9.7] Gorski-Popiel, G. 1967. 'RC-Active Synthesis using Passive Immittance Converter,' *Electronic Letters* 3: 381–2.

[9.8] Bruton, L. T. 1969. 'Network Transfer Functions Using the Concept of Frequency Dependent Negative Resistance,' *IEEE Transactions on Circuit Theory* CT-16: 406–8.

https://doi.org/10.1017/9781108762632.010 Published online by Cambridge University Press

Practice Problems

9-1 (a) Input impedance expression for the circuit in Figure 9.9(b) is obtained as $Z_{in} = Z_1Z_3Z_5/Z_2Z_4$ with OAs considered ideal. Resulting expression of the simulated inductance is given as $L_{eq} = R_1R_3R_5C/R_2$. Show that, when OAs are modeled by their first-order roll-off model as $A_i = B_i/s$, following input impedance is derived for the working frequency range $\omega^2 << (B_1B_2)$ as:

$$Z_{in}(s) \simeq sLeq\frac{1+\left(\frac{R_2}{R_3}\frac{1}{A_2}+\frac{1}{A_1}\right)\left(1+\frac{1}{sC_4R_5}\right)}{1+\left(\frac{1}{A_2}+\frac{R_3}{R_2}\frac{1}{A_1}\right)\left(1+sC_4R_5\right)}$$

(b) With $s = j\omega$, simulated impedance is $Z_{in}\, j\omega = j\omega\,(L_{eq} + \Delta L) + R_s$. Find expressions for ΔL and R_s.

(c) What shall be the significance of selecting resistance $R_2 = R_3$.

9-2 Design a lossless ladder for the following specifications:

$$\omega_1 = 2\frac{\text{krad}}{s}, A_{max} = 1\text{dB}, \omega_2 = 4\frac{\text{krad}}{\text{s}} \text{and } A_{min} = 20\,\text{dBs}$$

Use equal-ripple approximation with double termination ladder and realize the filter using GIC based inductor simulation. If possible, select a capacitor of 10 nF each.

9-3 Design an LC filter with Chebyshev approximation and minimum inductors and $R_{in} = R_{out} = 600\ \Omega$. Replace the inductors by an OA RC circuit; specifications are:

$f_1 = 12.5$ kHz, $A_{max} = 1$ dB, $f_2 = 56.25$ kHz, and $A_{min} = 35$ dBs

9-4 Obtain an active RC version of the ladder shown in Figure P9.1 using a gyrator, with $R_{in} = R_{out} = 1\ \text{k}\Omega$, $C_1 = C_3 = 20.94$ nF, $C_2 = 3.306$ nF and $L_2 = 0.8347$ H.

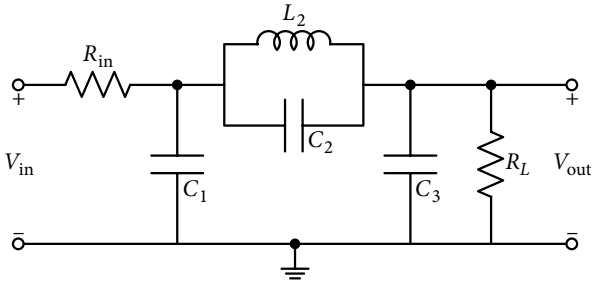


Figure P9.1

9-5 Design a GIC based third-order HP filter with Butterworth approximation having 3 dB frequency of 5 kHz. Use a doubly terminated ladder and capacitors need to be of 1 nF, if possible.

9-6 Realize the ladder shown in Figure P9.1 using Bruton's approach.

9-7 Design a fifth-order HP active RC filter using inductance simulation technique, having pass band ripples less than 1 dB and corner frequency of 100 krad/s. Compare its response with that of the passive prototype filter.

https://doi.org/10.1017/9781108762632.010 Published online by Cambridge University Press

9-8 Realize the ladder shown in Figure P9.2 using Bruton's approach for a center frequency of 10 kHz and $Q = 10$.

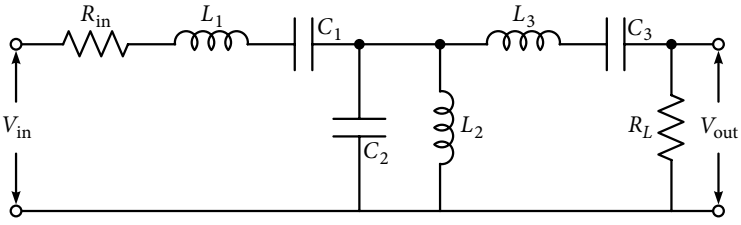


Figure P9.2

9-9 Design and test an LPF using operational simulation from a normalized third-order Butterworth filter. Cut-off frequency is 1 kHz and the terminating resistors are 2 kΩ each.

9-10 Repeat Problem 9-9 for a fifth-order Butterworth filter with the other specifications remaining the same.

9-11 Design and test an LPF using operational simulation from a normalized fifth-order Chebyshev filter. Pass band ridge frequency is 1 kHz and the terminating resistors are 2 kΩ each.

9-12 Specifications of a Butterworth LPF: range of pass band $0 \leq \omega \leq 8000$ rad/s and range of stop band 32000 rad/s $\leq \omega \leq \infty$ with $\alpha_{min} = 16$ dBs and $\alpha_{max} = 0.5$ dB. Design and test using the operational simulation approach.

Note: For Problems 9-13 to 9-16, employ the technique in Section 9.11.

9-13 A BPF is to be designed using a third-order LP Butterworth filter. Its center frequency is to be 2 kHz and quality factor $Q = 10$. Test the circuit using practical element values.

9-14 Repeat Problem 9-13 if its prototype is a fourth-order Butterworth filter.

9-15 Design a BPF with $\omega_o = 5$ krad/s and 3 dB bandwidth = 4500 rad/s. The prototype is to be a fourth-order maximally flat band pass.

9-16 An active BPF is to be constructed from a passive structure shown in Figure P.9.2 (Problem 9.16). Center frequency, lower and upper cut frequencies are 1265 Hz, 800 Hz and 2000 Hz, respectively. Employ operational simulation method to obtain the filter and test it.

9-17 In Figure 9.35(a), series resonance is to be at 4 krad/s and shunt resonance at 8 krad/s. Verify the frequency response with that of the passive structure. A resistance of 1 kohm is used in the de-normalized circuit.

9-18 Repeat Problem 9-17 for the circuit in Figure 9.35(b) with the shunt resistance in the de-normalized circuit being 1 kohm.

9-19 Use impedance scaling of 10^3 and frequency scaling of 10^5 for the series branch of Figure P9.3

https://doi.org/10.1017/9781108762632.010 Published online by Cambridge University Press

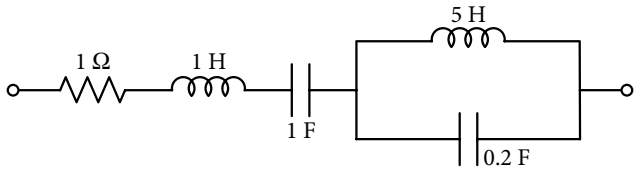


Figure P9.3

and compare frequency response with its de-normalized passive version.

9-20 Repeat Problem 9-19 for the circuit shown in Figure P9.4.

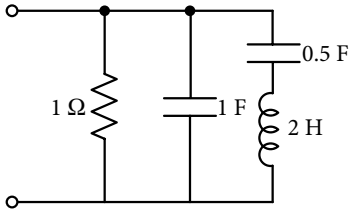


Figure P9.4

https://doi.org/10.1017/9781108762632.010 Published online by Cambridge University Press