Chapter 16

Current Conveyors and CDTA (Current Differencing Transconductance Amplifiers) Based Filters

16.1 Introduction

All conventional analog circuits are voltage mode (VM) circuits, where the performance of the circuit is determined in terms of voltage levels at all nodes including those at the input and output nodes; operational amplifiers (OAs), being the most commonly used active device, is a voltage controlled voltage source (VCVS). Unfortunately, VM circuits do suffer from some limitations: (i) voltages in the circuit cannot change very quickly when input voltage changes suddenly due to parasitic capacitances; (ii) the bandwidth of OA based circuits is usually limited to the audio frequency range unless high bandwidth OAs are used; and (iii) circuits generally do not have high voltage swings and require high supply voltages for better signal-to-noise ratio.

In the current mode (CM) approach, the circuit description is presented in terms of current. This implies that all signals, including those at the input and the output are taken in terms of current rather than voltage and the active devices used are preferably CM devices. Hence, CM signal processing techniques can be defined as the processing of current signals in an environment where voltage signals become irrelevant in determining circuit performance, although CM devices do generate VM circuits as well [16.1].

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Advancements in IC (integrated circuits) technologies together with the demand for smaller and low power devices have necessitated in the development of monolithic IC filters, not only at audio frequency but at a much higher frequency range. The advent of sub-micron IC processing (0.5 μm and smaller) has facilitated the realization of filters even in the VHF frequency (30–300 MHz) band. Together with its high frequency operation, reduction in power consumption is another advantage of CM filter circuits. In view of this, attention is being paid toward signal processing in terms of current rather than voltage. This new type of signal processing is known as CM signal processing and is evolving into a better alternative to VM signal processing, especially in the high frequency region.

CM signal processing leads to a higher frequency range of operation because the signal current is delivered to a small (ideally short circuit) load resistance. Due to this small resistance, the parasitic pole frequency becomes very high. As a result, signals are processed without any appreciable deviation for much larger frequencies. In summary, the following are the main advantages of the CM approach: (i) much larger frequency range of operation, (ii) easy addition, subtraction and multiplication of signals, (iii) higher dynamic range, (iv) lower power consumption with reduced power supply voltage and (v) better suited to micro-miniaturization and simpler circuits.

Second-generation current conveyors (CCs) being the most versatile, its description and MOS (metal–oxide–semiconductor) implementation is discussed in Section 16.2. It is used to generate some basic building blocks (BBBs) like controlled signal sources, weighted current and voltage summers, lossless and lossy CM and VM integrators discussed in Section 16.3. First-order filters are studied in Section 16.4, and a variety of second-order filters are included in Sections 16.5 to 16.9. Some circuits of inductance simulation are shown in Section 16.10 for their use in direct form synthesis. Current differencing transconductance amplifiers (CDTA), its application for inductance simulation, and development of biquadratic filters is shown in Section 16.11.

16.2 Second Generation Current Conveyors (CCII±)

Current conveyors are very versatile elements and they have become available in many forms, like first generation current conveyors (CCIs), second generation current conveyors (CCIIs), differential voltage current conveyors (DVCCs), current controlled current conveyor (CCCIIs) and dual-X current conveyors (DXCCIIs).

As mentioned here, there are many versions of CCs, but more attention has been given to CCIIs in literature and in this chapter as well. The reason being that it is one of the most functionally flexible and versatile CC since its inception [16.2, 16.3].

A current conveyor (CC) is a 3-port device with four (even five) terminals, which has emerged as a powerful alternative to OAs for performing analog signal processing. The first CC introduced in 1968 by Smith and Sedra [16.2] and named as CCI is shown in block form in Figure 16.1(a), for which the current–voltage relationship is given as:

$$i_Y = i_X,\ v_X = v_Y, \text{ and } i_Z = \pm i_X \tag{16.1}$$

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Here, current and voltage variables represent total instantaneous values. It is important to understand the meaning of the relations in equation (16.1) in conjunction with its block diagram in Figure 16.1(a). If an input current i_X flows in terminal X, it will force an equal current i_Y to flow in terminal Y. Similarly, if voltage v_Y is applied at terminal Y, an equal voltage v_X will appear at the terminal X. The same amount of current i_Z will go into or come out as i_X, but the terminal Z has a high impedance level and thus behaves like a current source.

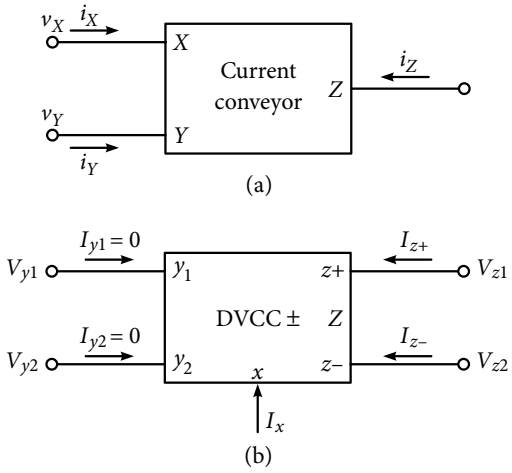

Figure 16.1 (a) A current conveyor in block form showing terminal voltages and currents. (b) Symbolic representation of a differential voltage CCII± with dual outputs (DVCCII).

Bipolar technology was used in the early stages of development of CCs in1960s. However, fabrication of good quality pnp transistors, which was a necessity to get near ideal CCs, was difficult. Later, with the availability of CMOS (complementary MOS) technology, which could provide good quality matching MOS transistors, it became comparatively easy to fabricate quality CCs.

CCI was soon overtaken by its second version CCII in which current does not flow in terminal Y [16.3]. For the same block-form representation of CCII in Figure 16.1(b), the current–voltage relationship is given as:

$$\begin{bmatrix} i_Y \\ v_X \\ i_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_Y \\ i_X \\ v_Z \end{bmatrix} \tag{16.2a}$$

The terminal Y has infinite input resistance. Terminal X follows the voltage at terminal Y, and ideally, it exhibits zero input impedance. Direction of current at terminal Z, which is at infinite output resistance ideally, defines the polarity of the CCII. As per convention, when current is going into the Z terminal, it is called a positive CCII (CCII+), and for outgoing current at Z terminal, it is called negative CCII (CCII-).

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If CCs are compared to OAs, it is observed that CCs can be realized whose performance is very close to their ideal values. Practically, the impedance level at terminal X is close to zero, and at terminal Z, the level is close to infinity, making the device a near perfect current source.

Signal processing functions which were realized using OAs, can be designed in a comparatively simpler way using CCs. Additionally, there are some other advantages too. One of the major advantages in using CCs is that a higher voltage (or current) gain becomes possible over a larger signal bandwidth for small input signals, or large signal frequency conditions. This amounts to a much higher gain–bandwidth product than obtainable with OAs.

A number of structures are available for realizing CCs. One such CMOS implementation of a differential voltage input current conveyor (DVCCII) is available in reference [16.4] along with the size of the MOSFETs (MOS field effect transistors) used in it.

Equation (16.2a) represents the current–voltage relation of an ideal CC with no parasitics whereas practical CCs do have some parasitics. To study the non-ideal behavior, the relationship given in equation (16.1) can be modified as:

$$I_Y = 0,\ V_X = \beta V_Y,\ I_Z = \pm\alpha I_X \tag{16.2b}$$

where the voltage transfer gain β from Y to X deviates from unity by an amount equal to the voltage transfer errors. Similarly, the current transfer gain α from X to Z represents a deviation from unity as current transfer error. The errors are expected to be quite low for integrated CCs for a large frequency range.

16.3 Some Basic Building Blocks

Current conveyors are able to realize almost all basic building blocks and complex networks which can be realized using OAs or OTAs (operational transconductance amplifiers). In fact, even at the very beginning of its usage, a large number of active network and signal processing basic blocks were given, showing the utility of CCs. Figures 16.2 and 16.3 show some of the basic building blocks using CCs, which can be utilized alone or for building more complex structures. Figures 16.2(a) and (b) show a voltage controlled current source (VCCS) and a current-controlled voltage source (CCVS), respectively.

For the VCCS:

$$I_1 = 0,\ I_x = (V_x/R) = (V_1/R) = I_z = I_2 \tag{16.3}$$

Output current I_2 depends on input voltage V_1; and for the CCVS:

$$V_1 = V_{x1} = 0,\ I_{z1} = I_1,\ V_2 = V_{y2} = I_{z1}R = I_1R \tag{16.4}$$

Equation (16.4) shows that the output voltage V_2 depends on the input current I_1.

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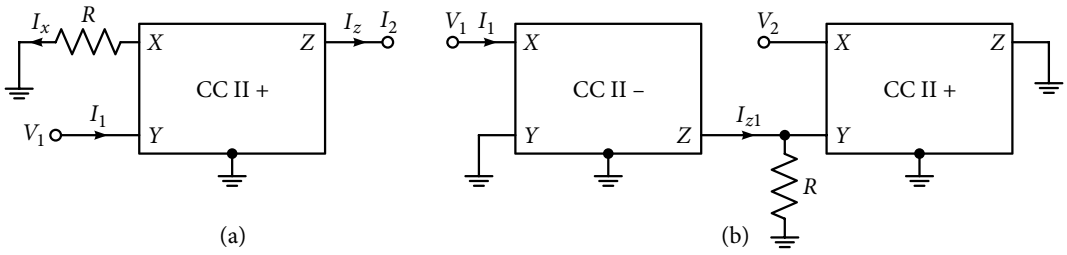

Figure 16.2 Current conveyor based (a) voltage controlled current source and (b) current controlled voltage source.

Some signal processing basic blocks like non-inverting current amplifiers, current integrators, and weighted current summers are shown in Figures 16.3(a), (b), and (c), respectively. Here, the relation for the current amplification for Figure 16.3(a) is given as:

$$V_y = I_{in}R_1 = V_x \rightarrow I_x = V_x/R_2 = I_{in}R_1/R_2 \rightarrow I_o/I_{in} = R_1/R_2 \tag{16.5a}$$

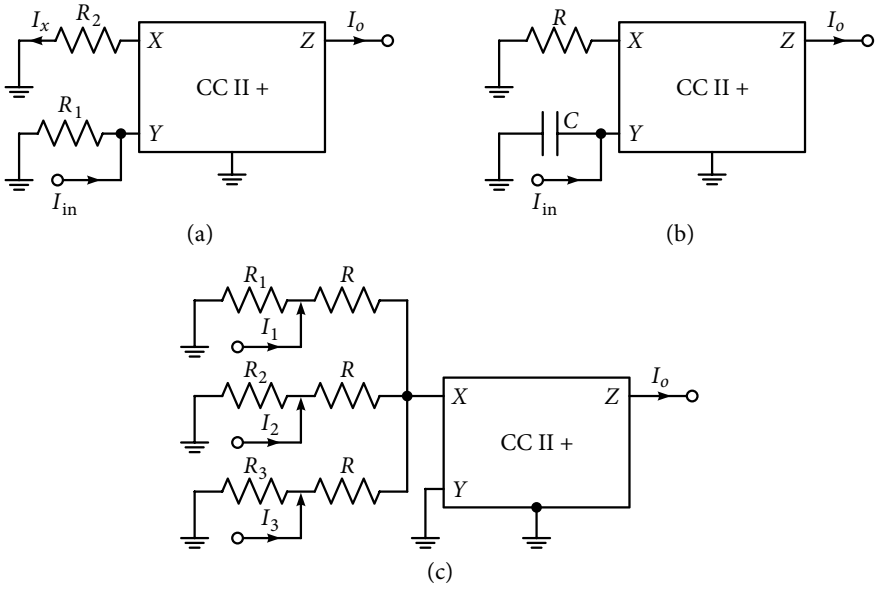

Figure 16.3 Current conveyor based (a) current amplifier, (b) current integrator and (c) current summation.

If R_1 is replaced by C, as shown in Figure 16.3(b), the CCII+ acts as an ideal current integrator for which expression of current gain is:

$$I_o/I_{in} = 1/sCR \tag{16.5b}$$

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For the weighted current summer of Figure 16.3(c), the expression for the output current is given as:

$$I_o = I_1 \{R_1/(R + R_1)\} + I_2 \{R_2/(R + R_2)\} + I_3\{R_3/(R + R_3)\} \tag{16.6}$$

It is to be noted that the current amplification factor will be less than unity with this configuration and the weighted summer can become a simple adder when input currents are applied directly at the terminal *X*; the number of currents to be summed up can be arbitrarily large.

Figure 16.4(a) and (b) show lossy integrators. In Figure 16.4(a), the direction of currents I_x and I_z has been shown to be negative for CCII; hence:

$$V_x = V_y = V_{in},\ I_x = (V_{in}/R_1),\ V_z = -I_z\{R_2/(1 + sCR_2)\} = V_{out} \tag{16.7}$$

$$(V_{out}/V_{in}) = -(R_2/R_1)/(1 + sCR_2) \tag{16.8}$$

For the inverting current integrator shown in Figure 16.4(b):

$$V_y = I_{in}(R_2/1+ sCR_2) = V_x,\ I_z = -I_x = -V_x/R_1$$

$$(I_{out}/I_{in}) = -(R_2/R_1)/(1+ sCR_2) \tag{16.9}$$

DC gain for both the VM and CM lossy integrators is (R_2/R_1) and half-power frequency is $1/CR_2$.

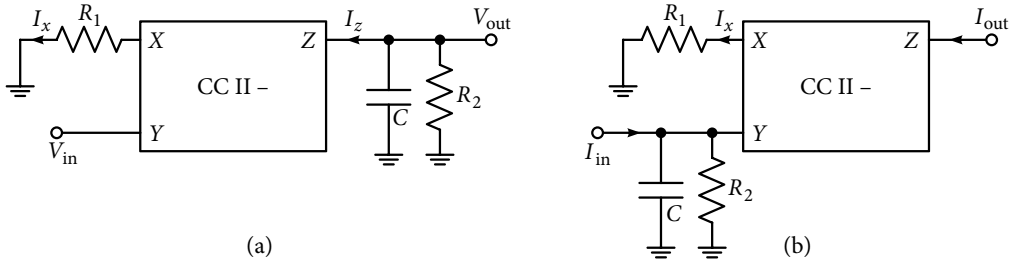

Figure 16.4 Lossy inverting integrator in (a) voltage mode and in (b) current mode.

If resistor R_2 is removed from Figures 16.4(a) or (b), it will result in respective lossless integrators.

16.4 Current Conveyor Based First-order Filters

Integrators of the circuits shown in Figure 16.4 behave as LPFs with the expression for 3 dB frequency as $1/2\pi RC$. However, there are a few simple circuits which act as all pass (AP) first-

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order filter structures, but can be simplified to act as an HPF (high pass filter) and LPF (low pass filter) as well.

As $V_x = V_y$ in Figure 16.5(a), impedances Z_1 and Z_2 are virtually parallel and current division in the two branches takes place accordingly; analysis give the following relations [16.5]:

$$V_x = V_y = Z_4\left(\frac{Z_1 I_{\text{in}}}{Z_1 + Z_2}\right),\ I_z = I_x = I_{\text{in}}\frac{Z_2}{Z_1 + Z_2} - \frac{V_x}{Z_3}$$

$$\frac{I_{\text{out}}}{I_{\text{in}}} = -\frac{I_z}{I_{\text{in}}} = -\frac{Z_2 Z_3 - Z_1 Z_4}{Z_3(Z_1 + Z_2)} \tag{16.10}$$

For $Z_3 = Z_4 = R'$, $Z_1 = 1/sC$ and $Z_2 = R$

$$\frac{I_{\text{out}}}{I_{\text{in}}} = -\frac{sCR - 1}{sCR + 1} \tag{16.11}$$

It works as a current mode first-order APF; it also works the same way if $Z_1 = R$ and $Z_2 = (1/sC)$ with negative sign removed in equation (16.11).

For $Z_4 = 0$, $Z_3 = \infty$, $Z_2 = R$, and $Z_1 = 1/sC$, the circuit becomes a CM first-order HP section; whereas, it becomes an LP section with $Z_1 = R$ and $Z_2 = 1/sC$. It will be shown a little later that the circuit can also provide second-order sections with some other combination for impedances.

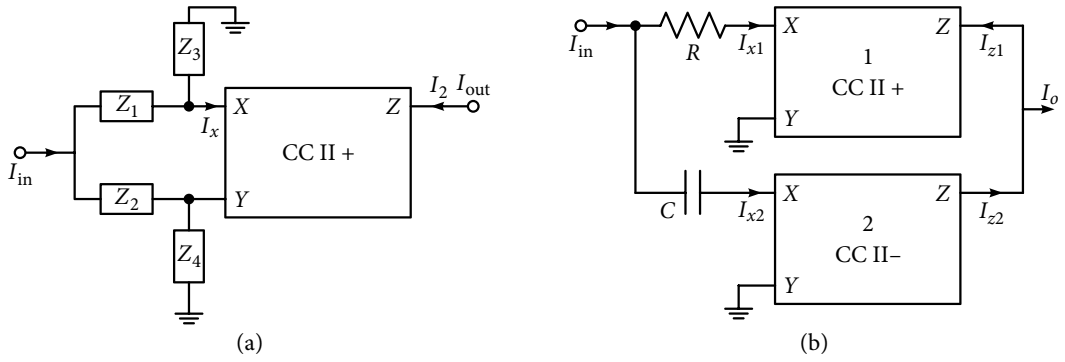

Figure 16.5 First-order current mode (a) general structure, and (b) alternate circuit using two CCs {With permission from Springer Nature}.

Another AP network is shown in Figure 16.5(b) using two CCs, a resistor and a capacitor. Resistor R and the capacitor C become practically parallel with both the Y terminals grounded. The circuit is a current input current output (CICO) configuration with the following relation:

$$V_{x1} = V_{x2} = V_{y1} = V_{y2} = 0,\ I_{z1} = I_{x1} = \frac{1/sC}{R + 1/sC},\ I_{z2} = I_{x2} = \frac{R}{R + 1/sC}$$

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$$I_o = I_{z2} - I_{z1} = \frac{sCR - 1}{sCR + 1} \tag{16.12}$$

Example 16.1: Obtain a CM HPF from the general structure shown in Figure16.5(a) having a 3 dB frequency of 1000 krad/s.

Solution: The HPF section is shown in Figure16.6(a) and derived from Figure 16.5(a). For selected value of C = 0.2 nF, R = 5 kΩ, its magnitude response is shown in Figure 16.6(b). High frequency gain is almost unity and the simulated 3 dB frequency is 159.46 kHz.

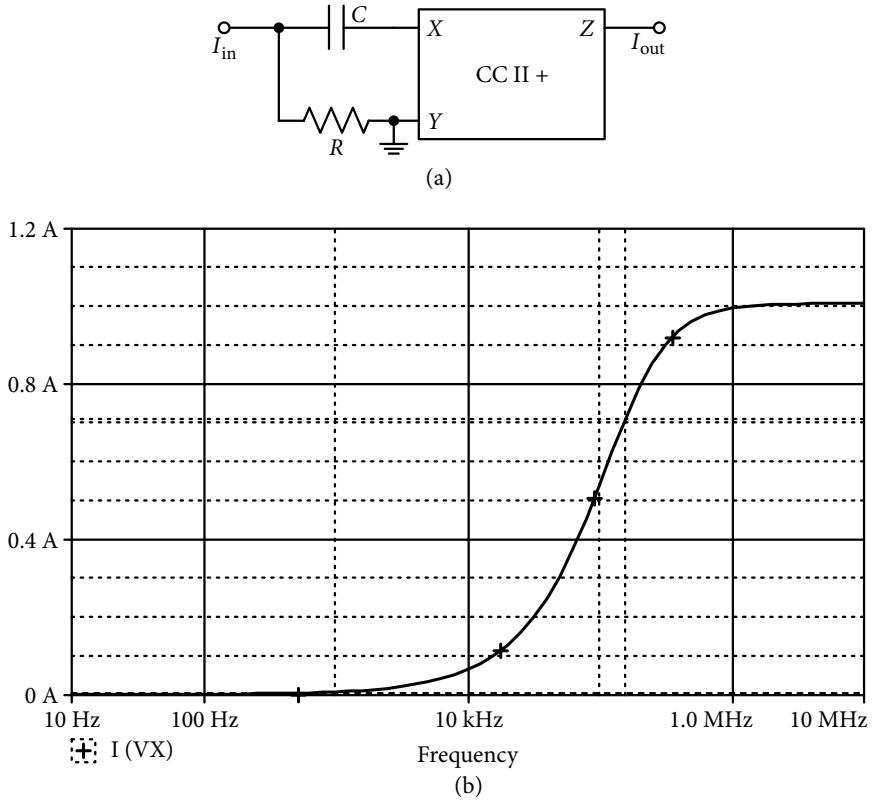

Figure 16.6 (a) Current mode HP filter from Figure 16.5(a) and (b) its simulated magnitude response.

16.5 Current Conveyor Based Second-order Filters

A large number of approaches have been used to obtain second-order filter structures using CCs. However, almost all of the approaches are like those employed in OA-RC or in OTA-RC cases. While most of the time CCIIs are used, sometimes CCIs are also used as will be shown later.

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16.5.1 Wein bridge based structure

It was mentioned earlier that more options are available in Figure16.5(a) for the selection of branch impedances. For example, if we select Z_1 as a series combination of resistance R_1 and capacitance C_1, and Z_2 as a parallel RC combination as shown here:

$$Z_1 = (1 + sC_1R_1)/sC_1,\ Z_2 = R_2/(1 + sC_2R_2),\ Z_3 = \infty \text{ and } Z_4 = 0 \tag{16.13}$$

a BP (band pass) response becomes available at the output, and equation (16.10) yields:

$$(I_{out}/I_{in}) = sC_1R_2/D(s) \tag{16.14}$$

$$D(s) = s^2C_1C_2R_1R_2 + s(C_1R_1 + C_1R_2 + C_2R_2) + 1 \tag{16.15}$$

From equation (16.15), the second-order BPF parameters are:

$$\omega_o^2 = 1/\left(C_1C_2R_1R_2\right) \tag{16.16}$$

$$Q = \frac{\sqrt{\left(C_1C_2R_1R_2\right)}}{\left(C_1R_1 + C_1R_2 + C_2R_2\right)} \tag{16.17}$$

$$\text{Mid-band gain } h_{mbg} = \frac{\left(C_1R_2\right)}{\left(C_1R_1 + C_1R_2 + C_2R_2\right)} \tag{16.18}$$

It is to be noted that the maximum obtainable value of Q with this configuration is less than 0.5.

Example 16.2: Design a second-order BPF with a 3 dB frequency of 400 krad/s and $Q = 0.4$ using the general configuration of Figure 16.5(a).

Solution: Assuming $C_1 = KC_2$ and $KR_1 = R_2$, and then using equations (16.16) and (16.17), the component values are:

$$4 \times 10^5 = 1/R_2C_2 \rightarrow R_2 = 2.5\ \text{k}\Omega,\ C_2 = 1.0\ \text{nF} \tag{16.19a}$$

In addition, with the help of equation (16.17):

$$Q = 0.4 = \frac{\sqrt{KC_2C_2R_2R_2\ /\ K}}{C_2R_2 + KC_2R_2 + C_2R_2} \rightarrow K = 0.5 \tag{16.19b}$$

So, $R_1 = 5\ \text{k}\Omega$, and $C_1 = 0.5$ nF

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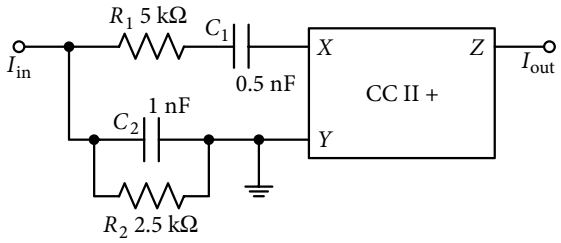
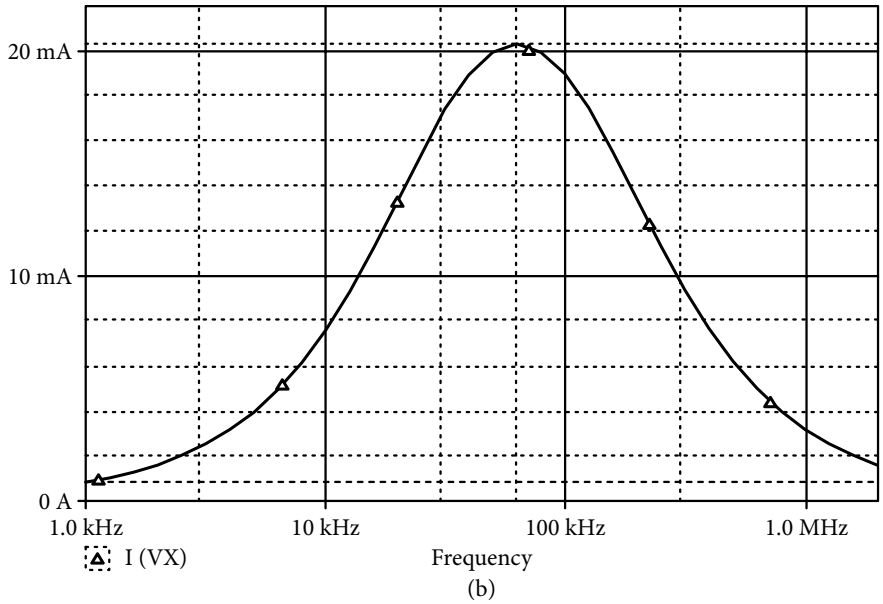
The designed circuit with element values is shown in Figure 16.7(a) and its simulated response is shown in Figure 16.7(b). Center frequency is obtained as 63.096 kHz (396.6 krad/s) and with the bandwidth of 157.98 kHz, value of Q = 0.399; very close to the design.



(a)



(b)

Figure 16.7 (a) Band pass filter from the general configuration of Figure 16.5(a); (b) its simulated response as a low-Q band pass CM filter.

In an alternate case, if we select the following combination of elements in Figure 16.5(a):

$$Z_1 = R_1 + (1/sC_1),\ Z_2 = R_2/(1 + sC_2R_2),\ Z_3 = R_3 \text{ and } Z_4 = R_4 \tag{16.20}$$

The obtained CM transfer function is as follows:

$$\frac{I_{out}}{I_{in}} = \frac{R_4}{R_3}\frac{s^2C_1C_2R_1R_2 + s\left(C_1R_1 + C_2R_2 - C_1R_2R_3 / R_4\right) + 1}{s^2C_1C_2R_1R_2 + s\left(C_1R_1 + C_2R_2 + C_1R_2\right) + 1} \tag{16.21}$$

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The circuit can now behave as an AP or a notch, under the following respective conditions:

$$\frac{R_3}{R_4} = \frac{2(C_1R_1 + C_2R_2)}{C_1R_2} + 1 \tag{16.22}$$

$$\frac{R_3}{R_4} = \frac{(C_1R_1 + C_2R_2)}{C_1R_2} \tag{16.23}$$

The important parameters of the filters are obtained from equation (16.21) as:

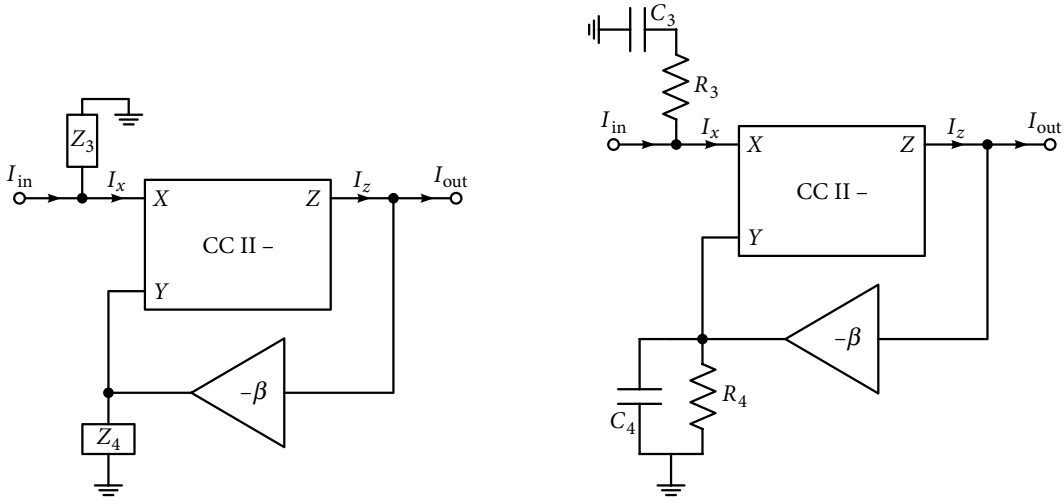
$$\omega_o^2 = 1/C_1C_2R_1R_2 \tag{16.24}$$

$$\text{Gain at dc} = R_4/R_3 \tag{16.25}$$

It is to be noted that in the aforementioned configuration of Figure 16.5(a), only real poles are possible, that is why in Example 16.2, Q was taken less than 0.5. To obtain complex conjugate poles, one option is to replace CCII by CCI, because CCI can be considered as a combination of CCII with an additional current output feed back to the Y input [16.6]. Hence, with Z_1 = 0 and $Z_3 = \infty$, Figure 16.5(a) modifies to Figure 16.8(a) using CCI, which gives the following relation:

$$V_y = V_x = (I_{in} - I_x)Z_3 = (I_{in} - I_{out})Z_3,\ V_y = -\beta I_{out}Z_4$$

$$(I_{out}/I_{in}) = Z_3/(Z_3 - \beta Z_4) \tag{16.26}$$



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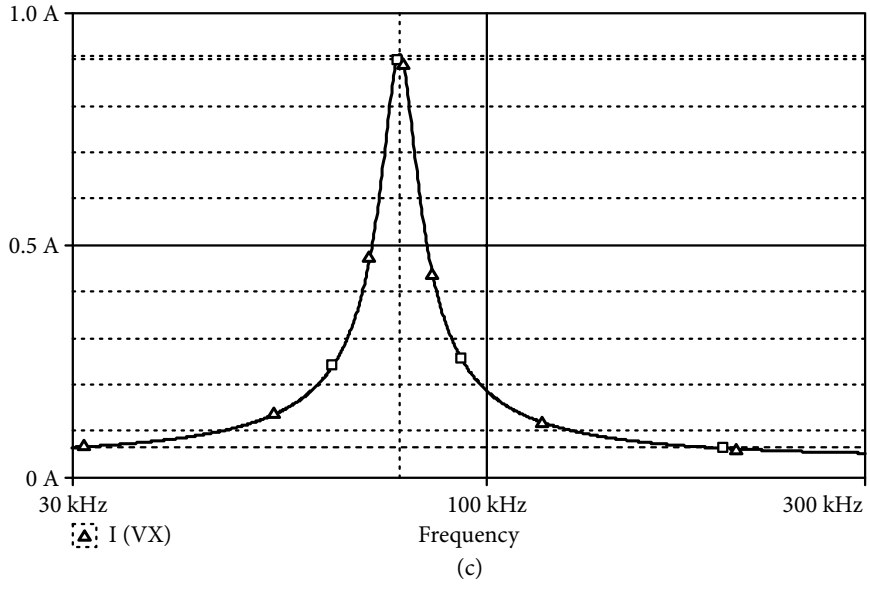

Figure 16.8 (a) First-order current mode filter which can realize complex poles {With permission from Springer Nature} (b) a CCI-RC version. (c) Response of the band pass filter for Figure 16.8(b) realizing high Q.

A CMBP (current mode band pass) transfer function can be obtained using equation (16.23), if we select $Z_3 = (R_3 + 1/sC_3)$ and $Z_4 = R_4/(1 + sC_4R_4)$. The resulting circuit is shown in Figure 16.8(b) and the transfer function is given as:

$$\frac{I_{out}}{I_{in}} = \frac{sC_3R_3/\beta}{s^2C_3C_4R_3R_4 + s\left(C_3R_3 + C_4R_4 - C_4R_3/\beta\right) + 1} \tag{16.27}$$

The BP response can have a large value of pole-Q on account of the difference term in the denominator. If the selected elements are R_3 = 1 kΩ, R_4 = 2 kΩ, C_3 = 2 nF and C_4 = 1 nF, center frequency will be 500 krad/s, and with feedback factor of 19/20, the expected value of Q = 10. The simulated circuit response is shown in Figure 16.8(c), where center frequency is 79.077 kHz and Q = 9.65.

16.6 High Input Impedance Biquads Using CCIIs

Filter realizations where the input is applied at terminal X do not have high input impedance because of the CC's characteristics. When it is important to have high input impedance of the filter, its input needs to be applied at terminal Y as I_y = 0. Quite a few circuits are available with input at Y. A representative circuit is shown in Figure 16.9(a)[16.7]. Its nodal current equations are:

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$$I_x + (V_{in} - V_1)Y_1 = 0 \tag{16.28a}$$

$$V_1(Y_1 + Y_2 + Y_3) - V_{in}\,Y_1 - V_2Y_3 = 0 \tag{16.28b}$$

$$V_2(Y_3 + Y_4) - V_1Y_3 - I_z = 0 \text{ and } I_z = I_x \tag{16.28c}$$

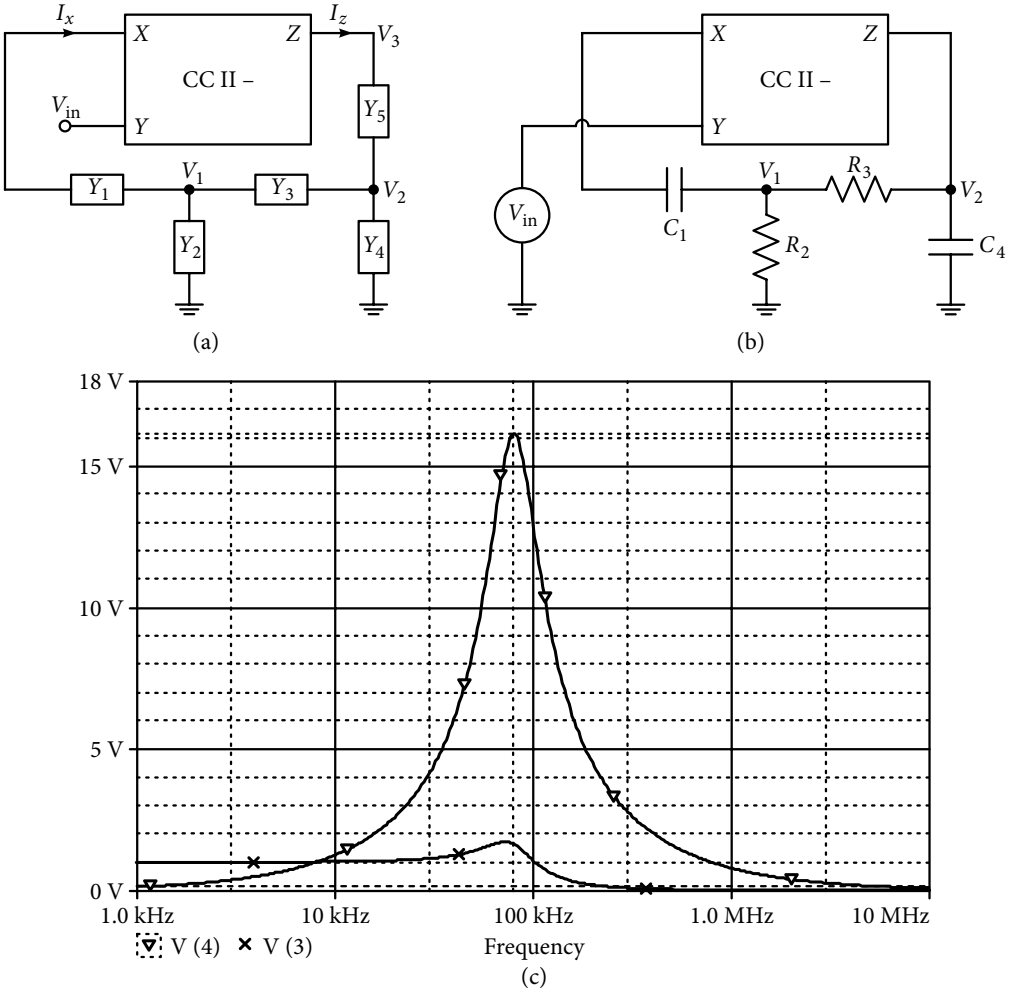

Figure 16.9 (a) High input impedance single CC biquad {With permission from Springer Nature}, and (b) circuit for providing high pass and band pass responses for Example 16.3. (c) Band pass and low pass responses from the circuit shown in Figure 16.9(b), when input is applied at the high impedance terminal Y.

Solving equations (16.28a–c) give the following transfer functions:

$$V_1/V_{in} = Y_1\,Y_4/D_1(s), \text{ and } V_2/V_{in} = Y_1\,Y_2/D_1(s) \tag{16.29a, b}$$

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$$D_1(s) = Y_1\,Y_4 + Y_2\,Y_3 + Y_2\,Y_4 + Y_3\,Y_4 \tag{16.29c}$$

$$V_3/V_{\text{in}} = -Y_1\,(Y_3\,Y_4 + Y_2\,Y_3 + Y_2\,Y_4 + Y_2\,Y_5)/Y_5\,D_1(s) \tag{16.30}$$

The circuit provides LP and BP responses easily with $Y_1 = G_1$, $Y_2 = sC_2$, $Y_3 = sC_3$, $Y_4 = G_4$ and $Y_5 = G_5$ or zero. The important parameters of the second-order filter section will be:

$$\omega_o = (G_2G_4 / C_2C_3)^{\frac{1}{2}},\ Q = (G_1G_4C_2C_3)^{\frac{1}{2}} / (C_2G_4 + C_3G_4) \tag{16.31}$$

To get a combination of BP and HP responses, we need to select:

$Y_1 = sC_1$, $Y_2 = G_2$, $Y_3 = G_3$, $Y_4 = sC_4$ and $Y_5 = G_5$ or zero

It gives the denominator and the parameters as:

$$D_2(s) = C_1C_4\,s^2 + (G_2 + G_3)\,C_4s + G_2G_3 \tag{16.32}$$

$$\omega_o = (G_2G_3 / C_1C_4)^{\frac{1}{2}},\ Q = (G_2G_3C_1)^{\frac{1}{2}} / (C_4)^{\frac{1}{2}}(G_2 + G_3) \tag{16.33}$$

Figure 16.9(b) shows the realized circuit with elements for which HP and BP responses will be:

$$V_1D_2(s)/V_{\text{in}} = Y_1\,Y_4 = s^2C_1C_4 \tag{16.34}$$

$$V_2D_2(s)/V_{\text{in}} = Y_1Y_2 = sC_1\,R_2 \rightarrow \text{mid-band gain} = C_1/C_2 \tag{16.35}$$

Example 16.3: Design a BPF with a center frequency of 500 krad/s and pole-Q = 1.666. Verify the LP response as well.

Solution: Using equation (16.31), the calculated values of the elements are

$R_1 = 1\ \text{k}\Omega$, $C_2 = 1$ nF, $C_3 = 0.2$ nF and $R_4 = 20\ \text{k}\Omega$

Figure 16.9(c) shows the simulated response, where the center frequency of the BPF is 79.76 kHz (501.3 krad/s), which is close to the design value and the obtained Q = 1.637 is slightly less than the design value of 1.666. For the LP response, a peak occurs at 73.16 kHz with a peak gain of 1.72. The LP has unity gain at dc and its critical frequency is calculated as f_o = $73.16(1 - 1/2 \times 1.72^2)^{-0.5}$ = 80.25 kHz (504.4 krad/s).

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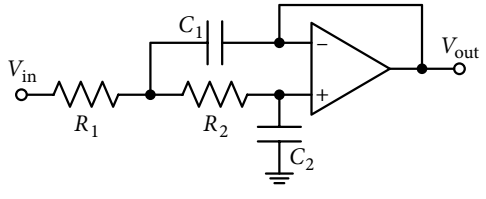
16.7 Application of Voltage Following Property of CCs

We know that the X terminal follows the Y terminal voltage in a CC like the two input terminals of an ideal OA. This property can be utilized to convert some OA-RC circuits into CC based ones. For example, the well-known Sallen–Key circuit shown in Figure 16.10(a) is shown in Figure 16.10(b) as a CC based circuit. The circuit can provide VM as well as CM responses, using two CCs. Here, the output voltage is taken using the CCII+2 based voltage amplifier. In an OA-RC circuit, voltage at the inverting and non-inverting terminals is ideally equal. In the CC version, $V_{y1} = V_{x1}$ and if $R_3 = R_4$, voltage level at V_{y2} and hence, V_{x2} will also be equal to V_{y1}, making the CC version equivalent to the OA-RC circuit. It is significant to notice that the technique is applicable to other active RC filters to get either a unity or finite gain voltage amplifier. The following current–voltage relations are obtained for the CC based circuit:

$$V_{out} = V_{y1} = V_{x1},\ I_{x1} = (V_{x1}/R_3) = (V_{out}/R_3) = I_{z1},\ V_{y2} = I_{z1}\,R_4 = V_{x2} = V_{out}(R_4/R_3) = KV_{out},\ K = (R_4/R_3) \tag{16.36a}$$

$$V_1\,(G_1 + G_2 + sC_1) - V_{in}\,G_1 - V_{out}\,G_2 - KV_{out}\,sC_1 = 0 \tag{16.36b}$$

$$(V_1 - V_{out})\,G_2 = sC_2\,V_{out} \rightarrow V_1 = V_{out}(sC_2 + G_2)/G_2 \tag{16.36c}$$



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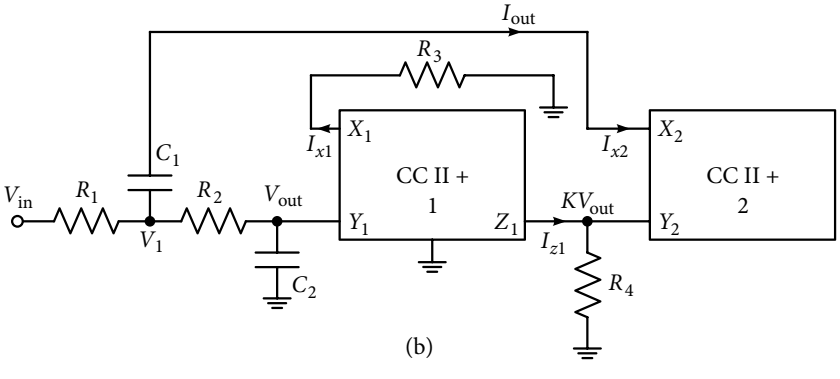

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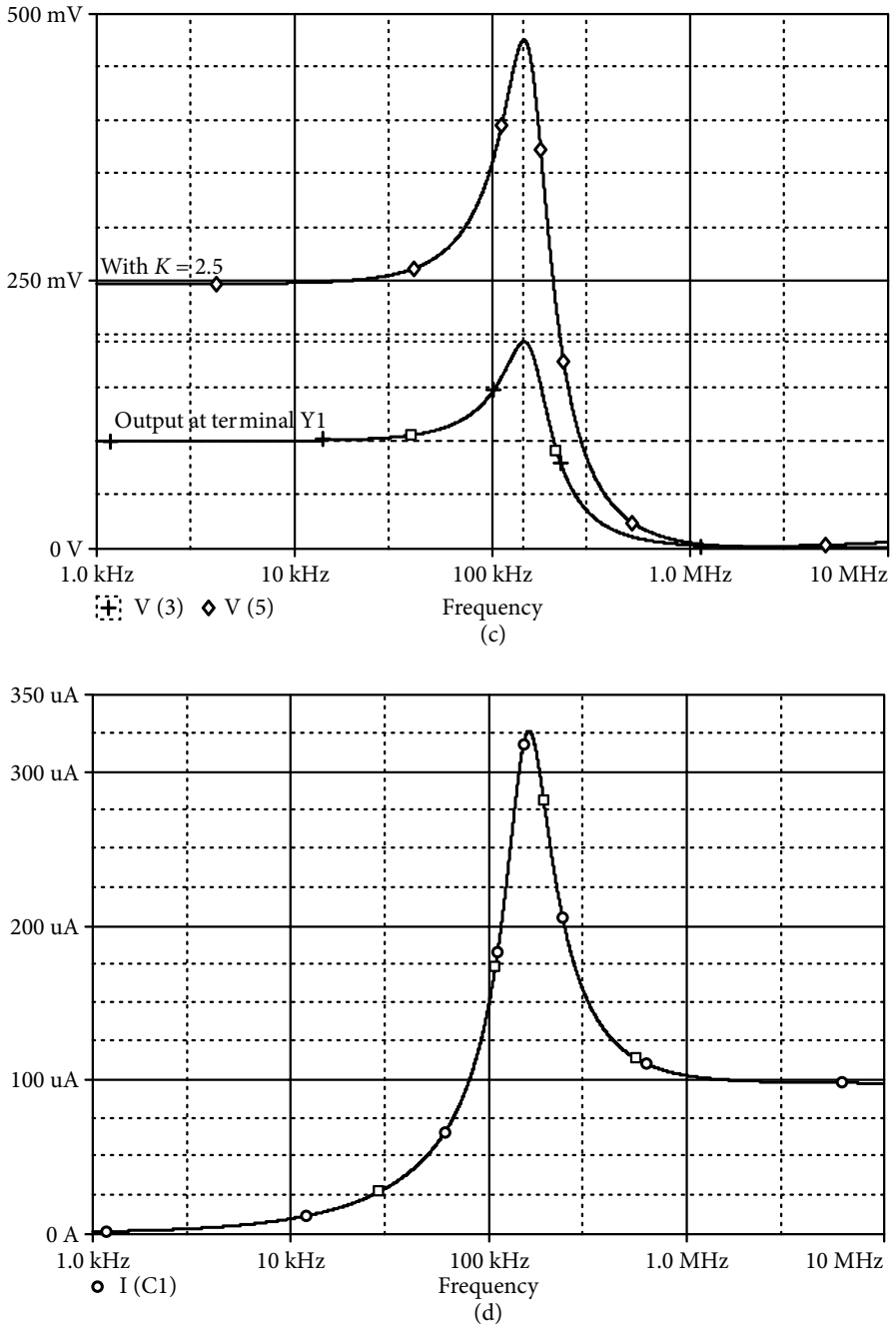

Figure 16.10 (a) Sallen–Key low pass OA-RC filter; (b) its CC based VM and CM version. (c) Voltage-mode low pass responses. (d) Current mode high pass response.

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Voltage ratio transfer function of the LPF is obtained as:

$$(V_{out}/V_{in}) = (1/R_1R_2C_1C_2)/D(s) \tag{16.37}$$

$$D(s) = s^2 + s\left\{\frac{1}{R_1C_1} + \frac{1}{R_2C_2} + (1-K)\frac{1}{R_2C_2}\right\} + \frac{1}{R_1R_2C_1C_2} \tag{16.38}$$

The circuit also provides a mixed mode HP voltage–current transfer function:

$$(I_{out}/V_{in}) = (s^2/R_1)/D(s) \tag{16.39}$$

Second-order filter parameters are obtained from equation (16.38) as:

$$\omega_o^2 = \frac{1}{R_1R_2C_1C_2} \text{ and } Q = \frac{(R_1R_2C_1C_2)^{0.5}}{\left\{\frac{1}{R_1C_1} + \frac{1}{R_2C_2} + (1-K)\frac{1}{R_2C_2}\right\}} \tag{16.40}$$

Example 16.4: Obtain the VM LP response of equation (16.37) and CM HP response with pole frequency of 1000 krad/s and pole-Q = 2.

Solution: From equation (16.40), selecting equal value capacitors $C_1 = C_2 = 1.0$ nF, we get $R_1 = 1$ kΩ, $R_2 = 1$ kΩ, and with $Q = 2$, K will be 2.5; hence, selected $R_3 = 1$ kΩ and $R_4 = 2.5$ kΩ. Using these element values in Figure 16.10(b), the circuit is simulated and the responses are shown in Figures 16.10(c)–(d). With $Q = 2$, it is expected that a peak in LP response would occur at $1000/(1 - 1/2 \times 2^2)^{0.5}$ krad/s or 148.8 kHz. For the simulated LP response, low frequency gain is unity and a peak gain of 1.93 occurs at 144.35 kHz; close to the design value. The direct effect of K being 2.5 is reflected in the LP response at the Y input of CC1 with low frequency gain as 2.5. Incidentally, the circuit also gives a HP response in the form of current through the capacitor C_1. For the CM HP response, a simulated peak gain of 2.08 occurs at 167.74 kHz as shown in Figure 16.10(d); with $Q = 2$, theoretical value of the peak frequency is evaluated as $1000/(1 - 1/(2 \times 2^2)^{0.5} = 1069$ krad/s = 168.9 kHz, which is very close to the simulated value.

For the conversion of OA-RC networks into CM ones, the *adjoint network* technique has been found suitable. Adjoint circuits are those circuits where response and excitation are exchanged while replacing each branch (source) by its adjoint branch; there is no effect on the passive elements. As an example of converting an OA-RC circuit to a CM circuit, the circuit of Figure 16.10(a) is converted to a CM second-order section. Figure 16.11(a) shows the converted CM circuit with inputs and outputs interchanged. Since in this circuit the second CC is not used, $K = 1$. Input terminal of the OA are the controlling terminals of the controlled voltage source, which gets converted into output terminals Z and ground, with current I_Z through it.

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Nodal current equations at nodes V_1, V_2 and X are as follows:

$$V_1(sC_1 + G_1 + G_2) - V_2G_2 = 0 \tag{16.41}$$

$$V_2(sC_2 + G_2) - V_1G_2 - I_x = 0 \tag{16.42}$$

$$V_1sC_1 - I_x + I_{in} = 0 \tag{16.43}$$

Solving equations (16.41)–(16.43), the following current ratio LP, BP and a combination of LP-BP transfer functions are obtained:

$$\frac{I(R_1)}{I_{in}} = \frac{-(G_1G_2)}{D(s)}, \frac{I(C_1)}{I_{in}} = \frac{-s(C_1G_2)}{D(s)}, \frac{I(R_2)}{I_{in}} = \frac{-s\left(C_1G_2\right)+(G_1G_2)}{D(s)}, \frac{I(C_2)}{I_{in}} = \frac{sC_2\left(sC_1+G_1+G_2\right)}{D(s)} \tag{16.44}$$

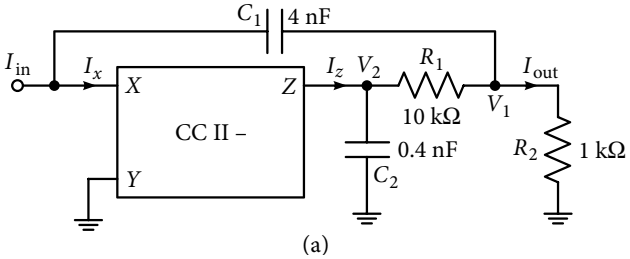
$$D(s) = s^2C_1C_2 + sC_2(G_1 + G_2) + G_1\,G_2 \tag{16.45}$$

Parameters of the second-order filters are:

$$\omega_o^2 = \frac{G_1G_2}{C_1C_2} \text{ and } Q = \frac{1}{(G_1+G_2)}\sqrt{\left(\frac{G_1G_2C_1}{C_2}\right)} \tag{16.46}$$

For selected values of the components as $R_1 = R_2 = 1$ kΩ, $C_1 = 4$ nF and $C_2 = 0.4$ nF, the design center frequency will be 125.7 kHz and Q will be 1.58.

Figure 16.11(b) shows the simulated LP response having a peak gain of 1.58 at 109.6 kHz, which gives a critical frequency of 122.5 kHz. Currents through other components simultaneously give HP and mixed BP responses. Center frequency of the BPF is 124.2 kHz with $Q = 1.52$. HP response shows a peak gain of 1.815 at a frequency of 135.03 kHz; this means an effective critical frequency of 124.3 kHz.



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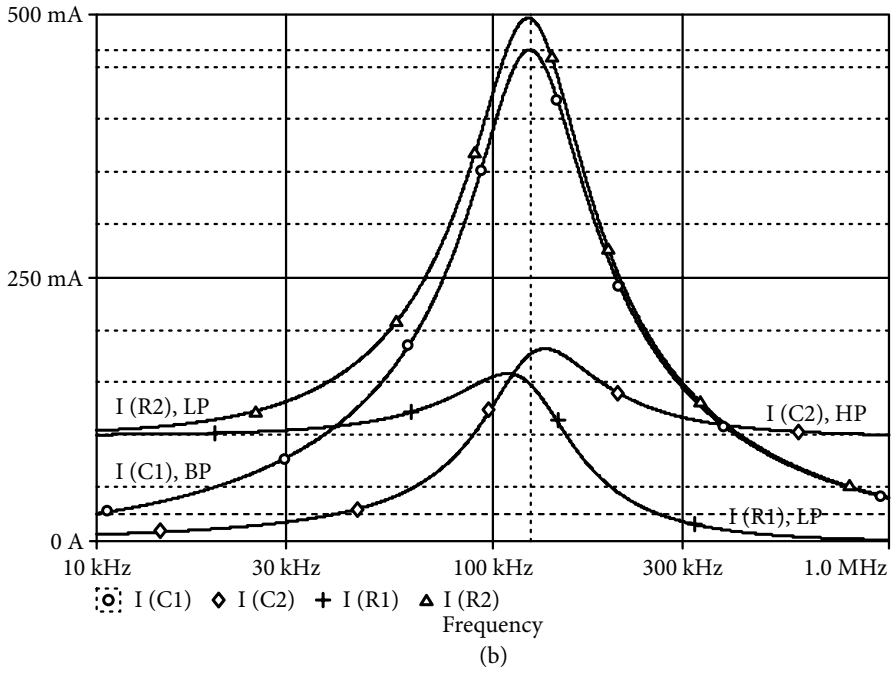

Figure 16.11 (a) CM second-order filter converted from Figure 16.10(a). (b) Simultaneous low pass, band pass and high pass, and mixed band pass responses from the circuit shown in Figure 16.11(a).

16.8 Biquads Using Single Current Conveyor

A general topology for obtaining biquads using single CC is shown in Figure 16.12(a). It shows three input currents I_1, I_2, and I_3. Different combinations of input currents and choice of elements have been given independently by several authors for such a configuration. For the general structure of Figure 16.12(a), the following transfer functions can be obtained while assuming the CC to be ideal.

$$I_{o1} = \{I_1(Y_1Y_2 + Y_1Y_3 + Y_2Y_3 + Y_3Y_4) + I_2Y_3\ Y_4 - I_3Y_1Y_4\}/D(s) \tag{16.47}$$

$$V_1 = \{I_2(Y_2 + Y_3) + I_3(Y_2 + Y_4)\}/D(s) \tag{16.48}$$

$$V_2 = \{I_3(Y_1 + Y_2 + Y_4) + I_2Y_2\}/D(s) \tag{16.49}$$

$$D(s) = Y_1Y_2 + Y_1Y_3 + Y_2Y_3 + Y_3Y_4 \tag{16.50}$$

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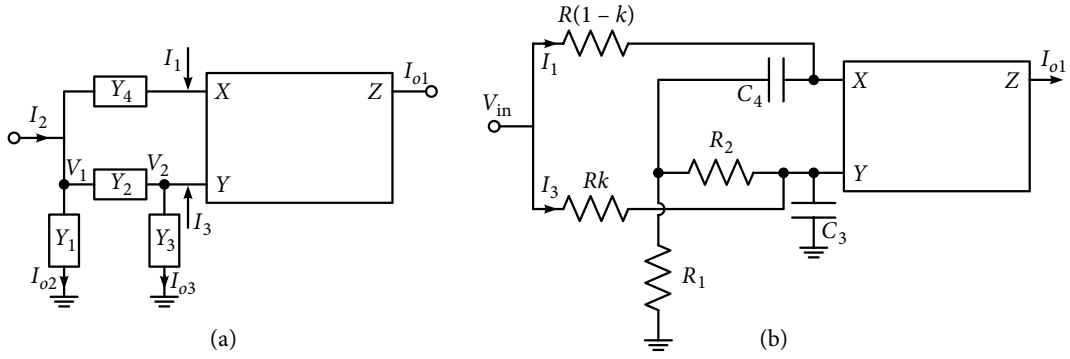

Figure 16.12 (a) A general C I C O biquad topology and (b) its implementation based on the feed-forward concept used in active filters for realizing notch and all pass response {With permission from Springer Nature}.

With reference to the choice of input currents by authors, Abuelmaatti [16.8] used only the input current I_2 with $I_1 = I_3 = 0$. For this choice, it is given that:

$$(I_{o1}/I_2) = \{Y_3\ Y_4/D_1(s)\} \text{ and } (V_2/I_2) = \{Y_2/D_1(s)\} \tag{16.51}$$

Selection of the elements as mentioned in Figure 16.12(b) gives an HP response at I_{o1}, and V_2 provides a VM LP response; it can be converted to a CM LP response using another CC utilizing the equipotential property between X and Y terminals. Additionally, the current through $Y_3(I_{o3} = V_2Y_3)$ yields a BP response with the following selection of elements.

$$Y_1 = G_1,\ Y_2 = G_2,\ Y_3 = sC_3, \text{ and } Y_4 = sC_4 \tag{16.52}$$

However, it may be noted that current through Y_3 (or Y_1) will be taken after un-grounding Y_3 (or Y_1) and using an extra CC with its Y terminal grounded.

Other choices in terms of selection of passive elements are also possible to get these responses.

In equation (16.47), with $I_2 = 0$, the negative term associated with I_3 provides notch and AP responses with elements as selected earlier in equation (16.52). Notch and AP responses are obtained with the following respective conditions in equation (16.53) and (16.54):

$$I_1\left\{\frac{C_3}{R_1}+\frac{C_3}{R_2}\right\} = I_3\frac{C_4}{R_1} \tag{16.53}$$

$$\left\{\frac{C_3}{R_1}+\frac{C_3}{R_2}\right\} - \frac{C_4}{R_1}\frac{I_3}{I_1} = -\left\{\frac{C_3}{R_1}+\frac{C_3}{R_2}\right\} \tag{16.54}$$

Obviously, the suggested configuration requires two input currents. Property of the equal voltage between X and Y terminals has been cleverly utilized by Anand Mohan [16.9] to

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circumvent it and uses only one input current. As shown in the circuit of Figure 16.12(b), input current division is obtained by two resistors having values of $R \times (1 - k)$ and Rk; here, $I_1 = kI_{in}$ and $I_3 = (1 - k) \times I_{in}$ while utilizing this technique. The transfer function for the circuit is obtained as:

$$\frac{I_{out}}{I_{in}} = k\frac{s^2C_3C_4 + s\left\{G_1\left(C_3 + C_4\right) - G_2\left(1-k\right)/k\right\} + G_1G_2}{s^2C_3C_4 + s\left\{G_1\left(C_3 + C_4\right)\right\} + G_1G_2} \tag{16.55a}$$

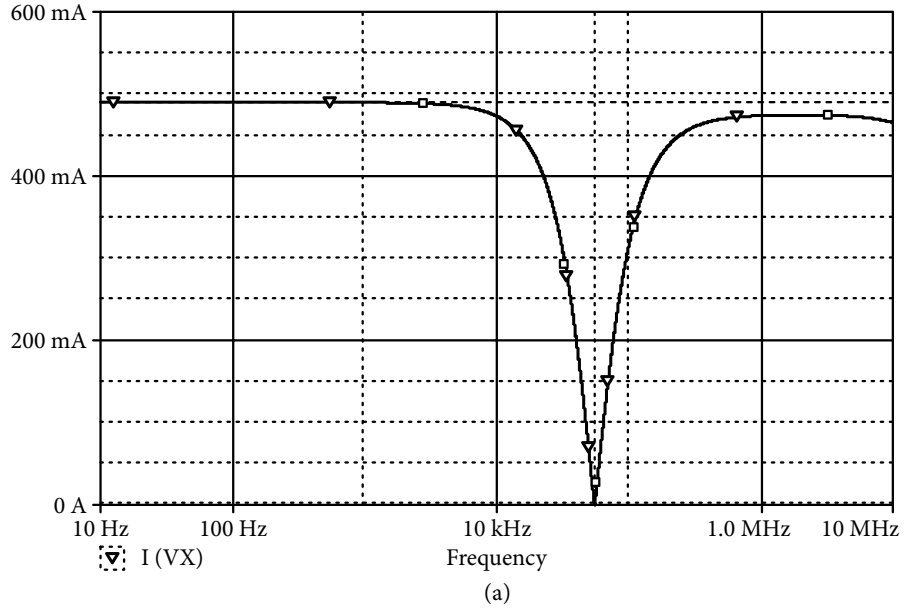
The transfer function in equation (16.55a) can realize symmetrical notch and AP responses. Parameters of the notch or APF are as follows:

$$\omega_o^2 = \frac{G_1G_2}{C_3C_4} \text{and} Q = \frac{1}{\left(C_3 + C_4\right)}\sqrt{\left(\frac{C_3C_4G_2}{G_1}\right)} \tag{16.55b}$$

Example 16.5: Design a notch filter using the structure shown in Figure 16.12(b), having one CC at the notch frequency of 350 krad/s (55.68 kHz). Convert it to an APF.

Solution: First, k is selected to be 0.5, for which current dividing resistors Rk and $R \times (1 - k)$ each are taken as 2 kΩ. With $I_3 = I_1$, and selecting $R_1 = R_2$, equation (16.53) gives $C_3 = 0.5C_4$. Finally, from equation (16.55b), the selected elements values for the notch frequency of 350 krad/s become:

$R_1 = R_2 = 2\ k\Omega$, $C_4 = 2$ nF, $C_3 = 1$ nF



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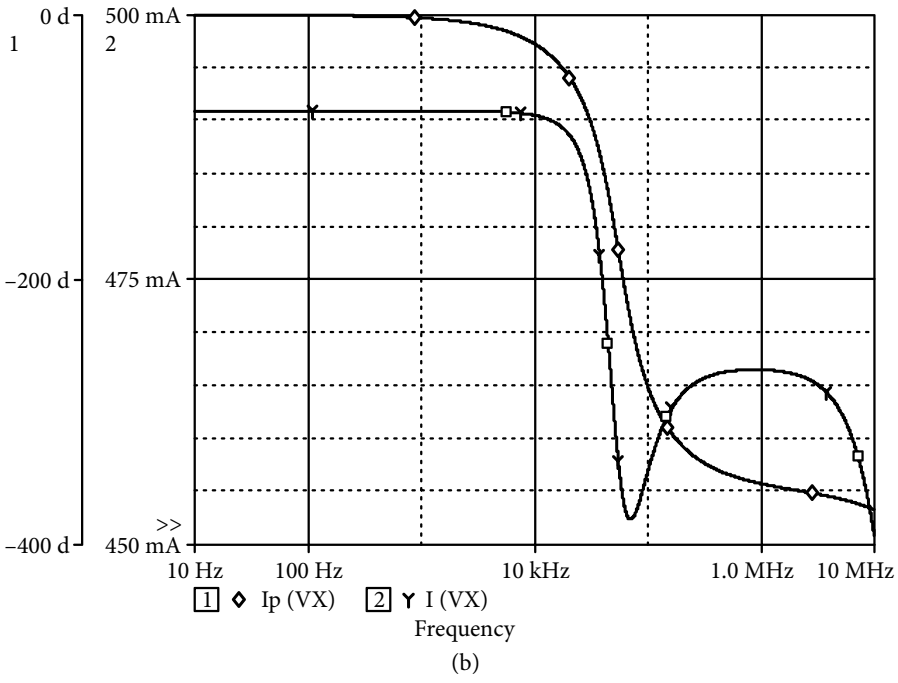

Figure 16.13 (a) CM notch filter response from Figure 16.12(b). (b) Magnitude and phase response of the CM all pass filter section of Figure 16.12(b).

The magnitude response of the simulated notch filter is shown in Figure 16.13(a), with notch at 56.08 kHz (352.5 krad/s) and attenuation of 55.1 dBs. Its gain at low frequency is 0.489 and gain at high frequencies is 0.474; k being 0.5.

To convert it to an APF, assuming the same current division with the same resistance values and the center frequency, equation (16.54) requires $C_4 = 4C_3$. For $C_3 = 1$ nF, the required values of the rest of the elements are $C_4 = 4$ nF and $R_1 = R_2 = 1.414$ kΩ. Using these elements, the simulated magnitude response of the APF is shown in Figure 16.13(b); variation in magnitude gain is from 0.491 to 0.452 only, when frequency was varied from 10 Hz to 10 MHz and the phase becomes 180° at a frequency of 55.47 kHz (348.67 krad/s) as shown in Figure 16.13(b).

16.9 Biquads Using Two or More Current Conveyors

A large number of biquadratic circuits using two or more CCs have been made available. Most of these depend on the tested ideas used in OA-RC active filter configurations. Some of these circuits are discussed in this section.

Figure 16.14(a) shows a multifunctional biquad given by Singh and Senani [16.10] which is based on the idea of well-known two-integrator loops, discussed in Section 8.2. CC1 and CC2

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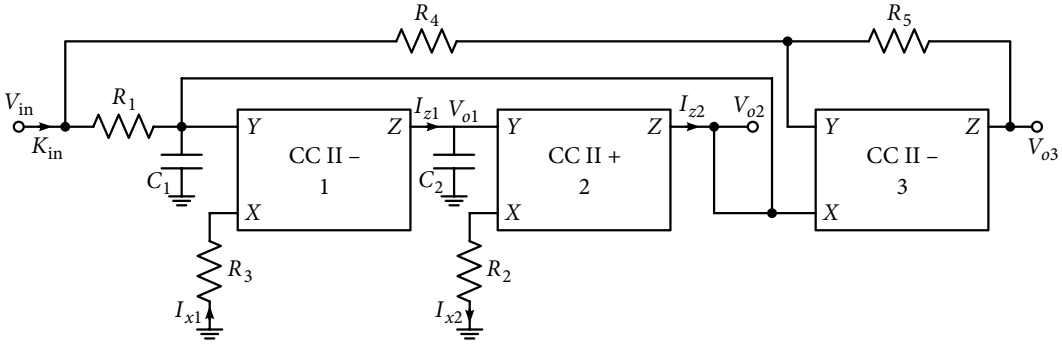
realize a lossless and lossy integrator respectively, using components R_1, C_1 and R_2, R_3 and C_2. LP and BP responses are available as V_{o1} and V_{o2}, respectively, and a notch or AP responses are obtained by subtracting the band pass output V_{o2} from the input V_{in} through CC3 and resistances R_4, R_5. In Figure 16.14(a), current–voltage relations are:

$$V_{x1} = V_{y1} = V_{o2} = I_{x1}R_3 \text{ and } I_{z1} = I_{x1} = V_{o1}sC_2 \tag{16.56a}$$

$$V_{x2} = V_{y2} = V_{o1} = I_{x2}R_2 \text{ and } I_{z2} = I_{x2} \tag{16.56b}$$



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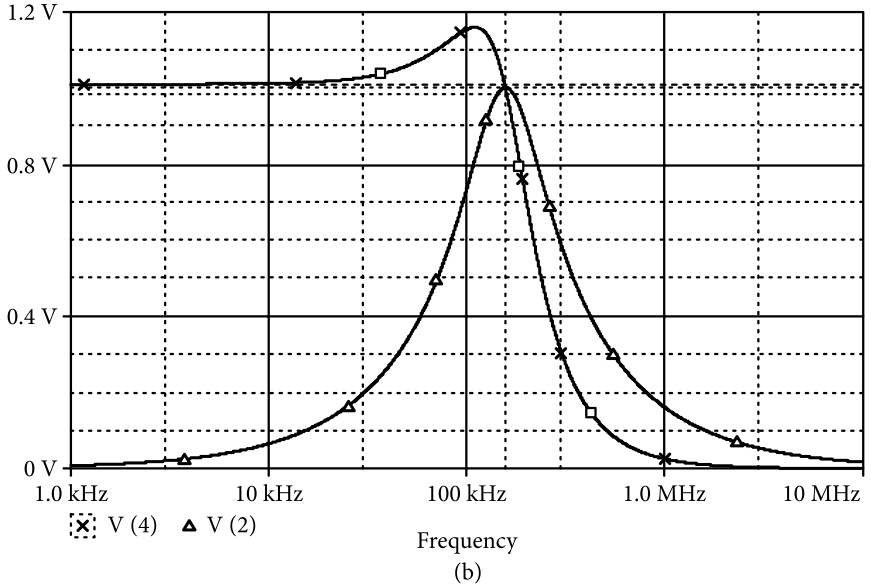

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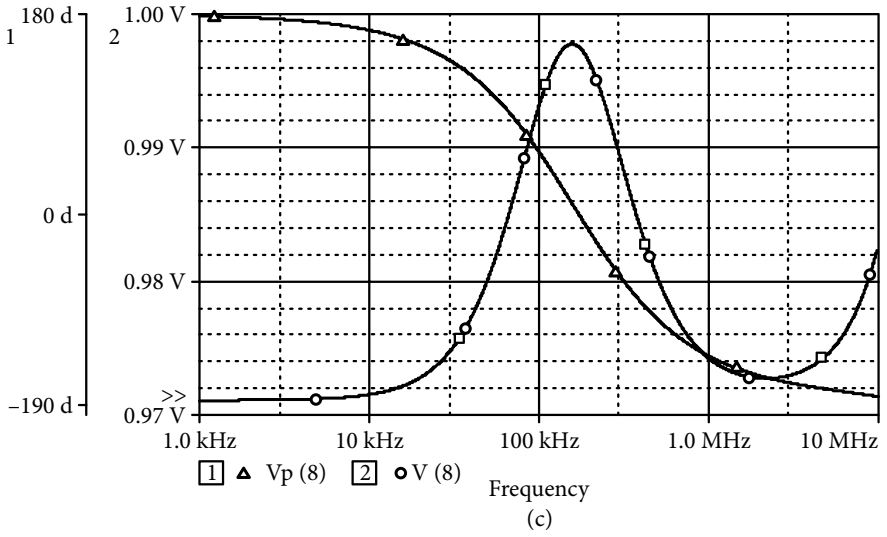

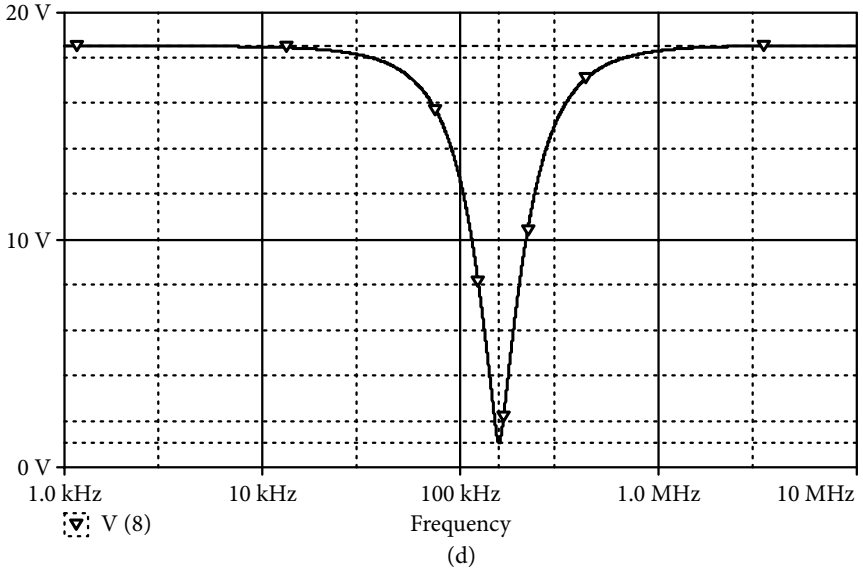

Figure 16.14 (a) Multi-function bi quad given by Singh and Senani {With permission from Springer Nature}. (b) Low pass and band pass responses using two-integrator loops and a summer for Example 16.6. (c) Magnitude and phase response of the all pass filter of Figure 16.14(a). (d) Notch filter response from the general biquad of Figure 16.14(a).

Nodal equation at terminal Y of CCII-1 will be:

$$V_{o2}\,(G_1 + sC_1) - I_{z2} - V_{\text{in}}G_1 = 0 \tag{16.57}$$

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Combining equations (16.56) and (16.57) gives the following LP and BP transfer functions:

$$(V_{o1}/V_{in}) = (1/R_2R_3C_1C_2)/D(s) \tag{16.58}$$

$$(V_{o2}/V_{in}) = (s/R_1C_1)/D(s) \tag{16.59}$$

$$D(s) = s^2 + \frac{s}{R_1C_1} + \frac{1}{R_2R_3C_1C_2} \tag{16.60}$$

From equation (16.60), expressions of the pole frequency and pole-Q are:

$$\omega_o^2 = \frac{1}{R_2R_3C_1C_2} \text{ and } Q = R_1\left(\frac{C_1}{R_2R_3C_2}\right)^{0.5} \tag{16.61}$$

To find the expression for output V_{o3}, the concerned relations are:

$$V_{x3} = V_{y3},\ I_{x3} = Iz_3 \text{ and } (V_{o2} - V_{in})\ G_4 + (V_{o2} - V_{o3})\ G_5 = 0 \tag{16.62}$$

Substituting V_{o2} from equation (16.59) in equation (16.62) gives:

$$\frac{V_{o3}}{V_{in}} = \frac{R_5}{R_4}\frac{s^2 - s\dfrac{R_4}{R_1R_5C_1} + \dfrac{1}{R_2R_3C_1C_2}}{D(s)} \tag{16.63}$$

AP and notch filter responses are available from equation (16.63) with the following respective relations:

$$R_5 = R_4 \text{ and } R_5 \gg R_4 \tag{16.64}$$

It is easily observed that while getting a notch with the condition of equation (16.64), the overall gain will become high.

Example 16.6: Design a BPF using the circuit of Figure 16.14(a) for center frequency of 1000 krad/s (159.09 kHz) and pole-Q of unity. Extend the same to realize AP and notch responses as well.

Solution: Selecting $C_1 = C_2 = 1$ nF, equation (16.61) gives the value of $R_2 = R_3 = 1$ kΩ and for $Q = 1$, $R_1 = 1$ kΩ. Using these components in Figure 16.14(a), the simulated filter response is shown in Figure 16.14(b). Simulated center frequency and bandwidth are158.5 kHz and 158.7 kHz, resulting in $Q = 0.998$. For $Q = 1$, the obtained LP response shows a peak gain of 1.158 at a frequency of $f_{peak} = 110.37$ kHz. From the f_{peak} value, its 3 dB frequency will be $110.37/(1 - 1/2)^{0.5} = 156.11$ kHz; very close to the design value.

To get AP response, for a selected value of $R_4 = 1$ kΩ, from equation (16.64), $R_5 = 1$ kΩ. Figure 16.14(c) shows magnitude and phase responses of the APF. Variation in magnitude is only from 0.9977 V to 0.9711 V, and phase variation is very symmetrical from 180° to –180° with 0° of phase shift at 157.19 kHz.

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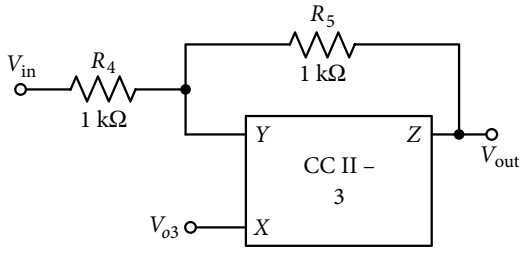
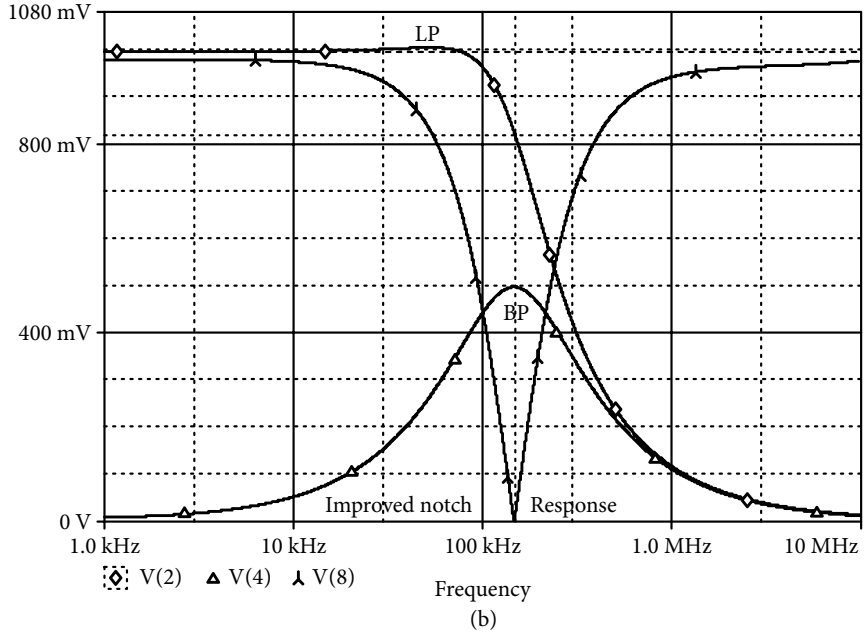
With R_4 = 1 kΩ and R_5 = 20 kΩ, notch appears at 157.46 kHz. However, at low and high frequencies, the gain magnitude is nearly 19.5, and at notch, its value is almost unity (0.976). In some cases, these gain levels may not be entirely desirable. Fortunately, there are other choices available; one such scheme is given here.

Figure 16.15(a) shows modified connections for CC3 of Figure 16.14(a) which replaces CC3 in Figure 16.14 (a). With R_4 = R_5 = 1 kΩ, the notch occurs at 223.56 kHz with attenuation of over 42 dBs. Rise in the value of notch frequency (and pole frequency of BP and LP as well) occurs even though other elements do not change. This means a certain feedback, which is confirmed by changing the values of R_4 or R_5.

As the new notch frequency is $\sqrt{2}$ times the design frequency of 1000 krad/s, capacitances C_1 and C_2 are modified to $\sqrt{2}$ nF. Simulated response is shown in Figure 16.15(b) with notch and center frequency of BPF as 159.2 kHz; though bandwidth of the BPF of the configuration with three CCs is still 223.2 kHz



(a)



(b)

Figure 16.15 (a) Modification in the circuit of Figure 16.14(a) for getting better notch, and (b) its responses.

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Different type of filter responses has been made available by Chang [16.11], who has given five biquadratic filter circuits employing four CCs and only grounded capacitors. Development of these circuits involve either of the following schemes: (i) connecting a grounded capacitor with a simulated lossless FI (floating inductance), (ii) using the idea of a KHN (Kerwin–Huelsman–Newcomb) biquad in which two integrator circuits are used to obtain LP and BP responses and (iii) use of a simulated GI (grounded inductance) shunted by a grounded capacitor multiplier. While simulating inductance, a practiced scheme is to first convert voltage to current and then re-convert the current to voltage. Figure 16.16(a) shows one of these circuits which is based on simulating FI using the same idea. The circuit can realize LP, BP and a notch response through simulating FI between terminals A and B.

Voltage V_{x1} being equal to V_{y1} (or at terminal A) and voltage V_{x3} being equal to V_{y3} (or V_{z4} at terminal B) means that $(V_A - V_B)$ is the voltage across the resistor R_1. Current through R_1 gets integrated through CC3 and capacitor C_1. The resulting integrated voltage is again converted to current, employing CC2, CC4 and resistor R_2 in such a way that it flows in terminals A and B, simulating FI. Resistor R_3 and capacitor C_2 are added to complete the second-order section for which current–voltage relations are:

$$V_{x1} = V_{o1} = V_{y1},\ V_{x2} = V_{o2} = V_{y2},\ V_{x4} = V_{y4} = 0 \tag{16.65a}$$

$$(V_{\text{in}} - V_{o1})\ G_3 = -V_{o2}\ G_2 \tag{16.65b}$$

$$I_{z4} = V_{o3}\ sC_2,\ I_{x4} = -V_{o2}\ G_2 \rightarrow V_{o3} = -V_{o2}\ G_2/sC_2 \tag{16.65c}$$

$$I_{x3} = (V_{o3} - V_{o1})\ G_1,\ I_{z3} = V_{o2}\ sC_1 \tag{16.65d}$$

From the relations in equation (16.65), the obtained transfer functions for notch, BP and LP are:

$$V_{o1} = V_{\text{in}} G_3 (s^2 C_1 C_2 + G_1 G_2)/D(s) \tag{16.66}$$

$$V_{o2} = -V_{\text{in}} \left\{ \frac{sC_2 G_1 G_3}{D(s)} \right\} \tag{16.67}$$

$$V_{o3} = V_{\text{in}} G_1 G_2 G_3 / D(s) \tag{16.68}$$

$$D(s) = s^2 C_1 C_2 G_3 + sC_1 G_1 G_2 + G_1 G_2 G_3 \tag{16.69}$$

From equation (16.69), expressions of pole frequency and pole-Q are obtained as:

$$\omega_o = \sqrt{\left(\frac{G_1 G_2}{C_1 C_2} \right)},\ Q_o = \frac{1}{R_3} \sqrt{\left(\frac{C_2 R_1 R_2}{C_1} \right)} \tag{16.70}$$

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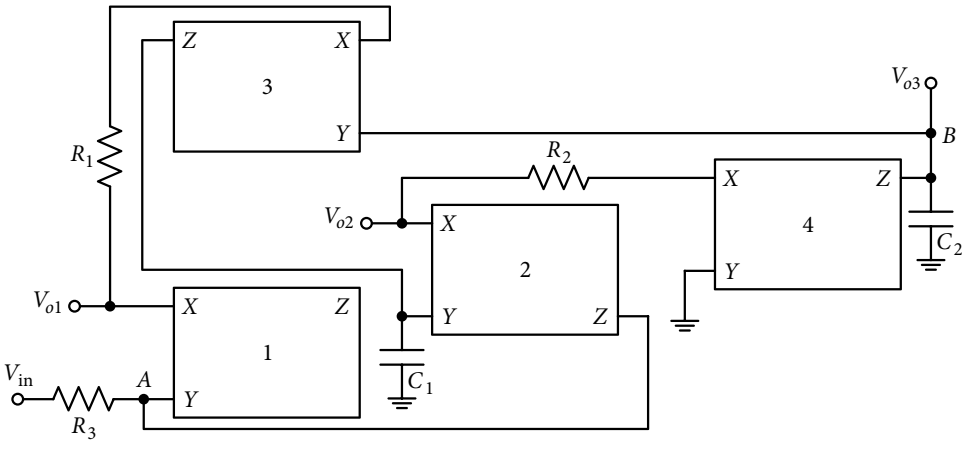
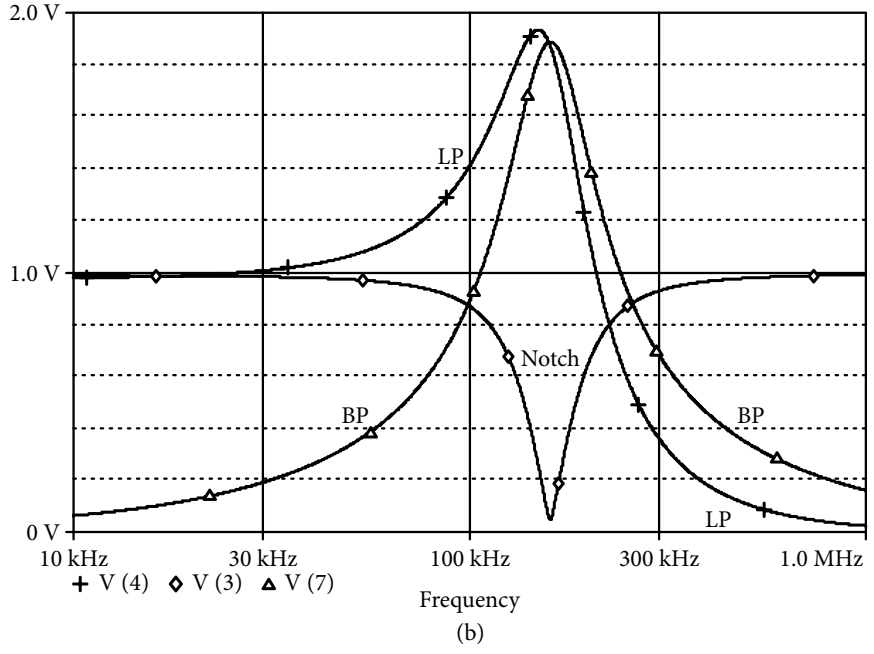


(a)



(b)

Figure 16.16 (a) One of the Chang's biquad topology using four CCs and grounded capacitors {With permission from Springer Nature} (b) its band pass, low pass and symmetrical notch responses.

Example 16.7: Design a BPF for a center frequency of 1000 krad/s and Q_o = 2, using the circuit of Figure 16.16(a). Also, show the response of the corresponding LP and notch.

Solution: From equation (16.70), selecting C_1 = C_2 = 0.1 nF, R_1 = R_2 will be 10 kΩ. For Q_o = 2, R_3 needs to be 5 kΩ. With these element values, the circuit is simulated and the

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responses are shown in Figure 16.16(b). Simulated ω_o = 1004.4 krad/s (159.789 kHz) and with a bandwidth of 83.57 kHz, realized Q_o = 1.91 for the BP. For the LP response, peak gain of 1.93 occurs at 148.39 kHz, which corresponds to $\omega_{oLP} = 148.39/(1 - 1/2 \times 1.93^2) = 159.48$ kHz. Notch frequency is 159.63 kHz (1003.38 krad/s) with attenuation of 26.3 dBs.

16.10 Inductance Simulation Using Current Conveyors

In most circuits, it is the inductance which has been attended to the most for well-known reasons. Inductance needs to be simulated in the grounded as well as in the floating form. Figure 16.17(a) shows a circuit, wherein direction of currents is shown according to the sign of CCII; expression of the voltage V_{y2} is written as:

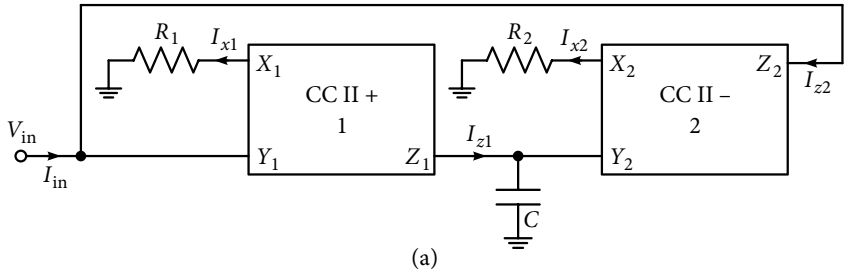
$$V_{y2} = V_{x2} = I_{x2} R_2 = I_{z2} R_2 = I_{in} R_2$$

$$V_{y2} = \frac{I_{z1}}{sC} = \frac{I_{x1}}{sC} = \frac{V_{x1}}{sCR_1} = \frac{V_{y1}}{sCR_1} = \frac{V_{in}}{sCR_1}$$

It gives the expression for simulated inductance as:

$$L_{sim} = CR_1 R_2 \tag{16.71}$$

Simulated GI as obtained in equation (16.71) depends on the same idea of voltage to current conversion and current to voltage conversion, which has been used for simulating FI by a number of authors. In this case, I_{in} is converted to V_{y2} using R_1 and C; then V_{x2} drives a current I_{z2} using R_2 and again to voltage V_{x1} using R_1.



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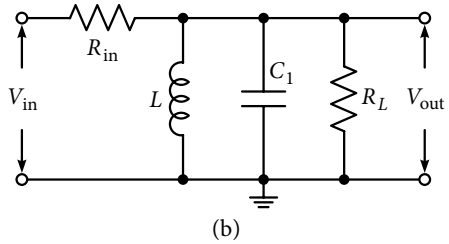

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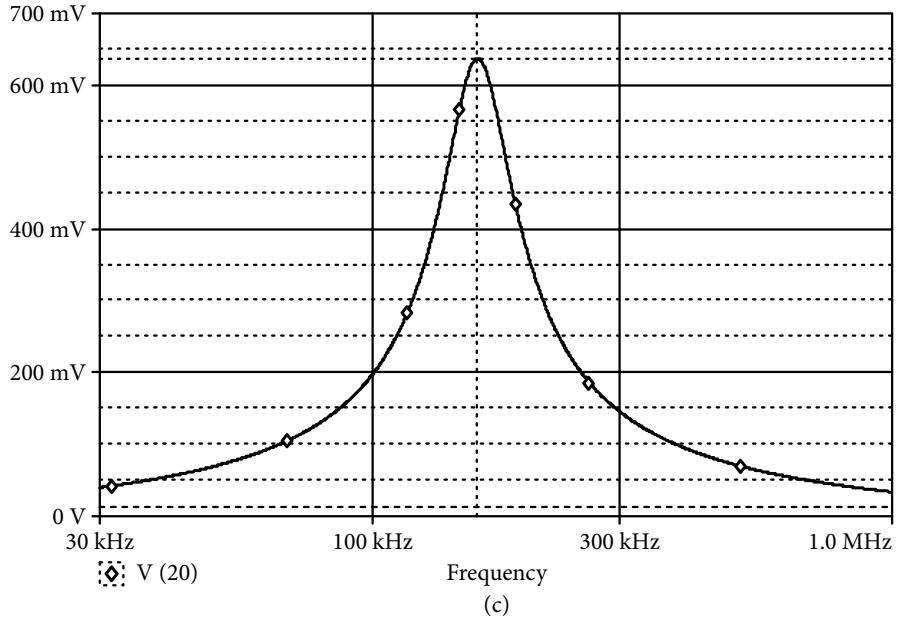

Figure 16.17 (a) Grounded impedance simulator using CCs (b) passive RLC band pass circuit for testing the simulated grounded inductance and (c) its simulated response for Example 16.7.

Example 16.7: Verify the simulation of the grounded inductance of Figure 16.17(a).

Solution: Figure 16.17(b) shows a passive RLC circuit which realizes BP response. Its transfer function is obtained as:

$$\frac{V_{\text{in}}}{V_{\text{out}}} = \frac{\left(s / C_1 R_L\right)}{s^2 + s\left(\frac{R_{\text{in}} + R_L}{C_1 R_{\text{in}} R_L}\right) + \frac{1}{LC_1}} \tag{16.72}$$

For the test circuit, center frequency and pole-Q expressions are:

$$\omega_o = \frac{1}{\sqrt{LC_1}} Q_o = \frac{R_{\text{in}} R_L}{R_{\text{in}} + R_L} \sqrt{\left(\frac{C_1}{L}\right)} \tag{16.73}$$

For ω_o = 1000 krad/s, if selected C_1 = 0.4 nF, the required value of the inductance to be simulated will be 2.5 mH. Using equation (16.71), inductance is simulated with $R_1 = R_2$ = 5 kΩ and C = 0.1 nF. Again, using equation (16.73), if values of R_{in} and R_L are 50 kΩ and 100 kΩ, respectively, it gives Q_o = 3. Figure 16.17(c) shows the simulated response with $\omega_o = 2\pi \times$ 159.84 = 1002.8 krad/s. Its bandwidth is 49.9 kHz giving simulated Q_o = 3.2.

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Figure 16.18(a) shows a scheme given by Toumazou and Lidgey [16.12] for general floating impedance simulation. Here input voltages are buffered by CC1 and CC2, which also converts voltages to currents using impedance Z_1. Next the currents get converted to voltages using impedances Z_2 and Z_3. Lastly, conveyors CC3 and CC4 convert these voltages to current using impedance Z_4; these conveyors also provide path for the input currents. With CC1 and CC3 as negative and CC2 and CC4 as positive, current–voltage relations are as follows:

$$V_{x1} = V_{y1} = V_1,\ V_{x2} = V_{y2} = V_2$$

$$I_{x1} = -I_{x2} = (V_2 - V_1)Y_1 = I_{z1},\ I_{z2} = I_{x2} = -(V_2 - V_1)\ Y_1$$

$$V_{y3} = -I_{z1}Z_2 = -(V_2 - V_1)\ Y_1Z_2 = V_{x3},\ V_{y4} = -I_{z2}Z_3 = (V_2 - V_1)\ Y_1Z_3 = V_{x4}$$

$$I_{x3} = I_{x4} = (V_{x3} - V_{x4})Y_4 = -\{(V_2 - V_1)Y_1Y_4\ (Z_2 + Z_3)\} = I_{z3} = I_{z4} = -I_2 = I_1 \tag{16.74}$$

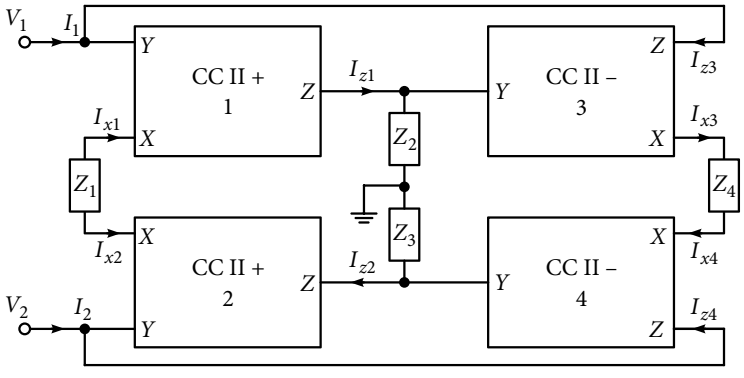
Hence, expression of the realized floating impedance from equation (16.74) is given as:

$$Z_1Z_4/(Z_2 + Z_3) \tag{16.75a}$$

Choice of elements for these impedances can give inductance, FDNR (frequency dependant negative resistor) or, can function as a capacitance multiplier as well.

Few circuits are available using the idea behind this configuration. Figure 16.18(b) shows one such circuit given by Singh [16.13]. For the circuit shown in Figure 16.18(b), the realized floating inductance expression will be as given below:

$$R_1R_3C_2 \tag{16.75b}$$



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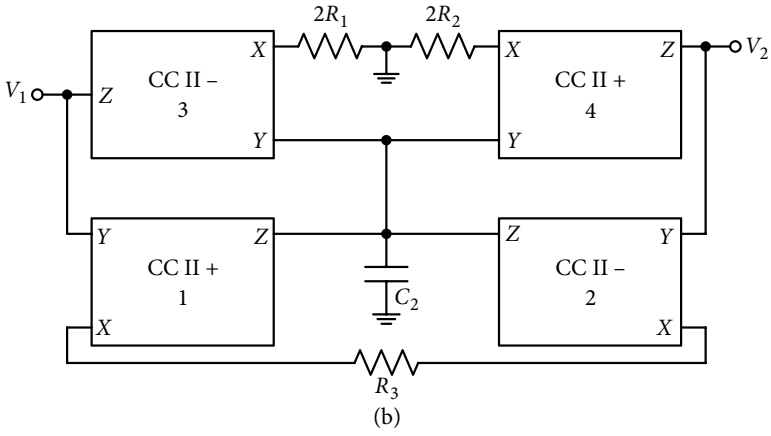


(b)

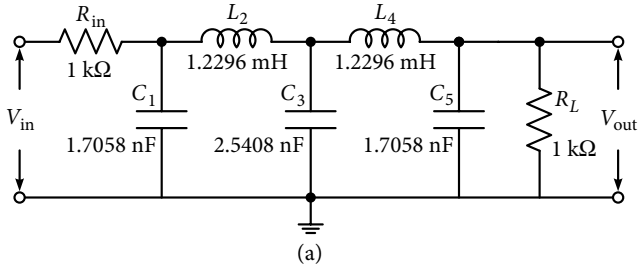
Figure 16.18 (a) A generalized scheme for realizing floating impedance [16.12] {With permission from Springer Nature}, and (b) floating inductance simulators by Singh [16.13] {With permission from Springer Nature}.

Example 16.9: Realize a fifth-order Chebyshev filter having maximum 0.5 dB pass band ripple with pass band edge frequency of 1000 krad/s using the FI simulator of Figure 16.18(b).

Solution: Fifth-order Chebyshev passive filter structure is shown elsewhere as well but repeated in Figure 16.19(a). For the given specifications, frequency scaling factor will be 1000 krad/s and if the impedance scaling factor of 1 kΩ is used, component values will become:

$$R_{in} = R_L = 1\ \text{k}\Omega,\ C_1 = C_5 = 1.7058\ \text{nF},\ C_3 = 2.5408\ \text{nF and}\ L_2 = L_4 = 1.2296\ \text{mH}$$

FIs are simulated using the circuit in Figure 16.18(b). For both the inductors, $2R_1$ = 2.459 kΩ = $2R_2$, R_3 = 1 kΩ and C_2 = 1 nF; the complete circuit is shown in Figure 16.19(b). The simulated magnitude response of the filter is shown in Figure 16.19(c) with a pass band edge frequency of 157.29 kHz (988.68 krad/s) with maximum ripple width of 0.4917 dB.



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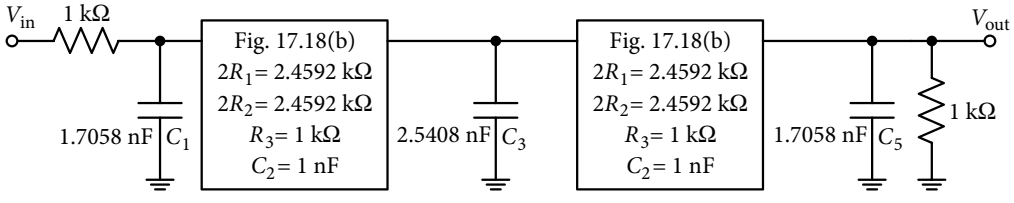

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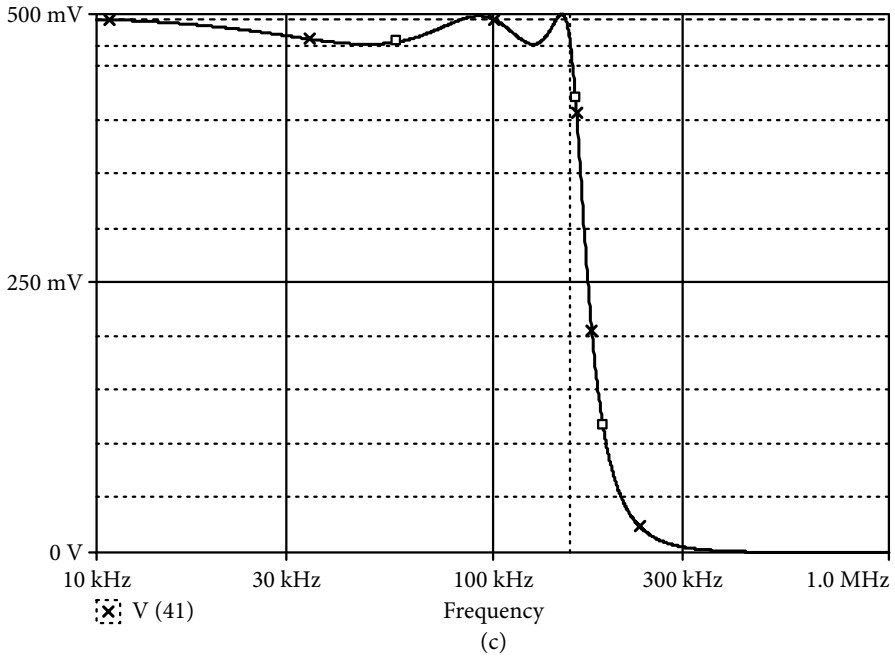

Figure 16.19 (a) Fifth-order Chebyshev passive filter. (b) Chebyshev filter using the floating inductor simulator circuit shown in Figure 16.18(b). (c) its simulated response while using four CC circuit of Figure 16.18(b).

Non-ideal inductance has also been simulated using non-ideal gyrators [16.14]. Figure 16.20(a) and (c) show two such circuits. For the circuit in Figure 16.20(a):

$$V_{y1} = V_{x1} = \left(I_{\text{in}} - I_{z2}\right)Z_2,\ V_{y2} = V_{x2} = 0,\ I_{x2} = I_{z2} = \frac{V_{x1}}{Z_3} \rightarrow I_{z2} = \frac{Z_2}{Z_2 + Z_3} I_{\text{in}} \tag{16.76}$$

$$V_{\text{in}} = V_{y1} + \left(I_{\text{in}} - I_{z2}\right)Z_1 \rightarrow \frac{V_{\text{in}}}{I_{\text{in}}} = Z_3 \frac{Z_1 + Z_2}{Z_2 + Z_3} \tag{16.77}$$

For equation (16.77), equivalent of input impedance results in a parallel combination of a few components. For example, for $Z_1 = R_1$, $Z_2 = (1/sC_2)$ and $Z_3 = R_3$, simulated equivalent circuit contains inductance $L = R_1R_3C_2$ as shown in Figure 16.20(b) in parallel with a series combination of R_1 and C_2. It is to be noted that both the conveyors are positive with I_{z2} going into it. Similarly, for the circuit shown in Figure 16.20(c), simulated inductance expression is the same for the same selection of components as that in Figure 16.20(b), and its equivalent circuit is shown in Figure 16.20(d).

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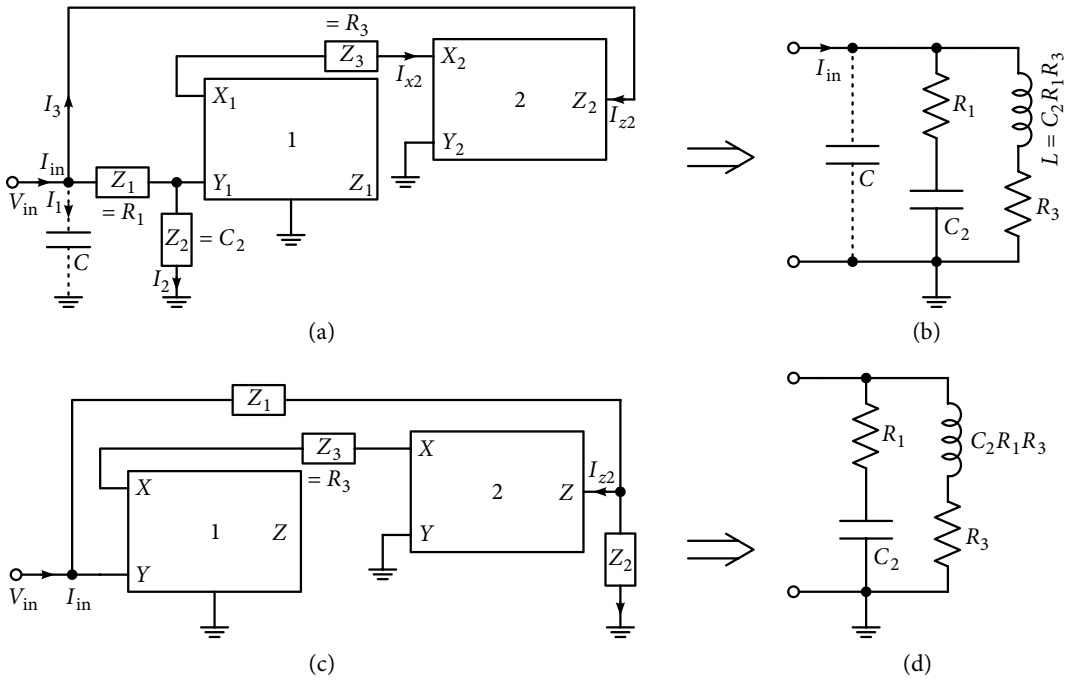

Figure 16.20 (a) and (c) Realizing non-ideal inductor, [16.14]{With permission from Springer Nature} and (b) and (d) are their simulated equivalents.

Example 16.10: Obtain a biquad using the non-ideal inductance simulator of Figure 16.20(a) with a pole frequency of 250 krad/s.

Solution: If a capacitor C is connected in parallel with the non-ideal inductor as shown with dotted lines in Figure 16.20(a), LP, BP and HP transfer functions are obtained. In Figure 16.20(b), the following relations can be easily written:

$$I_{in} = I_1 + I_2 + I_3 \tag{16.78}$$

$$I_1 = V_{in}\, sC,\ I_2 = V_{in}/\{R_1 + (1/(sC_2)\},\ I_3 = sC_2\ V_{in}/(R_3 + sC_2\ R_1\ R_3) \tag{16.79}$$

Combining equations (16.78)–(16.79), the following transfer functions are obtained:

$$\frac{I_2}{I_{in}} = \frac{I(R_1)}{I_{in}} = \frac{R_3C_2s}{D(s)},\ \frac{I_3}{I_{in}} = \frac{I(R_3)}{I_{in}} = \frac{1}{D(s)} \tag{16.80}$$

$$D(s) = R_1R_3C_2Cs^2 + R_3(C_2 + C)s + 1 \tag{16.81}$$

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Pole frequency and pole-Q expressions are:

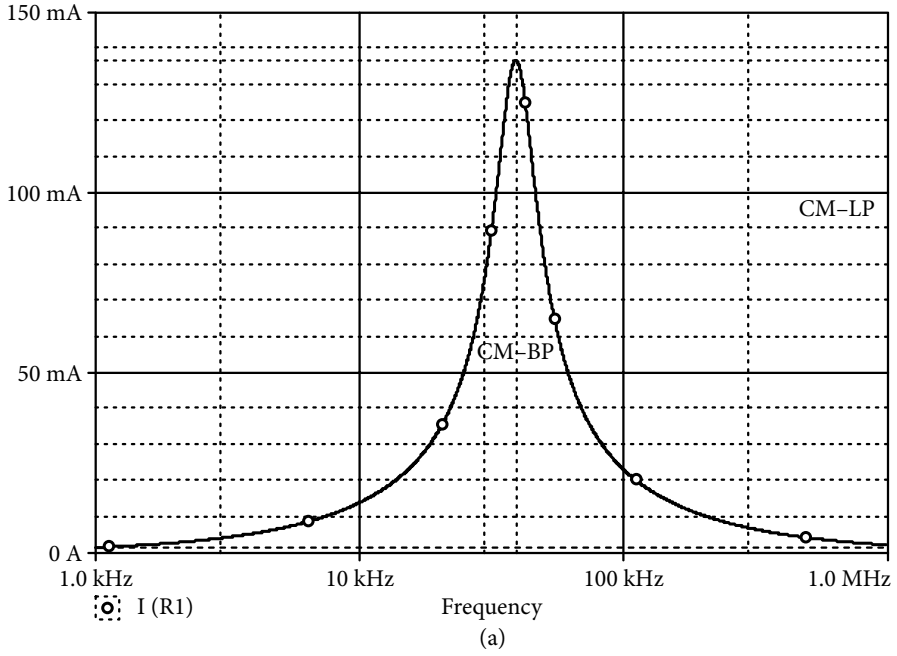
$$\omega_o = \frac{1}{\sqrt{\left(R_1 R_3 C_2 C\right)}},\ Q = \frac{\sqrt{\left(R_1 R_3 C_2 C\right)}}{R_3 (C_2 + C)} \tag{16.82}$$

Selected component for the center frequency of 250 krad/s, values are:

R_1 = 64 kΩ, R_3 = 1.0 kΩ, C_2 = 0.2 nF and C =1.25 nF

Theoretical value of pole-Q from equation (16.82) will be 2.758.

Simulated responses are shown in Figure 16.21(a)–(b). Center frequency of the CM BPF is 39.355 kHz (247.37 krad/s) and with a bandwidth of 14.526 kHz, Q = 2.706; mid-band gain is 0.136. For the CM LP response, peak occurs at 37.804 kHz, with a peak gain of 2.748 (almost equal to Q) and CM HP response has a peak gain of 2.872 at a frequency of 40.703 kHz. Deviations in the pole frequency of LP and HP are justified with the value of Q very nearly equal to 2.748 and 2.872, respectively.



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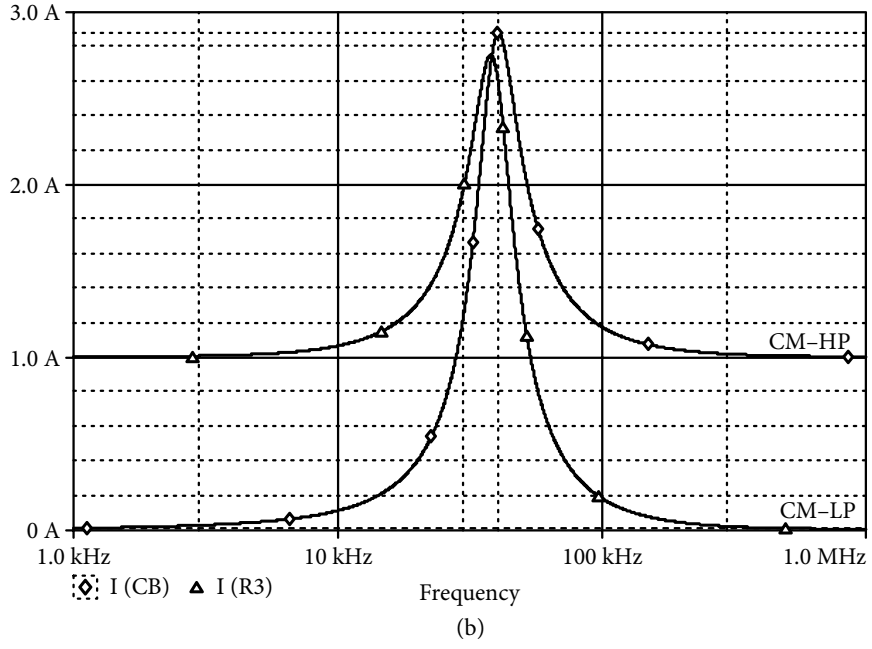

Figure 16.21 (a) CM band pass and (b) high pass and low pass responses from the circuit of Figure 16.20(a).

16.11 Application of CDTA

Recently, current differencing transconductance (CDTA) has been gaining attention for the realization of CM filters. Its behavioral model and symbol for double input double output (DIDO) are shown in block form structure in Figure 16.22(a) and (b) [16.15]. Its transconductance g_m can be controlled by difference current sources and an OTA as shown in Figure 16.22(c) [16.15] with an external load resistance. Though the difference between the input currents I_p and I_n can be multiplied by an electronically controllable gain factor b, which may be more than one, but generally 'b' is equal to unity. Voltage developed across grounded impedance gets converted to current I_x through transconductance. Behavior of the CDTA model can be expressed by the following matrix:

$$\begin{bmatrix} I_x \\ I_z \\ V_p \\ V_n \end{bmatrix} = \begin{bmatrix} 0 & 0 & b & -b \\ \pm g_m & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_z \\ V_x \\ I_p \\ I_n \end{bmatrix} \tag{16.83}$$

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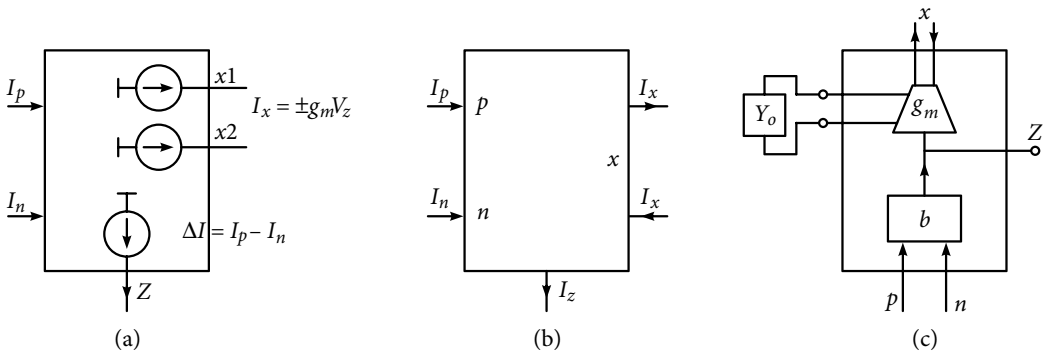

Figure 16.22 (a) Behavioral model of a CDTA and (b) symbol of DIDO type of CDTA. (c) CDTA element with the possibility to choose transconductance by an external admittance Y_o.

A number of options are available for the realization of CDTA. One of the options is through the use of current conveyors and OTAs. Shown in Figure 16.23, two CCII+ are used to implement differential current source and the output current is obtained through the OTA [16.16]. More than one OTA may be used to get as many output currents.

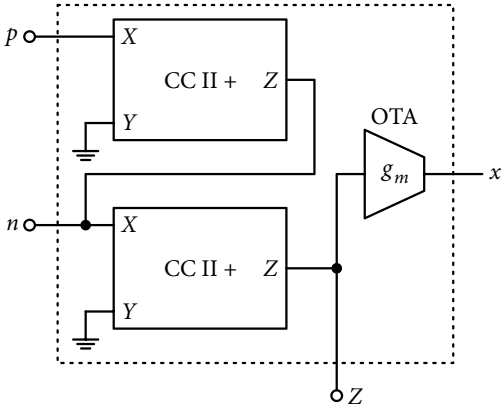

Figure 16.23 Implementation of CDTA using current conveyors and OTA.

Some simple applications of CDTAs are shown in Figure 16.24 [16.15]. Figure 16.24(a) shows a difference current ($I_p - I_n$) -controlled current source, wherein the current gain K_I equals ($g_m Z$); Z being an externally connected impedance. Obviously, depending upon the nature of Z, current gain will be linear or frequency dependent. If Z is removed, the CDTA becomes a current operational amplifier (COA). A dual input, duel output COA is shown in Figure 16.24(b). Finite current gain is obtainable from a COA by applying negative feedback, through a current divider as shown in Figure 16.24(c).The current gain is independent of g_m, and depends on the ratio of the elements of the external potential divider.

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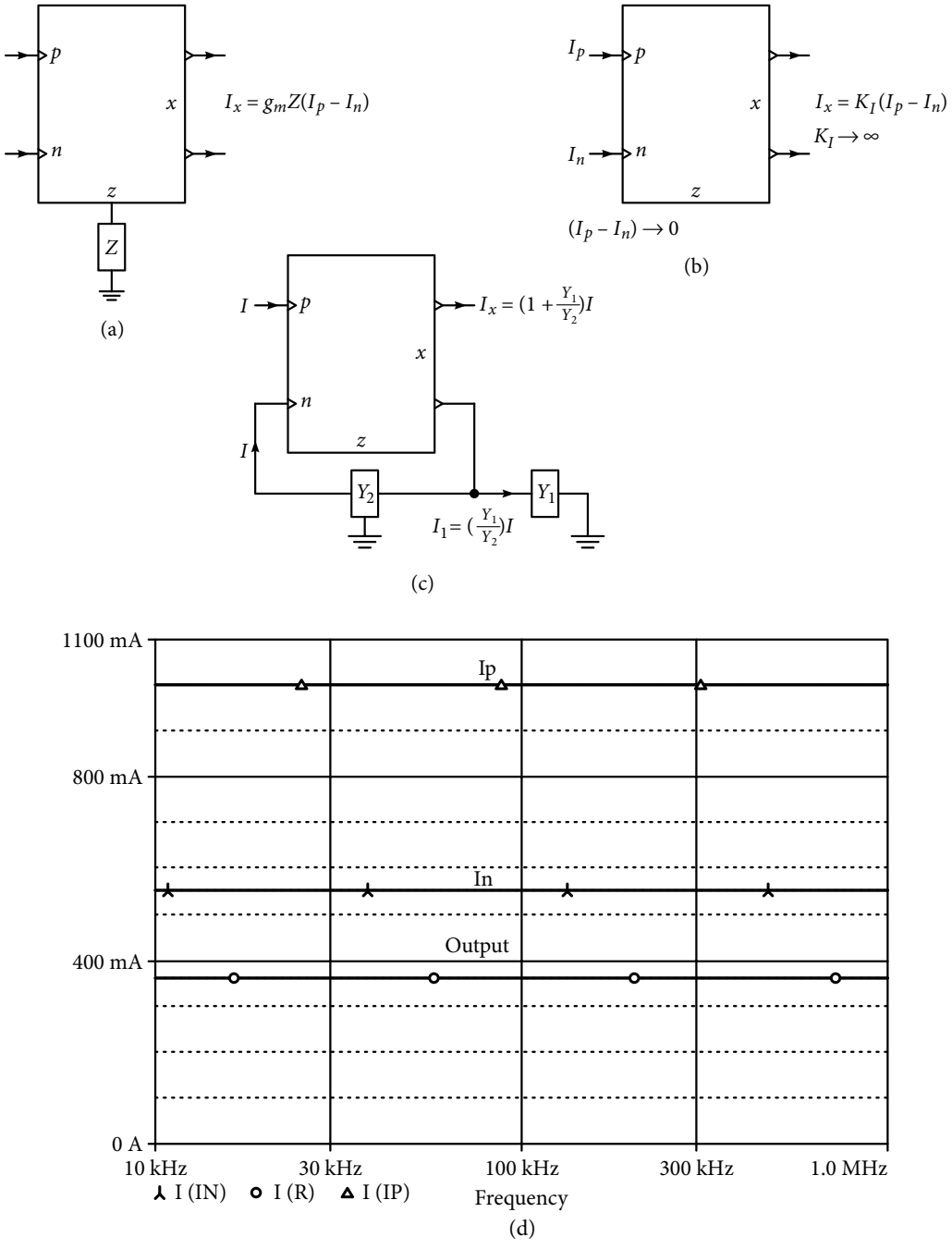

Figure 16.24 CDTA as (a) a difference current controlled current amplifier, (b) COA and (c) finite current gain amplifier using negative feedback. (d) Input and output currents of the CCCA using Figure 16.24(c).

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As a simple example, let I_p = 1 mA, I_n = 0.55 mA, g_m = 0.8 mA/V; then, with Z being a resistance of 1.0 kΩ, the theoretical value of output current will be 0.36 mA. Figure 16.24(d) shows PSpice simulated input and output currents confirming the working of the circuit as a current controlled current amplifier (CCCA).

If a grounded capacitor is used as the impedance Z, CDTA becomes an ideal integrator; it becomes a lossy integrator by connecting a resistance in parallel with the capacitor.

16.11.1 Inductance simulation using CDTAs

Inductance simulation technique is one of the most often used techniques in active filter synthesis. To use this approach, grounded as well as the floating form of inductance simulator are needed. Figure 16.25(a) shows a circuit for the simulation of GI. With applied voltage V_{in}, output current from CDTA1 will be $g_{m1} V_{in}$.

It gives $V_{z2} = -(g_{m1} V_{in} b_2/sC_L)$, and with $I_{in} = -b_1 I_{n1}$:

$$I_{in} = g_{m1}\, V_{in}\, b_1\, g_{m2}\, b_2/sC_L \rightarrow (V_{in}/I_{in}) = sC_L/g_{m1}\, b_1\, g_{m2}\, b_2 \tag{16.84}$$

For $b_1 = b_2 = 1$, input impedance is that of an inductor with the inductance expression being $(C_L/g_{m1}g_{m2})$.

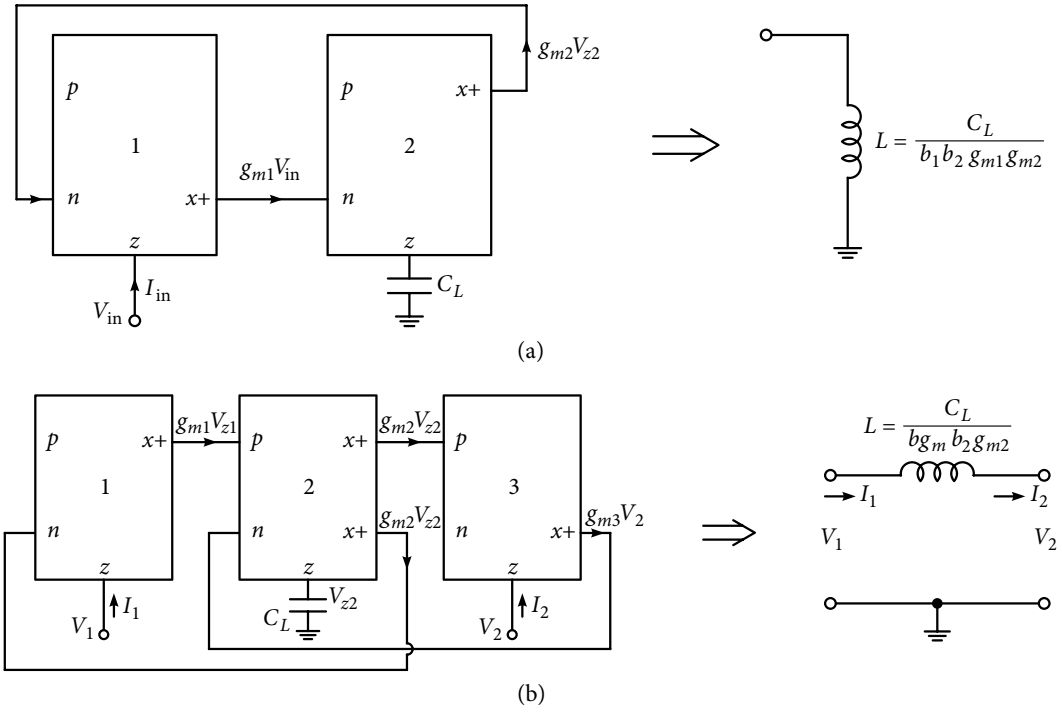

Figure 16.25 (a) Grounded inductance simulation using two CDTAs. (b) Floating inductance simulation using three CDTAs.

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Figure 16.25(b) shows a circuit simulating floating inductance [16.17]. Here current I_1, I_2 and V_{z2} are obtained as:

$$I_1 = b_1\, g_{m2}\, V_{z2},\ I_2 = b_3\, g_{m2}\, V_{z2} \text{ and } V_{z2} = b_2\, (g_{m1}\, V_1 - g_{m3}\, V_2)/(sC_L) \tag{16.85}$$

For $b_1 = b_3 = b$ and $g_{m1} = g_{m3} = g_m$

$$I_1 = I_2 = \frac{V_1 - V_2}{sL},\ \text{where}\, L = \frac{C_L}{bg_m b_2 g_{m2}} \tag{16.86}$$

Example 16.11: Use the GI of Figure 16.25(a) in the passive RLC filter of Figure 16.26(a), and test it for a center frequency of 100 krad/s and $Q = 2$.

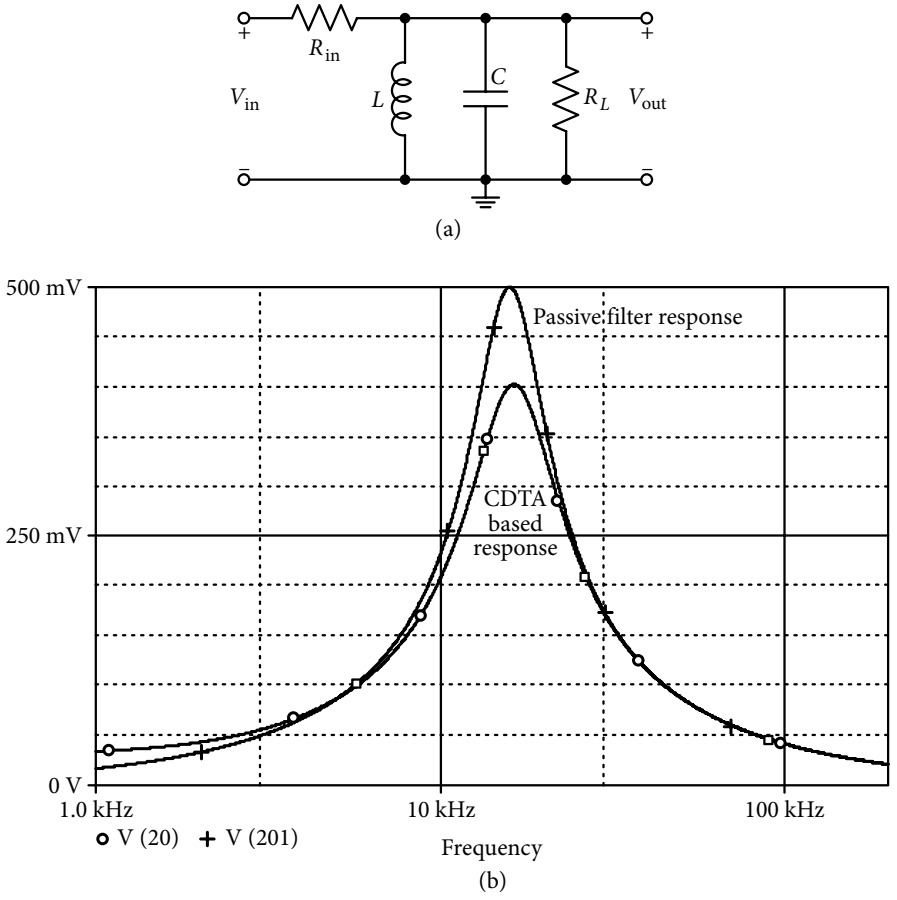

Figure 16.26 (a) A passive second-order band pass filter. (b) Response of the second-order band pass filter of Figure 16.26(a) and its active version using CDTA based grounded inductance.

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Solution: For the passive filter, expressions for the center frequency and pole-Q are:

$$\omega_o = (1/LC)^{0.5}, Q = \frac{R_L \times R_{in}}{R_L + R_{in}}\sqrt{(C/L)} \tag{16.87}$$

For ω_o = 100 krad/s, if C is selected as 10 nF, then the required value of inductance from equation (16.87), L = 10 mH. Inductance is realized with $g_{m1} = g_{m2}$ = 0.1 mA/V, C_L = 0.1 nF and if $R_L = R_{in}$, for Q = 2, $R_L = R_{in}$ = 4 kΩ. With these element values, passive RLC BPF, as well as its active version using CDTA based GI are simulated, and the responses are shown in Figure 16.26(b). Response for the passive filter is near ideal, whereas for the active filter ω_o = 102.86 krad/s and Q = 1.646.

16.11.2 Biquadratic circuits using CDTAs

A number of good performance second-order filter circuits are available in literature. Here, only two circuits and their important relations are given in brief. The circuit shown in Figure 16.27 is given by M. Dehran et al. [16.18], for which the current ratio transfer function are as follows:

$$\frac{I_{LP}}{I_{in}} = \frac{g_m/RC_1C_2}{D(s)}, \frac{I_{BP}}{I_{in}} = \frac{s/RC_1}{D(s)}, \frac{I_{HP}}{I_{in}} = \frac{s^2}{D(s)}, D(s) = s^2 + (s/RC_1) + g_m/RC_1C_2 \tag{16.88}$$

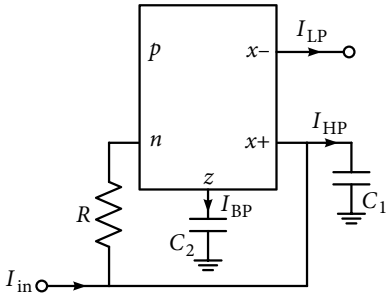

Figure 16.27 A biquad using a CDTA [16.18].

The circuit in Figure 16.28 is given by Bioleck and Biolkava [16.16], which is based on the Tow–Thomas biquad. Important expressions are as follows:

$$\frac{I_{x1}}{I_{in}} = \frac{s(\omega_o/Q)}{D(s)}, \frac{I_{x2}}{I_{in}} = \frac{\omega_o^2}{D(s)}, \frac{I_{c1}}{I_{in}} = \frac{s^2}{D(s)}, \frac{I_{c2}}{I_{in}} = \frac{s(G_{m1}\omega_o R/Q)}{D(s)}, \frac{I_R}{I_{in}} = \frac{s(\omega_o/Q)}{D(s)} \tag{16.89}$$

$$D(s) = s^2 + s(\omega_o/Q) + \omega_o^2, \omega_o^2 = \frac{G_{m1}G_{m2}}{C_1C_2}, Q = R\sqrt{(G_{m1}G_{m2}C_1/C_2)} \tag{16.90}$$

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Obviously for obtaining BE or AP, either some other circuit is to be used or the well-known techniques of summing two responses can be used.

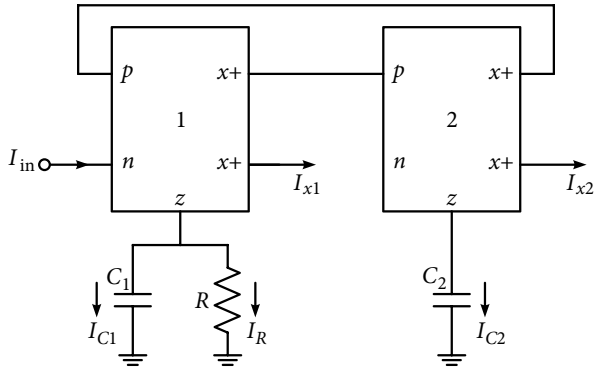

Figure 16.28 Realization of Tow–Thomas biquad using two CDTAs.

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Practice Problems

16-1 Using CCII, obtain (a) a current source of 10 μA at a frequency of 100 kHz from a voltage source of 1 volt and (b) convert it again into a voltage source of 1.5 volts.

16-2 Verify that the circuit shown in Figure 16.3(a) is a current amplifier. Test it for a current gain of 10, and also show that it is a non-inverting current amplifier.

16-3 Design and test the current summation circuit shown in Figure 16.3(c) with input currents of 2 mA, 3 mA and 4 mA with respective weightage of 0.2, 0.75 and 0.5.

16-4 What will be the magnitude of the output current if direction of the 3 mA current in Problem 16-3 is reversed? Verify the same.

16-5 Design and test VM and CM inverting integrators of Figure 16.4 using CCII with a dc gain of 12 dBs and their gain attenuates by 3 dBs at 100 kHz.

16-6 (a) Design and test a CM LP filter using the general structure shown in Figure16.5(a) with a dc gain of unity and a 3 dB frequency of 500 krad/s.

(b) Design and test a CM HP filter using the general structure shown in Figure16.5(a) with a high frequency gain of unity and a 3 dB frequency of 250 krad/s.

(c) Design and test a CM AP filter using the general structure shown in Figure16.5(a) having a phase shift of 90° at a frequency of 200 krad/s.

16-7 Repeat Problem 16-6(c) using the circuit shown in Figure16.5(b).

16-8 Design and test a notch filter using the circuit shown in Figure16.5(a) having a notch at 120 kHz. Find the attenuation at the notch.

16-9 Design and test a VM AP filter using the circuit shown in Figure P16.1(a) with its phase shift becoming –90° at 200 kHz.

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16-10 Repeat Problem 16-9 using the alternate circuit shown in Figure P16.1(b).

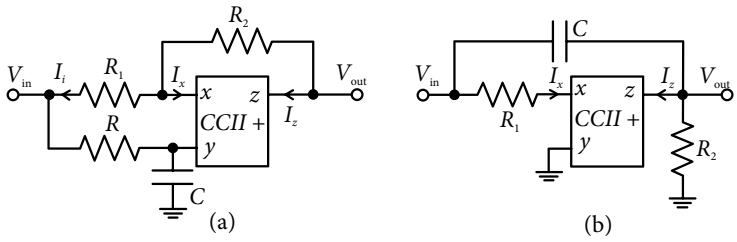

Figure P16.1

16-11 Using the passive structure of Figure 16.17(b), obtain a BP filter for center frequency of 50 kHz and Q = 5. Employ non-ideal inductor of Figure 16.20 (a).

Use the voltage following property in CCs for Problems 16-12 to 16-14.

16-12 Design and test the CC based second-order VM LP and a CM HP filter through conversion of an OA-RC single amplifier circuit, having cut-off frequency of 100 kHz and pole-Q = 2.5.

16-13 Convert a single amplifier circuit to a CC based second-order VM BP filter having center frequency of 100 krad/s and Q = 5. What kind of other CM response can also become available from the circuit? Verify the responses.

16-14 Repeat Problem 16-13 to realize a VM HP filter with a cut-off frequency of 150 krad/s and Q = 1.5.

16-15 Realize a BP filter using the multi-functional biquadratic circuit shown in Figure 16.14(a) for ω_0 = 500 krad/s and Q = 5. What is the peak gain and frequency at the peak for the corresponding LP response? Also realize AP and notch responses.

16-16 Modify the circuit in Problem 16-15 to get a notch when the lowest output voltage is not equal to the input voltage.

16-17 Design and test a maximally flat second-order HP filter section having 3 dB frequency of 50 kHz using the inductor circuit shown in Figure 16.18(b).

16-18 An LP filter has the following specifications:

ω_1 = 100 krps, ω_2 = 600 krps, $\mathcal{A}_{max}$ = 1 dB and $\mathcal{A}_{min}$ = 50 dB

Design and test a CC based filter to satisfy the specifications employing the inductor shown in Figure 16.17(a).

16-19 Use the general topology shown in Figure 16.12(a) and the feed-forward concept of Figure 16.12(b) to realize a BP and a LP response with Q = 2.5 and center frequency of 100 kHz. Find the mid-band gain realized for the BP and the peak frequency of the LP filter. Convert the structure to realize an asymmetrical notch and an AP filter; test the designed circuit.

16-20 Show that the circuit shown in Figure P16.2 works as a current -controlled current source.

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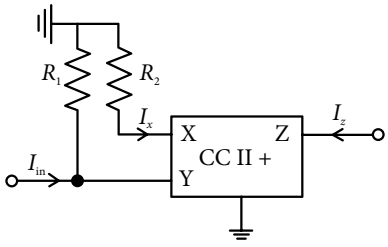

Figure P16.2

16-21 Utilize the circuit in Figure 16.18(b) to realize a second-order BR filter having notch frequency of 60 kHz.

16-22 Show that the circuit shown in Figure P16.3 works as a voltage-controlled current source.

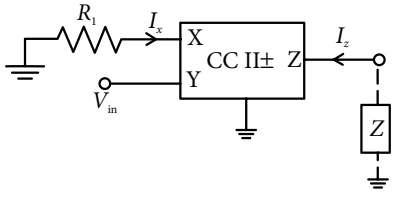

Figure P16.3

16-23 Using the passive structure shown in Figure 16.17(b), obtain a BP filter for center frequency of 60 kHz and $Q = 6$. Employ the non-ideal inductor shown in Figure 16.20(c).

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