8

Two-port networks

8.1 Introduction

Networks are frequently encountered in electronics, control and communication systems in which an input signal is impressed at one pair of terminals and an output signal is taken from another pair of terminals; such networks are called *two-terminal pair* networks or, more frequently *two-port* networks.

The resistance voltage divider, first introduced in section 2.2, is an example of an elementary two-port network, and many other examples have occurred in the intervening chapters. In particular, it was demonstrated in section 7.3.2 that a non-linear device such as the transistor could, for small-signal conditions, be modelled by linear, two-port network. The concepts relating to such networks are therefore of considerable generality, and in this chapter we examine the theory of two-ports in greater detail and introduce further applications.

The theory contained in this chapter is concerned with the functional relationships among the voltage and current variables at the two ports of the network as defined in fig. 8.1. If the variables are steady-state a.c. quantities, then these relationships are formulated in terms of impedances or admittances. These same relationships will, of course, apply if the variables are transformed variables; in this case impedances and admittances are generalized functions of complex frequency as defined in chapter 6. In the case of purely resistive networks the functional relationships among variables are identical in form for instantaneous and d.c. quantities as well as for a.c. quantities. It should also be noted that the same relationships apply for incremental (small-signal) a.c. quantities as defined in section 7.3.1.*

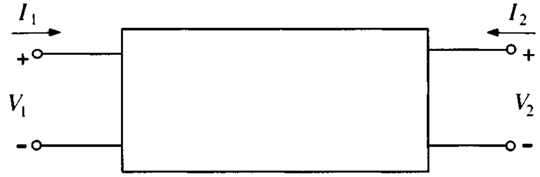
* In view of the variety of meanings that may be attached to the current and voltage variables and to impedance, the use of bold face type to indicate phasors and complex quantities is discontinued in this chapter.

A network having a single pair of terminals, a one-port network has associated with it a single current and a single voltage. The ratio of voltage to current, or current to voltage, is the impedance (admittance), which parameters completely characterize the circuit so far as any external network is concerned. For a two-port network there are four variables: an input voltage–current pair and an output voltage–current pair. The possible combinations of four variables taken two at a time is six; it is therefore possible to define six sets of parameters that characterize the two-port, one set for each pair of variables that are chosen to be independent. Which of the parameter sets chosen to characterize a given two-port depends on the application. In the following sections the parameter sets and their interrelationships are derived, and their areas of application are indicated.

Two-port networks are often categorized according to the degree of electrical symmetry which they possess. If a network is symmetrical about the axis XX' (fig. 8.2(*a*)) then it is said to be *balanced*; if it possesses symmetry about YY', then it is said to be *symmetrical*. Some typical network configurations with various types of symmetry are illustrated in figs. 8.2(*b*)–(*e*).

It will be noted that the networks shown in figs. 8.2(*b*) and (*d*) possess four distinct terminals while the networks shown in figs. 8.2(*c*) and (*e*) possess only three, terminals 1′ and 2′ being common to both input and output ports in both cases. However, in the theory which follows, no distinction is drawn between these two different configurations, the theory being concerned only with a description of a two-port with respect to the defined variables. So, although in the case of fig. 8.2(*b*), a potential difference may, in general, exist between terminals 1′ and 2′ while for fig. 8.2(*c*) terminals 1′ and 2′ must be at the same potential, as far as the theory here is concerned both networks possess identical characteristics. From a practical point of view this implies that connections between a two-port and its external circuits must be made in such a way as to prevent any external mesh current from flowing through any internal impedance other than the defined

Fig. 8.1. Voltage and current variables appertaining to the theory of two-port networks.



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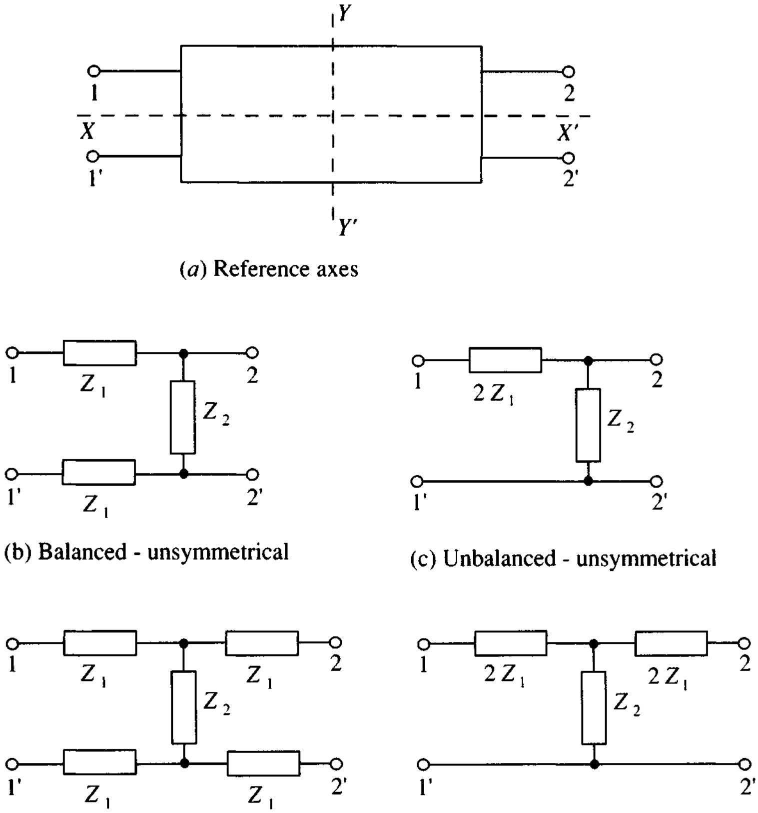
currents I_1 and I_2. If such currents flow through any of the impedances within the two-port, then the established relationships among the defined variables will no longer apply. In this respect the three-terminal networks of figs. 8.2(c) and (e) provide somewhat greater flexibility since external mesh currents can flow in the common connection without the predicted relationships among the defined variables being affected.

8.2 Admittance, impedance and hybrid parameters

8.2.1 Admittance parameters

The reference directions of currents and voltages at the two ports of the networks are indicated in fig. 8.1. Let us first consider the voltages as the excitations and the currents as the responses, then by linearity:

Fig. 8.2. Balance and symmetry in two-port networks.



(a) Reference axes

(b) Balanced - unsymmetrical

(c) Unbalanced - unsymmetrical

(d) Balanced - symmetrical

(e) Unbalanced - symmetrical

$$\left.\begin{aligned} I_1 &= y_{11}V_1 + y_{12}V_2 \\ I_2 &= y_{21}V_1 + y_{22}V_2 \end{aligned}\right\} \tag{8.1}$$

We may interpret the coefficients in (8.1), which have dimensions of admittance, in terms of measurements made at the terminals. For example, if the output terminals are short circuited, so that $V_2 = 0$, and if the responses I_1 and I_2 are measured when an excitation V_1 is applied, then

$$y_{11} = \left.\frac{I_1}{V_1}\right|_{V_2=0} \qquad y_{21} = \left.\frac{I_2}{V_1}\right|_{V_2=0} \tag{8.2}$$

y_{11} is clearly an *input admittance.* y_{21} represents the output current response to an input voltage: it is called the *forward transfer admittance.* If the input terminals are shorted so that $V_1 = 0$, and if the responses I_1 and I_2 are measured when an excitation V_2 is applied, then

$$y_{12} = \left.\frac{I_1}{V_2}\right|_{V_1=0} \qquad y_{22} = \left.\frac{I_2}{V_2}\right|_{V_1=0} \tag{8.3}$$

Now y_{22} is the *output admittance* and y_{12} is the *reverse transfer admittance.*

The four admittances completely characterize the two-port. They are commonly referred to as the short-circuit admittance parameters. The input admittance y_{11} and the output admittance y_{22} are frequently called *driving-point* admittances because each describes the response at a port when a driving function is applied. y_{12} and y_{21} are *transfer* admittances, describing the response at one port to excitation at the other.

As an example let us find the y-parameters for the π-network shown in fig. 8.3 in which the elements are specified in terms of their admittances. With $V_2 = 0$, the input admittance is simply the parallel combination of Y_1 and Y_3. Therefore,

$$y_{11} = Y_1 + Y_3$$

Also, with $V_2 = 0$, the current I_2 is the current in Y_3. Since with $V_2 = 0$ the voltage V_1 appears directly across Y_3 it follows that

$$y_{21} = -Y_3$$

The negative sign appears because with $V_2 = 0$ the current that results from V_1 is opposite in direction to the positive direction of I_2. Now we short circuit the input port making $V_1 = 0$. Then we find

$$y_{22} = Y_2 + Y_3 \qquad \text{and} \qquad y_{12} = -Y_3$$

where the negative sign indicates that when $V_1 = 0$, V_2 produces a short-circuit input current that is opposite in direction to the positive direction of I_1.

We see that for this example $y_{12}=y_{21}$ and we conclude that with equal voltage excitations the current responses will be equal. This is an example of *reciprocity*. As long as the circuit elements are linear and bilateral and the reciprocity principle applies then $y_{12}=y_{21}$ no matter how complicated the circuit that joins the two ports. Two-port networks of this type, which include all circuits containing only passive elements, are said to be *reciprocal*; those that have unequal transfer admittances, which include many types of active circuit, are said to be *non-reciprocal*.

8.2.2 Impedance parameters

If in the circuit of fig. 8.1 we assume the currents are the excitations, then the voltages are the responses and

$$\left.\begin{aligned} V_1 &= z_{11}I_1 + z_{12}I_2 \\ V_2 &= z_{21}I_1 + z_{22}I_2 \end{aligned}\right\} \tag{8.4}$$

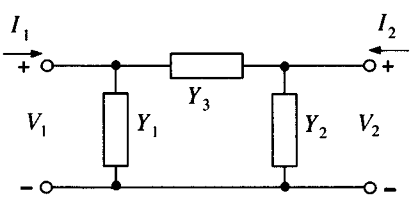
Now the parameters may be evaluated by making measurements of the three remaining variables when first I_1 and then I_2 is required to be zero. Then

$$\begin{aligned} z_{11} &= \left.\frac{V_1}{I_1}\right|_{I_2=0} \qquad & z_{21} &= \left.\frac{V_2}{I_1}\right|_{I_2=0} \\ z_{12} &= \left.\frac{V_1}{I_2}\right|_{I_1=0} \qquad & z_{22} &= \left.\frac{V_2}{I_2}\right|_{I_1=0} \end{aligned} \tag{8.5}$$

The zs all have dimensions of impedance. z_{11} and z_{22} are the *driving point impedances* with, respectively, the output and the input open circuited. z_{21} is the *forward transfer impedance* and z_{12} is the *reverse transfer impedance*. As is the case for the admittance parameters if the circuit elements are linear and bilateral, $z_{12}=z_{21}$.

It should be evident that there is no direct correspondence between the ys and the zs, that is, z_{11} is *not* the reciprocal of y_{11}. However, because they describe the same network there must be definite relationships between the

Fig. 8.3. π-network.



impedance parameters and the admittance parameters. We may find these interrelationships by solving (8.1) for V_1 and V_2 and then comparing the results with (8.4). We find:

$$z_{11}=\frac{y_{22}}{\Delta_y} \quad z_{12}=\frac{-y_{12}}{\Delta_y} \quad z_{21}=\frac{-y_{21}}{\Delta_y} \quad z_{22}=\frac{y_{11}}{\Delta_y} \tag{8.6}$$

where

$$\Delta_y=y_{11}y_{22}-y_{12}y_{21}$$

By solving (8.4) for I_1 and I_2 and comparing ith (8.2), we obtain

$$y_{11}=\frac{z_{22}}{\Delta_z} \quad y_{12}=\frac{-z_{12}}{\Delta_z} \quad y_{21}=\frac{-z_{21}}{\Delta_z} \quad y_{22}=\frac{z_{11}}{\Delta_z} \tag{8.7}$$

where

$$\Delta_z=z_{11}z_{22}-z_{12}z_{21}$$

Let us now find the z-parameters of the T-network of fig. 8.4. First apply a current source I_1 with the output port open so that $I_2=0$. The current flows through Z_1 and Z_3 in series, so

$$z_{11}=Z_1+Z_3 \qquad \text{and} \qquad z_{21}=Z_3$$

Next apply current source I_2 with $I_1=0$. Now the current flows through Z_2 and Z_3 in series, so

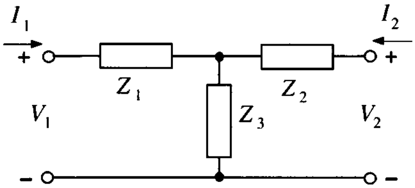
$$z_{12}=Z_3 \qquad \text{and} \qquad z_{22}=Z_2+Z_3$$

8.2.3 Hybrid and inverse hybrid parameters

These parameters derive their names from the fact that in neither set do all the parameters have the same dimensions. The *hybrid* parameters result when I_1 and V_2 are chosen as independent variables. Then

$$\left.\begin{aligned} V_1&=h_{11}I_1+h_{12}V_2 \\ I_2&=h_{21}I_1+h_{22}V_2 \end{aligned}\right\} \tag{8.8}$$

Fig. 8.4. T-network.



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Hybrid parameters are defined operationally in a manner similar to the admittance and impedance parameters:

$$h_{11}=\left.\frac{V_1}{I_1}\right|_{V_2=0} \qquad h_{21}=\left.\frac{I_2}{I_1}\right|_{V_2=0}$$
$$h_{12}=\left.\frac{V_1}{V_2}\right|_{I_1=0} \qquad h_{22}=\left.\frac{I_2}{V_2}\right|_{I_1=0} \tag{8.9}$$

It is apparent that h_{11} has dimensions of impedance, h_{22} has dimensions of admittance, and h_{12} and h_{21} are dimensionless.

When V_1 and I_2 are independent variables, I_1 and V_2 are written in terms of the *inverse hybrid* parameters:

$$\left.\begin{aligned} I_1 &= g_{11}V_1 + g_{12}I_2 \\ V_2 &= g_{21}V_1 + g_{22}I_2 \end{aligned}\right\} \tag{8.10}$$

These parameters may be found from appropriate open- and short-circuit measurements. g_{11} is an admittance, g_{22} is an impedance, and g_{12} and g_{21} are dimensionless.

8.3 Equivalent circuits and circuit models

For any one of the six possible sets of 2-port parameters, equivalent circuits may be derived which conform to the voltage–current relations expressed by those parameters. For example, the circuits shown in fig. 8.5 are two possible configurations conforming to the relations (8.1) in which the coefficients are the admittance parameters. In the case of fig. 8.5(*a*) we see that the first expression in (8.1) is simply the nodal equation for the left-hand half of the circuit, while the second expression represents the nodal equation for the right-hand half. (It is left as an exercise for the reader to show that the circuit of fig. 8.5(*b*) also conforms to the relations (8.1).)

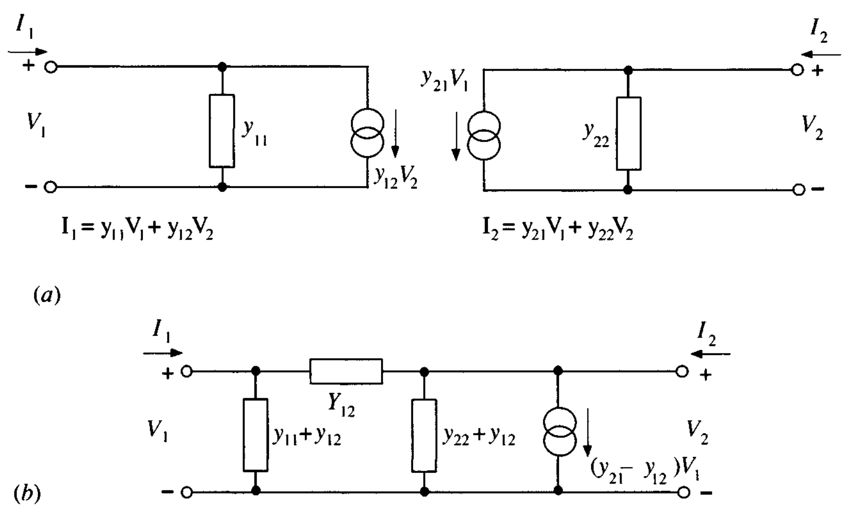
The circuits shown in fig. 8.5 are not unique in expressing the relations (8.1), but they are two of the simplest and are generally the most convenient to use for the purposes of practical circuit analysis. It should be observed that the sources in these equivalent circuits are of the *controlled* or *dependent* type; the methods of analysis of circuits containing such sources have been treated in section 2.13. It is also worthy of note that the single dependent current source in the circuit of fig. 8.5(*b*) becomes zero (an open circuit) if $y_{12}=y_{21}$, that is, if the circuit is reciprocal. From this we may infer that a passive 2-port network, which must be reciprocal, may be represented by three immittances connected in a π-configuration.

Equivalent circuits derived from the admittance, impedance or hybrid parameter sets are commonly used as a basis for the modelling of non-linear devices such as the transistor. In section 7.3.2 we saw how an h-parameter model for the transistor, operating under small-signal conditions, could be derived by considering its input and output characteristics. This model (shown in fig. 7.13) is repeated in fig. 8.6 together with an equivalent circuit conforming to the relations (8.8). The first expression in (8.8) derives from the mesh equation for the left-hand half of the equivalent circuit; the second expression from the nodal equation for the right-hand half. The h-parameter subscripts differ in the two circuits of fig. 8.6, but the correspondence, element for element, will be obvious.*

The behaviour of a transistor operating at low or medium frequencies may be adequately represented by a linear model containing only resistive elements; consequently, in fig. 8.6, the impedance h_{11} corresponds to resistance h_{ie} and the admittance h_{22} corresponds to conductance h_{oe}. The parameters h_{re} and h_{fe} are, of course, dimensionless.

Although the h-parameter equivalent circuit shown in fig. 8.6 is the one commonly used for modelling the transistor, other models may for particular applications be more convenient or appropriate. For example, the model shown in fig. 8.7 is of interest because each of the elements relates directly to some part of the two-junction physical model for the transistor

Fig. 8.5. Admittance parameter equivalent circuits.

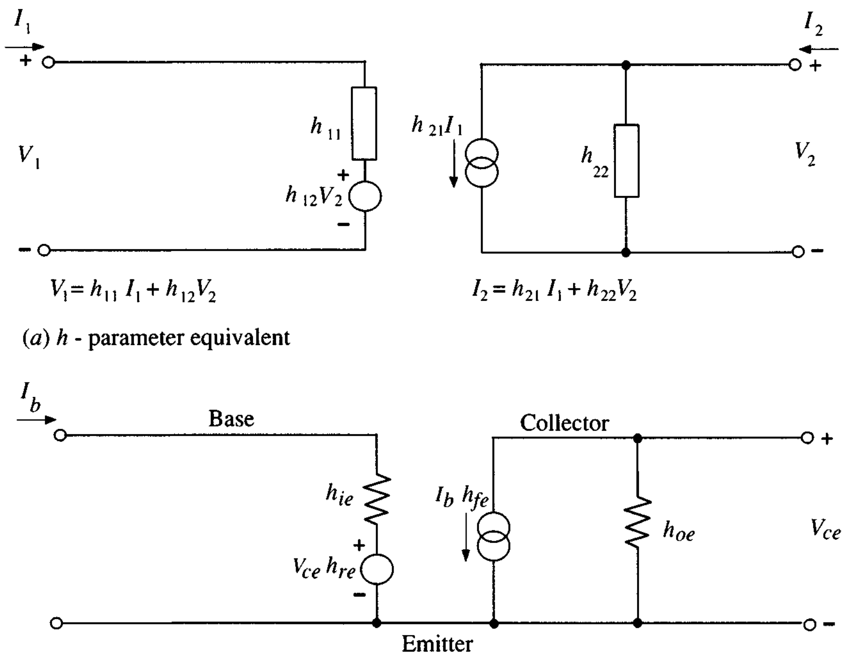


* In the context of transistor circuits the h-parameters are designated by the letters i, o, r and f; standing for, respectively, input, output, reverse and forward. The second letter indicates which of the three terminals of the transistor (emitter, base, collector) is common to the input and output ports.

(see reference 5). It is possible to show that this model is related to an equivalent circuit defined in terms of the z-parameters (see problem 8.3).

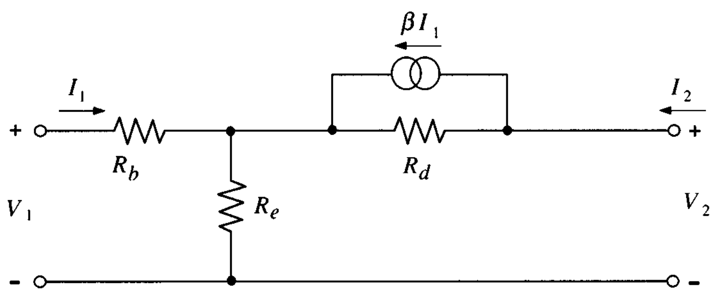
The 2-port parameters chosen to model a device such as a transistor are determined in practice by making direct, physical measurements at its terminals. At low or medium frequencies such measurements present no special difficulty and the hybrid parameters, or indeed any of the 2-port parameters sets, may be readily determined. At high or very high

Fig. 8.6. Hybrid parameter circuits.



(*b*) Transistor model

Fig. 8.7. T-equivalent network for the bipolar transistor.



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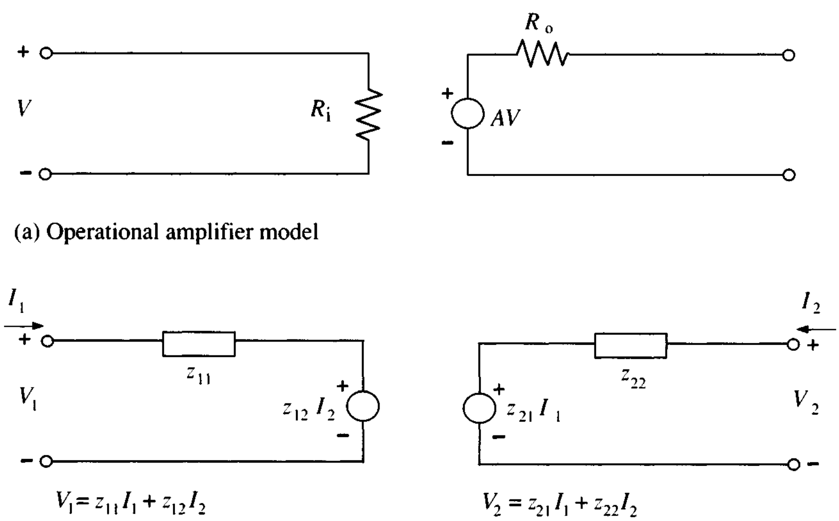
frequencies, however, sophisticated measurement techniques become necessary and in this respect a model based on the admittance parameters is advantageous. The reason for this will become apparent if we compare the definitions of the h- and y-parameter sets. From (8.9) it is seen that determination of h_{21} and h_{22} necessitates making measurements with terminals open circuit, but the creation of a valid open circuit at high frequencies is complicated by the presence of stray capacitance. The y-parameters, on the other hand, can all be determined by making admittance measurements with terminals short circuit (see definitions (8.2) and (8.3)), and it is easier to produce a valid short circuit in the presence of stray capacitance than it is an open circuit. Thus the admittance parameters may be related directly to the most appropriate set of physical measurements and for this reason are preferred as a basis for modelling transistors intended for high-frequency operation.

As a final example of device modelling by means of the two-port parameters we consider the circuit of fig. 8.8(a), which is commonly used to model an operational amplifier at low or medium frequencies. (The use of this model was illustrated in section 2.14.) The model is based on the z-parameter equivalent circuit shown in fig. 8.8(b). The mesh equations for the left- and right-hand halves of this circuit conform to (8.4). At low or medium frequencies, only the resistive components of the impedances

Fig. 8.8. Circuit model for an operational amplifier based on an impedance-parameter equivalent circuit.



(b) z-parameter equivalent circuit

associated with the amplifier need be considered, hence the impedances z_{11} and z_{22} are identified respectively with the input resistance R_i and output resistance R_o of the amplifier.

For a practical operational amplifier the voltage and current conditions at its output have an insignificant effect on conditions at its input, in other words, the transfer impedance z_{12} is negligibly small, consequently a voltage source corresponding to $(z_{12}I_2)$ is absent from the model. If z_{12} is negligible, then for fig. 8.8(*b*) the input current is $I_1 = V_1/z_{11}$ and the magnitude of the voltage source in the output circuit is $z_{21}I_1 = (z_{21}/z_{11})V_1$. The ratio (z_{21}/z_{11}) is a dimensionless quantity called the *forward voltage transfer coefficient*; it may be identified with A, the gain of the amplifier.

8.4 Transmission, inverse transmission and *ABCD* parameters

When a 2-port is used to transfer a signal from one port to another, it is appropriate to express the voltage and current at one port in terms of the voltage and current at the other. If V_2 and I_2 are the independent variables,

$$\left.\begin{aligned} V_1 &= a_{11}V_2 + a_{12}I_2 \\ I_1 &= a_{21}V_2 + a_{22}I_2 \end{aligned}\right\} \tag{8.11}$$

where the *a*s are the *transmission* parameters. When V_1 and I_1 are the independent variables,

$$\left.\begin{aligned} V_2 &= b_{11}V_1 + b_{12}I_1 \\ I_2 &= b_{21}V_1 + b_{22}I_1 \end{aligned}\right\} \tag{8.12}$$

where the *b*s are the *inverse transmission* parameters.* Here again the parameters do not all have the same dimensions. a_{12} and b_{12} are impedances, a_{21} and b_{21} are admittances and the other four parameters are dimensionless.

At this point we encounter a problem in terminology. Although the definition of the *a* and *b* parameters in (8.11) and (8.12) follow directly from what has gone before, these are not the parameters commonly used in circuit analysis. Transmission parameters were defined originally for power system calculations, and the positive direction of the current at port number 2 was taken to be *out* of the positive end of that port. The parameters A, B, C and D are then defined by

* The terminology here is not altogether logical. The *transmission* parameters express *input* in terms of *output*, while the *inverse* parameters express *output* in terms of *input*.

$$\left.\begin{aligned} V_s &= AV_r + BI_r \\ I_s &= CV_r + DI_r \end{aligned}\right\} \tag{8.13}$$

where the currents and voltages are as shown in fig. 8.9. The subscripts r and s may be taken to stand, respectively, for receiving and sending. In order to avoid confusion with the transmission parameters defined by (8.11) we shall, in all that follows, refer to the parameters defined by (8.13) as the *ABCD* parameters.

In terms of short-circuit and open-circuit measurements:

$$\begin{aligned} A &= \left.\frac{V_s}{V_r}\right|_{I_r=0} \qquad & B &= \left.\frac{V_s}{I_r}\right|_{V_r=0} \\ C &= \left.\frac{I_s}{V_r}\right|_{I_r=0} \qquad & D &= \left.\frac{I_s}{I_r}\right|_{V_r=0} \end{aligned} \tag{8.14}$$

The *inverse ABCD parameters* are defined by the following relations:

$$\left.\begin{aligned} V_r &= A'V_s + B'I_s \\ I_r &= C'V_s + D'I_s \end{aligned}\right\} \tag{8.15}$$

In the analysis of two-port networks it is frequently useful to be able to convert from one set of parameters to another set. The relationships between the *ABCD* parameters and the admittance and impedance parameters already defined are readily determined.

Using (8.1) but with the currents and voltages as defined in fig. 8.9 we obtain:

$$\begin{aligned} I_s &= y_{11}V_s + y_{12}V_r \\ -I_r &= y_{21}V_s + y_{22}V_r \end{aligned}$$

Solving these equations for V_s and I_s and comparing the results with (8.13) we find:

$$\begin{aligned} A &= -\frac{y_{22}}{y_{21}} \qquad & B &= -\frac{1}{y_{21}} \\ C &= y_{12} - \frac{y_{11}y_{22}}{y_{21}} \qquad & D &= -\frac{y_{11}}{y_{12}} \end{aligned} \tag{8.16}$$

By using (8.4) with currents and voltages as defined in fig. 8.9, we obtain:

$$\begin{aligned} A &= \frac{z_{11}}{z_{21}} \qquad & B &= \frac{z_{11}z_{22}}{z_{21}} - z_{12} \\ C &= \frac{1}{z_{21}} \qquad & D &= \frac{z_{22}}{z_{21}} \end{aligned} \tag{8.17}$$

We have already shown that for passive, linear circuit elements $y_{12} = y_{21}$ and $z_{12} = z_{21}$. It follows then from either (8.16) or (8.17) that

$$AD - BC = 1 \qquad \text{or} \qquad \begin{vmatrix} A & B \\ C & D \end{vmatrix} = 1 \tag{8.18}$$

If the network is symmetrical, then $z_{11} = z_{22}$ and $y_{11} = y_{22}$ and therefore $A = D$. It follows then that *for a symmetrical 2-port*

$$\begin{vmatrix} A & B \\ C & A \end{vmatrix} = 1 \tag{8.19}$$

8.5 Matrix notation

It is often convenient to write the various sets of parameters for the two-port in matrix form. Thus, the relations (8.1) for the admittance parameter may be written:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{8.20}$$

or

$$[I] = [Y)][V]$$

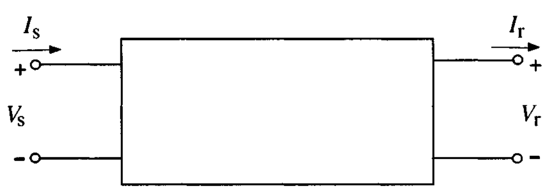
The matrix

$$[Y] = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix}$$

is often referred to as the *short-circuit admittance matrix.* The term 'short circuit' refers to the fact that we may determine numerical values of the matrix elements by making short-circuit measurements on the two-port. (Or by making short-circuit calculations if the details of the two-port are known.)

In similar fashion one may, from (8.4), write the *open-circuit impedance matrix*:

Fig. 8.9. Reference directions for current and voltage variables for *ABCD* parameters.



$$\begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix}$$

where 'open circuit' refers to the conditions under which measurements (or calculations) are made on the two-port to determine the matrix elements.

It is apparent that for each of the six possible sets of equations that may be used to characterize the two-port we may write an appropriate matrix and express the behaviour of the two-port by means of matrix equations.

8.6 Worked example

For the simple unsymmetrical two-port shown in fig. 8.10, calculate the impedance, admittance and *ABCD* parameters and express the appropriate equations in matrix form.

Solution. From (8.4) and (8.5), it follows that the impedance parameters are

$$z_{11}=2+4=6\,\Omega \qquad z_{22}=8+4=12\,\Omega$$
$$z_{12}=4\,\Omega \qquad z_{21}=4\,\Omega$$

Then

$$\Delta_z=z_{11}z_{22}-z_{21}z_{12}=6\times 12-4\times 4=56$$

Now we use (8.7) to calculate the y-parameters

$$y_{11}=\frac{z_{22}}{\Delta_2}=\frac{3}{14} \qquad y_{22}=\frac{z_{11}}{\Delta_2}=\frac{3}{28}$$

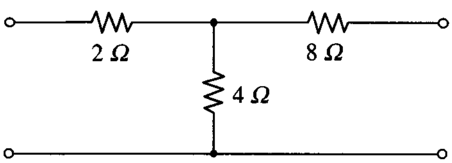
$$y_{12}=-\frac{z_{12}}{\Delta_2}=-\frac{1}{14} \qquad y_{21}=-\frac{z_{21}}{\Delta_2}=-\frac{1}{14}$$

To find the transmission parameters we use (8.17)

$$A=\frac{z_{11}}{z_{21}}=\frac{3}{2} \qquad B=\frac{z_{11}z_{22}}{z_{21}}-z_{12}=18-4=14$$

$$C=\frac{1}{z_{21}}=\frac{1}{4} \qquad D=\frac{z_{22}}{z_{21}}=3$$

Fig. 8.10. Circuit for worked example (section 8.6).



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We may use the relation (8.18) to check our results.

$$(AD-BC)=(3/2)\cdot 3-14\cdot(1/4)=(9/2)-(7/2)=1$$

Now in matrix form the equations for the two-port of fig. 8.10 are

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix}=\begin{bmatrix} 3/14 & -1/14 \\ -1/14 & 3/28 \end{bmatrix}\begin{bmatrix} V_1 \\ V_2 \end{bmatrix}$$

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix}=\begin{bmatrix} 6 & 4 \\ 4 & 12 \end{bmatrix}\begin{bmatrix} I_1 \\ I_2 \end{bmatrix}$$

$$\begin{bmatrix} V_s \\ I_s \end{bmatrix}=\begin{bmatrix} 3/2 & 14 \\ 1/4 & 3 \end{bmatrix}\begin{bmatrix} V_r \\ I_r \end{bmatrix}$$

8.7 Relationships between direct and inverse *ABCD* parameters

In matrix form the relations (8.15) for the inverse *ABCD* parameters are

$$\begin{bmatrix} V_r \\ I_r \end{bmatrix}=\begin{bmatrix} A' & B' \\ C' & D' \end{bmatrix}\begin{bmatrix} V_s \\ I_s \end{bmatrix} \tag{8.21}$$

We now employ matrix algebra to find the relations among the parameters A, B, C, D and the parameters A', B', C', D'. From (8.13) we have

$$\begin{bmatrix} V_s \\ I_s \end{bmatrix}=\begin{bmatrix} A & B \\ C & D \end{bmatrix}\begin{bmatrix} V_r \\ I_r \end{bmatrix} \tag{8.22}$$

or

$$[S]=[M][R] \tag{8.23}$$

Now we multiply (8.23) by $[M]^{-1}$. Then, since $[M][M]^{-1}$ is the unit matrix, we have

$$[R]=[M]^{-1}[S] \tag{8.24}$$

Now, from the theory of matrix algebra, a matrix defined by

$$[L]=\begin{bmatrix} L_{11} & L_{12} \\ L_{21} & L_{22} \end{bmatrix}$$

has an inverse

$$[L]^{-1}=\frac{1}{\Delta}\begin{bmatrix} L_{22} & L_{12} \\ -L_{21} & L_{11} \end{bmatrix}$$

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where

$$\Delta=(L_{11}L_{22}-L_{12}L_{21})$$

Applying this result in (8.24) gives

$$[R]=\frac{1}{(AD-BC)}\begin{bmatrix} D & -B \\ -C & A \end{bmatrix}[S]$$

But $(AD-BC)=1$. Hence

$$\begin{bmatrix} V_r \\ I_r \end{bmatrix}=\begin{bmatrix} D & -B \\ -C & A \end{bmatrix}\begin{bmatrix} V_s \\ I_s \end{bmatrix} \tag{8.25}$$

Comparing the matrices (8.21) and (8.25) we find:

$$A'=D, \quad B'=-B, \quad C'=-C, \quad \text{and } D'=A$$

Then in terms of the direct $ABCD$ parameters, V_r and I_r are given by

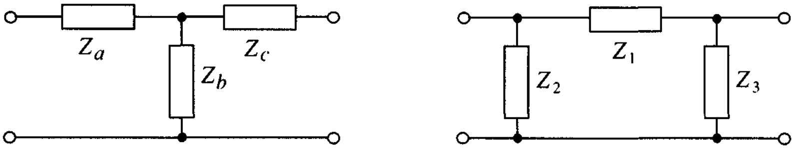
$$V_r=DV_s-BI_s$$
$$I_r=-CV_s+AI_s$$

8.8 Parameter relationships for π- and T-networks

The networks shown in fig. 8.11 are commonly employed in both power and communications branches of electrical engineering, and reference has already been made to them in sections 2.9.2 and 5.3.6 where they were referred to as star–delta or wye–delta networks. As we have already observed in connection with power systems, the analysis of circuits containing such configurations is sometimes considerably facilitated by the transformation of one configuration into the other. One technique for effecting this transformation has been given in section 2.9.2 and the sets of transformation relations are expressed in (2.23) for the case of a purely resistive network.

An alternative method for deriving the relations that must hold at the two ports of the T- and π-networks if they are to be equivalent is to

Fig. 8.11. T–π transformation.



(*a*) (*b*)

determine, say, the transmission parameters for the two networks and then set corresponding parameters equal. It is left as an exercise for the reader to prove in this way the following relations, which are similar in form to those in (2.23):

$$\begin{aligned} Z_1 &= Z_a + Z_c + \frac{Z_a Z_c}{Z_b}; \qquad & Z_a &= \frac{Z_1 Z_2}{Z_1 + Z_2 + Z_3} \\ Z_2 &= Z_b + Z_a + \frac{Z_b Z_a}{Z_c}; \qquad & Z_b &= \frac{Z_2 Z_3}{Z_1 + Z_2 + Z_3} \\ Z_3 &= Z_c + Z_b + \frac{Z_c Z_b}{Z_a}; \qquad & Z_c &= \frac{Z_3 Z_1}{Z_1 + Z_2 + Z_3} \end{aligned} \tag{8.25}$$

8.9 Worked example

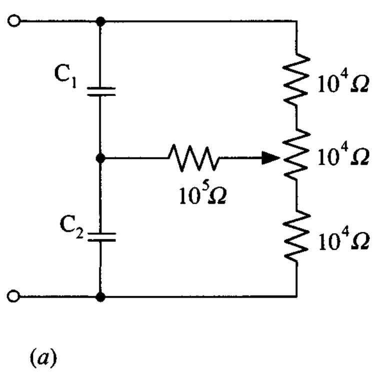
The resistors in the circuit of fig. 8.12(*a*) are used as part of a bridge circuit in which the effective resistances in parallel with C_1, C_2 can be varied. Calculate the maximum and minimum value of the resistances appearing in parallel with C_1, C_2.

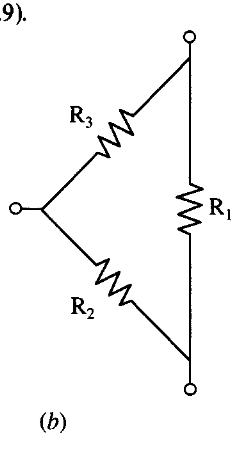
Solution

The resistive T-network in fig. 8.12(*a*) can be replaced exactly by the π-network of fig. 8.12(*b*). The resistors of interest are R_2, R_3. Using the notation of fig. 8.11 we have

$$Z_a = [(1-\alpha)+1] \times 10^4\,\Omega = (2-\alpha) \times 10^4\,\Omega$$
$$Z_c = (1+\alpha) \times 10^4\,\Omega$$
$$Z_b = 10^5\,\Omega$$

Fig. 8.12. Circuit for worked example (section 8.9).





in which α represents the fractional position of the slider on the potentiometer. Equations (8.25) can then be applied to give

$$R_1 = 3 \times 10^4 + (2-\alpha)(1+\alpha) \times 10^3$$

$$R_2 = 10^5 + (2-\alpha) \times 10^4 + \frac{2-\alpha}{1+\alpha} \times 10^5$$

$$R_3 = 10^5 + (1+\alpha) \times 10^4 + \frac{1+\alpha}{2-\alpha} \times 10^5$$

From the nature of the circuit it is clear that the extremes of R_2, R_3 will occur for the slider at an end of the potentiometer, i.e. $\alpha = 0$ or 1.

Putting $\alpha = 0$ we find

$$R_2 = 3.2 \times 10^5\,\Omega$$
$$R_3 = 1.6 \times 10^5\,\Omega$$

In the middle for $\alpha = 0.5$

$$R_2 = R_3 = 2.15 \times 10^5\,\Omega$$

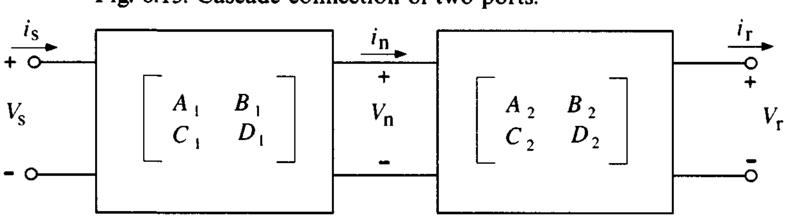
8.10 Cascaded two-ports and chain matrices

Of special interest is the situation where two or more two-ports are connected in *cascade* with the output of the first providing the input to the second and so on. We are interested then in calculating the output of the final two-port in terms of the input to the first two-port. For such calculations the *ABCD* parameters are appropriate. The matrix that represents the *ABCD* parameters is frequently referred to as the *chain matrix*.

Consider the cascade connection shown in fig. 8.13, where the parameters of the two circuits are identified by the subscripts '1' and '2'. The subscript 's' identifies the input to the first two-port and the subscript 'r' identifies the output of the second two-port. Then in fig. 8.13

$$\begin{bmatrix} V_n \\ I_n \end{bmatrix} = \begin{bmatrix} A_2 & B_2 \\ C_2 & D_2 \end{bmatrix} \begin{bmatrix} V_r \\ I_r \end{bmatrix}$$

Fig. 8.13. Cascade connection of two-ports.



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and

$$\begin{bmatrix} V_s \\ I_s \end{bmatrix} = \begin{bmatrix} A_1 & B_1 \\ C_1 & D_1 \end{bmatrix} \begin{bmatrix} V_n \\ I_n \end{bmatrix}$$

Then

$$\begin{bmatrix} V_s \\ I_s \end{bmatrix} = \begin{bmatrix} A_1 & B_1 \\ C_1 & D_1 \end{bmatrix} \begin{bmatrix} A_2 & B_2 \\ C_2 & D_2 \end{bmatrix} \begin{bmatrix} V_r \\ I_r \end{bmatrix} \tag{8.26}$$

We now show how the $ABCD$ parameters of a two-port network may be derived by combining the chain matrices for the individual elements or sections of which the two-port is comprised. Consider first the two simple two-port networks of fig. 8.14.

Clearly in fig. 8.14(a)

$$V_s = V_r + ZI_r$$
$$I_s = I_r$$

Thus the $ABCD$ matrix for this network is

$$\begin{bmatrix} 1 & Z \\ 0 & 1 \end{bmatrix} \tag{8.27}$$

For the circuit of fig. 8.14(b) (in which Y represents the shunt admittance)

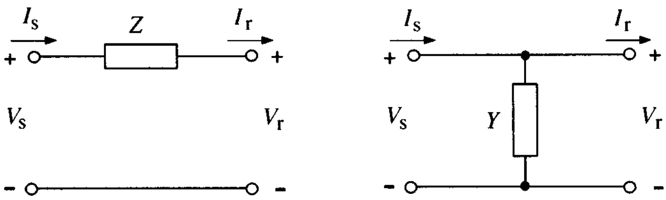
$$V_s = V_r$$
$$I_s = YV_r + I_r$$

Thus the $ABCD$ matrix is

$$\begin{bmatrix} 1 & 0 \\ Y & 1 \end{bmatrix} \tag{8.28}$$

For both of these we may check the validity of $AD - BC = 1$. Applying (8.26) the $ABCD$ matrix for the circuit of fig. 8.15(a) is found as

Fig. 8.14. Single element two-ports.



(a) Series element (b) Parallel element

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$$\begin{bmatrix} 1 & Z_1 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ 1/Z_2 & 1 \end{bmatrix} = \begin{bmatrix} 1+Z_1/Z_2 & Z_1 \\ 1/Z_2 & 1 \end{bmatrix} \tag{8.29}$$

For the circuit of fig. 8.15(*b*)

$$\begin{bmatrix} 1 & 0 \\ 1/Z_2 & 1 \end{bmatrix} \begin{bmatrix} 1 & Z_1 \\ 0 & 1 \end{bmatrix} = \begin{bmatrix} 1 & Z_1 \\ 1/Z_2 & 1+Z_1/Z_2 \end{bmatrix} \tag{8.30}$$

By combining these results with (8.27, 8.28) we may then find the *ABCD* matrices for the T- and π-sections of fig. 8.11. For the T-section of fig. 8.11(*a*) we have, using (8.27, 8.29),

$$\begin{bmatrix} 1+Z_a/Z_b & Z_a \\ 1/Z_b & 1 \end{bmatrix} \begin{bmatrix} 1 & Z_c \\ 0 & 1 \end{bmatrix} = \begin{bmatrix} 1+Z_a/Z_b & (Z_aZ_b+Z_bZ_c+Z_cZ_a)/Z_b \\ 1/Z_b & 1+Z_c/Z_b \end{bmatrix} \tag{8.31}$$

The same result can be obtained by pre-multiplication of equation (8.30) by (8.27).

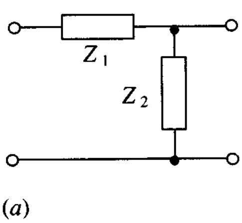
For the π-section of fig. 8.11(*b*) we similarly find for the *ABCD* matrix

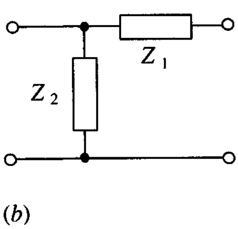
$$\begin{aligned} &\begin{bmatrix} 1 & Z_1 \\ 1/Z_2 & 1+Z_1/Z_2 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ 1/Z_3 & 1 \end{bmatrix} \\ &= \begin{bmatrix} 1+Z_1/Z_3 & Z_1 \\ (Z_1+Z_2+Z_3)/Z_2Z_3 & 1+Z_1/Z_2 \end{bmatrix} \end{aligned} \tag{8.32}$$

These results illustrate the formal procedure for evaluating the *ABCD* matrix of any ladder network (consisting solely of series or shunt elements).

For other circuits, equations similar to those by which (8.27) and (8.28) were derived may be set, or the formal expression of equations (8.14) may be used. This latter process will be illustrated for the balanced lattice of fig. 8.16(*a*). To apply equations (8.14) we need to analyse the circuit for the two cases $I_r=0$ and $V_r=0$. When $I_r=0$ the relevant variables are shown in fig. 8.16(*b*) whence

Fig. 8.15. Cascade connections of the two-ports of fig. 8.14.





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$$V_r = \left(\frac{Z_2}{Z_1+Z_2} - \frac{Z_1}{Z_1+Z_2}\right)V_s = \left(\frac{Z_2-Z_1}{Z_2+Z_1}\right)V_s$$

and

$$I_s = 2V_s/(Z_1+Z_2)$$

These two results used in equations (8.14) give

$$A = \frac{Z_2+Z_1}{Z_2-Z_1}$$

$$C = \frac{2}{Z_2-Z_1}$$

The case $V_r = 0$ is shown in fig. 8.16(*c*), whence

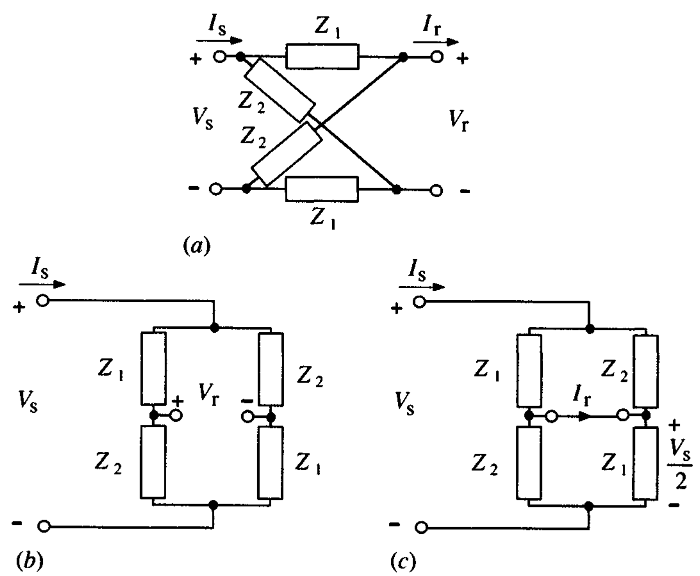
$$B = \frac{2Z_1Z_2}{Z_2-Z_1}$$

$$D = \frac{Z_2+Z_1}{Z_2-Z_1}$$

Thus the *ABCD* matrix for the balanced lattice is given by

$$\frac{1}{Z_2-Z_1}\begin{bmatrix} Z_2+Z_1 & 2Z_1Z_2 \\ 2 & Z_2+Z_1 \end{bmatrix} \tag{8.33}$$

Fig. 8.16. Balanced lattice network.



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As a check the symmetry is observed and the relation $AD - BC = 1$ may be verified.

Another common component is the ideal transformer, shown in fig. 8.17. The action of this ideal component is defined by the relations

$$V_r = \frac{1}{n} V_s$$

$$I_r = nI_s$$

whence the *ABCD* matrix is given by

$$\begin{bmatrix} n & 0 \\ 0 & 1/n \end{bmatrix} \tag{8.34}$$

The simplest equivalent circuit for a real transformer takes the form shown in fig. 8.18, in which Z_1, Z_2 will be inductances. Following previous examples the overall matrix may be calculated as

$$\begin{bmatrix} 1 & 0 \\ 1/Z_1 & 1 \end{bmatrix} \begin{bmatrix} n & 0 \\ 0 & 1/n \end{bmatrix} \begin{bmatrix} 1 & Z_2 \\ 0 & 1 \end{bmatrix}$$

$$= \begin{bmatrix} n & nZ_2 \\ n/Z_1 & \dfrac{1}{n} + \dfrac{nZ_2}{Z_1} \end{bmatrix} \tag{8.35}$$

The above results are summarized in table 8.1. Two other two-ports are also listed which cannot be constructed from bilateral components since

Fig. 8.17. Ideal transformer.

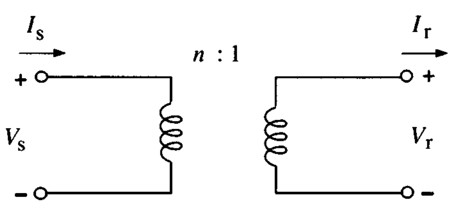

Fig. 8.18. Non-ideal transformer.

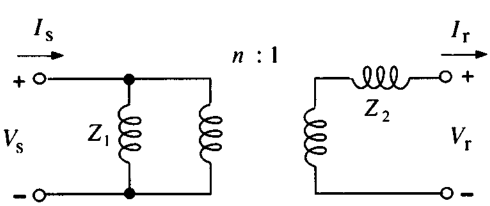

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Table 8.1

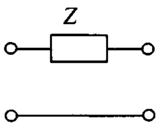
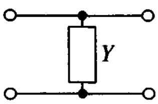
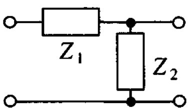
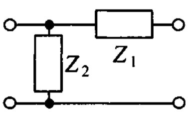
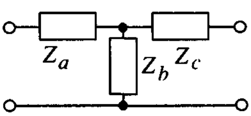
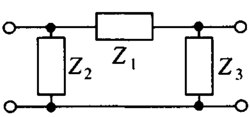
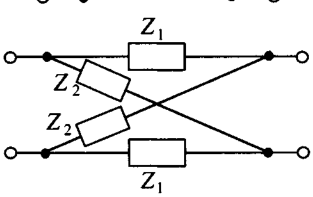
Circuit	Chain matrix
	$\begin{bmatrix} A & B \\ C & D \end{bmatrix}$
	$\begin{bmatrix} 1 & Z \\ 0 & 1 \end{bmatrix}$
	$\begin{bmatrix} 1 & 0 \\ Y & 1 \end{bmatrix}$
	$\begin{bmatrix} 1 + Z_1/Z_2 & Z_1 \\ 1/Z_2 & 1 \end{bmatrix}$
	$\begin{bmatrix} 1 & Z_1 \\ 1/Z_2 & 1 + Z_1/Z_2 \end{bmatrix}$
	$\begin{bmatrix} 1 + Z_a/Z_b & (Z_aZ_b + Z_bZ_c + Z_cZ_a)/Z_b \\ 1/Z_b & 1 + Z_c/Z_b \end{bmatrix}$
	$\begin{bmatrix} 1 + Z_1/Z_3 & Z_1 \\ (Z_1 + Z_2 + Z_3)/Z_2Z_3 & 1 + Z_1/Z_2 \end{bmatrix}$
	$\frac{1}{Z_2 - Z_1} \begin{bmatrix} Z_2 + Z_1 & 2Z_1Z_2 \\ 2 & Z_2 + Z_1 \end{bmatrix}$

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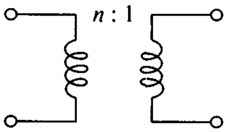
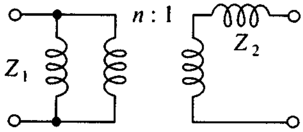
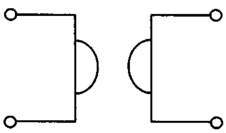
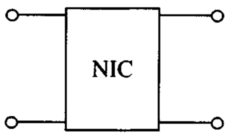
Table 8.1 (*cont.*)

Circuit	Chain matrix
	$\begin{bmatrix} n & 0 \\ 0 & 1/n \end{bmatrix}$
	$\begin{bmatrix} n & nZ_2 \\ n/Z_1 & 1/n + nZ_2/Z_1 \end{bmatrix}$
	$\begin{bmatrix} 0 & a \\ 1/a & 0 \end{bmatrix}$
	$\begin{bmatrix} a & 0 \\ 0 & -a \end{bmatrix}$

both are non-reciprocal. These are the *gyrator* and the *negative-impedance-converter*. Using the standard conventions for V_s, I_s, V_r and I_r the power dissipated in the two-ports is $V_sI_s - V_rI_r$. For a passive lossless component therefore

$$V_sI_s = V_rI_r$$

Two simple sets of relations satisfy this equation:

either:

$$\frac{V_s}{V_r} = \frac{I_r}{I_s} = n$$

or

$$\frac{V_s}{I_r} = \frac{V_r}{I_s} = a$$

The first of these is applied to the ideal transformer, which was considered above, the second defines the gyrator. Hence the *ABCD* matrix for the gyrator is

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$$\begin{bmatrix} 0 & a \\ 1/a & 0 \end{bmatrix} \tag{8.36}$$

for which $AD-BC=-1$ and so is non-reciprocal. The conventional symbol is shown in fig. 8.19(a). The input impedance resulting from a termination in impedance Z, fig. 8.19(b), will be seen to be

$$a^2/Z$$

The negative-impedance-converter (NIC) is defined by the relations

$$V_s = aV_s$$
$$I_s = -aI_r$$

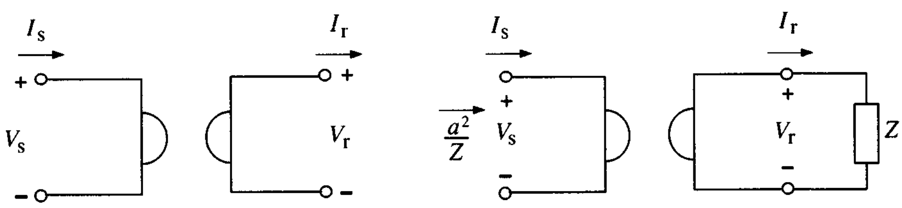
corresponding to the $ABCD$ matrix

$$\begin{bmatrix} a & 0 \\ 0 & -a \end{bmatrix} \tag{8.37}$$

Such a two-port takes its name because the input impedance is the negative of the terminating impedance, as indicated in fig. 8.20. As might be expected by considering a resistive termination this two-port is active as well as non-reciprocal.

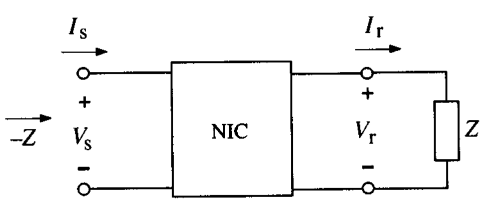
Both these two-ports can be realized approximately at low frequencies by use of operational amplifiers.

Fig. 8.19. Gyrator.



(a) (b)

Fig. 8.20. Negative-impedance-converter.



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8.11 Worked example

A two-wire high voltage, 50 Hz, transmission line has the following parameters:

Series inductance	2.2 mH/km
Series resistance	0.2 Ω/km
Shunt capacity	15 nF/km

Suggest a T-network which will represent a 50 km length of such a line, and calculate the chain matrix at 50 Hz.

Solution

Total series elements are 10 Ω in series with 110 mH; shunt capacitance is 0.75 μF. The T-network which suggests itself is shown in fig. 8.21(*a*); it is not quite accurate since it neglects the fact that the components are distributed along the length of the wire. However for this length at 50 Hz the error is not significant.

The value for the chain-matrix can be obtained by use of table 8.1. We find

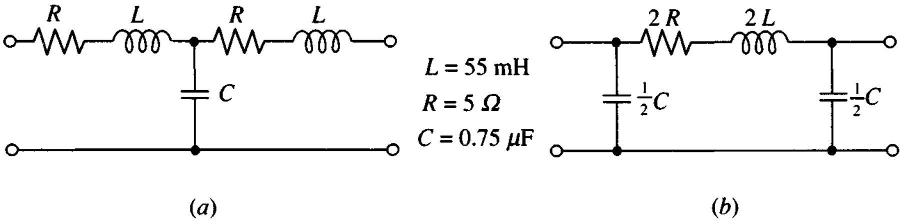
$$A = D = 1 + (R + j\omega L)j\omega C$$
$$C = j\omega C$$
$$B = 2(R + j\omega L) + j\omega C(R + j\omega L)^2$$

Using the values in the circuit, we find for 50 Hz

$$A = D = 0.996 + j10^{-3}$$
$$C = j2.4\ 10^{-4}$$
$$B = 10 + j34.6$$

In this case the shunt impedance is very high compared with the series impedance (by some 4000 ×); this also implies that the π-network of fig. 8.21(*b*) is an acceptable equivalent.

Fig. 8.21. Circuit for worked example (section 8.11).



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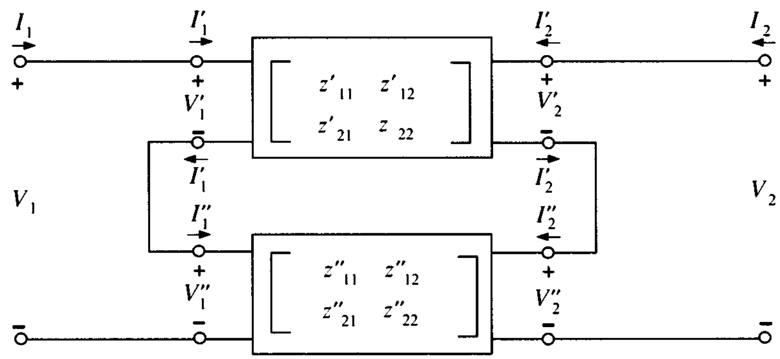
†8.12 Series and parallel connections of two-ports

Two ways of interconnecting two two-ports are shown in fig. 8.22: that in fig. 8.22(*a*) is the series connection, that in fig. 8.22(*b*) the parallel connection. Each way results in a composite two-port. In order to deduce the two-port parameters of the composite in terms of the individual two-port parameters before interconnection, it is important that the current flow is not affected by the interconnection.

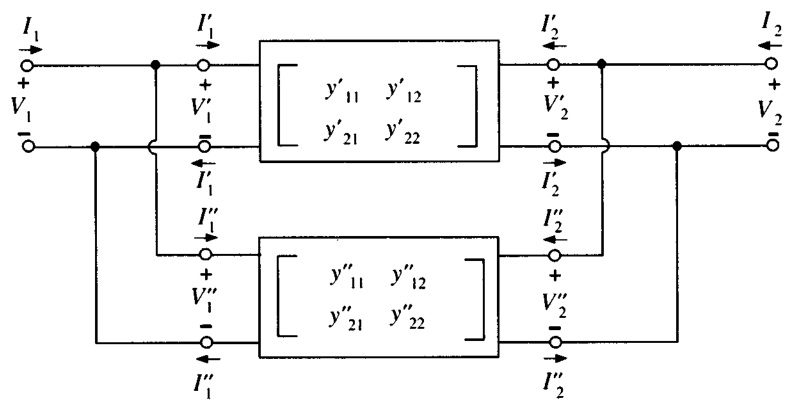
In the series connection, fig. 8.22(*a*), describing the individual two-ports by their impedance matrices as indicated in the figure, we have from (8.4)

$$V'_1 = z'_{11}I'_1 + z'_{12}I'_2$$
$$V'_2 = z'_{21}I'_1 + z'_{22}I'_2$$
$$V''_1 = z''_{11}I''_1 + z''_{12}I''_2$$
$$V''_2 = z''_{21}I''_1 + z''_{22}I''_2$$

Fig. 8.22. Interconnection of two-port networks.



(*a*) Series connection



(*b*) Parallel connection

The interconnection imposes the following relations

$$V_1 = V'_1 + V''_1$$
$$V_2 = V'_2 + V''_2$$
$$I_1 = I'_1 = I''_1$$
$$I_2 = I'_2 = I''_2$$

Hence

$$V_1 = (z'_{11} + z''_{11})I_1 + (z'_{12} + z''_{12})I_2$$
$$V_2 = (z'_{21} + z''_{21})I_1 + (z'_{22} + z''_{22})I_2$$

showing that the impedance matrix of the composite two-port is the sum of the individual impedance matrices.

For the parallel connections the following relations are imposed

$$V_1 = V'_1 = V''_1$$
$$V_2 = V'_2 = V''_2$$
$$I_1 = I'_1 + I''_1$$
$$I_2 = I'_2 + I''_2$$

The description of the two-ports by the admittance parameters, equation (8.1), combined with these relations show that the admittance matrix of the composite is the sum of the individual admittance matrices

$$\begin{bmatrix} y'_{11} + y''_{11} & y'_{12} + y''_{12} \\ y'_{21} + y''_{21} & y'_{22} + y''_{22} \end{bmatrix}$$

†8.13 Worked example

Find the conditions in the twin-T circuit of fig. 8.23(*a*) so that an input signal does not give rise to any output.

Solution

From (8.1) the conditions for no output from a two-port is $y_{12} = y_{21} = 0$, effectively disconnecting the input from the output. The circuit of fig. 8.23(*a*) is reciprocal, so that a physical interpretation of y_{12} is the negative of the admittance of the series element in the equivalent π-circuit. Accordingly the easiest way to proceed is to use the T-π equivalence in section 8.8 to find π-networks for each of the T-components of fig. 8.23(*a*). These are shown in figs. 8.23(*b*) and (*c*), and combined in fig. 8.23(*d*) to give the π-equivalent of the twin T-circuit. Note that this circuit could not simply be made since it involves a resistance which is both negative and varies with frequency.

The condition $y_{12} = 0$ then implies

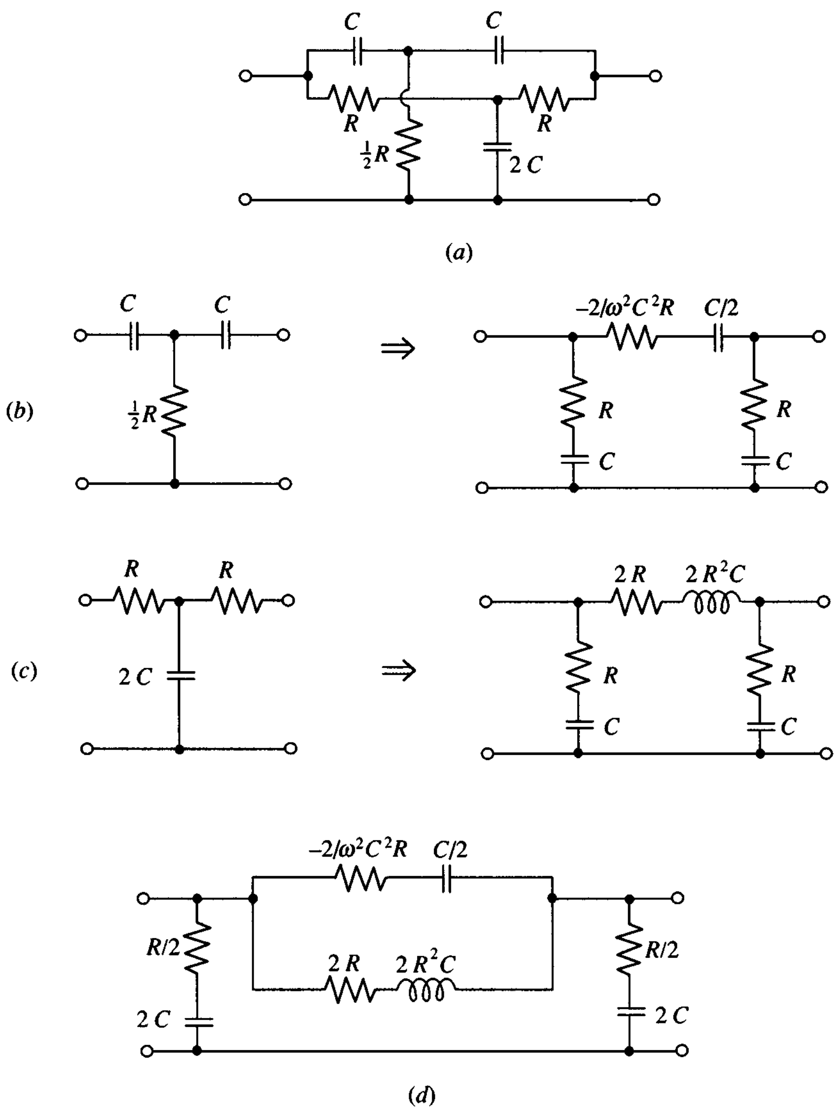
$$\left(-\frac{2}{\omega^2 C^2 R} + \frac{2}{j\omega C}\right)^{-1} + (2R + j\omega 2R^2 C)^{-1} = 0$$

or

$$-\frac{1}{\omega^2 C^2 R}+\frac{1}{j\omega C}=-(R+j\omega R^2 C)$$

Both real and imaginary parts of this equation are satisfied for $\omega CR=1$, which is the required condition.

Fig. 8.23. Circuits for worked example (section 8.13).



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†8.14 Iterative and image impedances

Although equation (8.26) provides a way of determining the overall *ABCD* matrix of any number of two-ports in cascade the process is clearly laborious. The process can be made simpler in certain cases, leading to the concept of iterative and image impedances.

8.14.1 Iterative impedances

This impedance relates to a cascade of identical two-ports, fig. 8.24(*a*): if a value of Z_L exists for which the input impedance to a two-port is also Z_L then clearly we may consider each two-port in the cascade separately. The impedance if this condition is true is known as an iterative impedance, of which in general there are two, one for each direction. The two possibilities are indicated in fig. 8.24(*b*), (*c*).

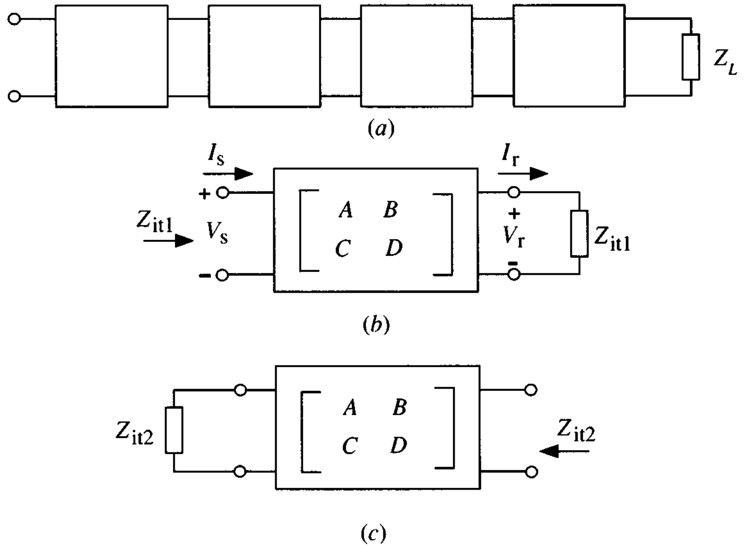
Consider the situation in fig. 8.24(*b*). We have

$$V_s = AV_r + BI_r$$
$$I_s = CV_r + DI_r$$
$$V_r = Z_{it1} I_r$$

Hence we must have

$$Z_{it1} = \frac{V_s}{I_s} = \frac{AZ_{it1} + B}{CZ_{it1} + D}$$

Fig. 8.24. Illustrating iterative impedances.



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or

$$CZ_{it1}^2 + (D-A)Z_{it1} - B = 0$$

whence

$$Z_{it1} = \frac{1}{2C}[A - D \pm \sqrt{\{(D-A)^2 + 4BC\}}] \tag{8.38}$$

Carrying out a similar process for the situation in fig. 8.24(c) we find

$$Z_{it2} = \frac{1}{2C}[D - A \pm \sqrt{\{(D-A)^2 + 4BC\}}] \tag{8.39}$$

In each case we shall choose a value with positive resistive part. If the network is symmetrical, $A = D$ and

$$Z_{it1} = Z_{it2} = \sqrt{(B/C)} \tag{8.40}$$

8.14.2 Image impedances

The concept of iterative impedance outlined in the last section is of use only for cascades of identical two-ports. The situation may be broadened slightly by use of image impedances. The two image impedances of a two-port, Z_{I1}, Z_{I2}, are defined by the circuit configurations of fig. 8.25. For the case of fig. 8.25(a) we have

$$V_s = AV_r + BI_r$$
$$I_s = CV_r + DI_r$$
$$V_r = Z_{I2}I_r$$

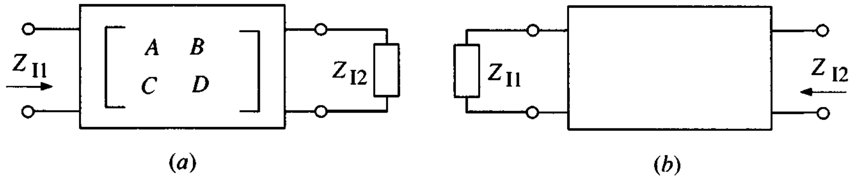
We require

$$V_s = Z_{I1}I_s$$

Hence

$$Z_{I1} = \frac{AZ_{I2} + B}{CZ_{I2} + D} \tag{8.41}$$

Fig. 8.25. Illustrating image impedances.



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In the case of fig. 8.25(b)

$$V_s = -Z_{I1} I_s$$

and we require

$$V_r = -Z_{I2} I_r$$

Hence

$$-Z_{I1} = \frac{-AZ_{I2} + B}{-CZ_{I2} + D} \tag{8.42}$$

Adding equations (8.41, 8.42) we find

$$Z_{I2} = \sqrt{\left(\frac{BD}{AC}\right)} \tag{8.43}$$

and

$$Z_{I1} = \sqrt{\left(\frac{BA}{DC}\right)} \tag{8.44}$$

For a symmetrical network $A = D$ and we see that

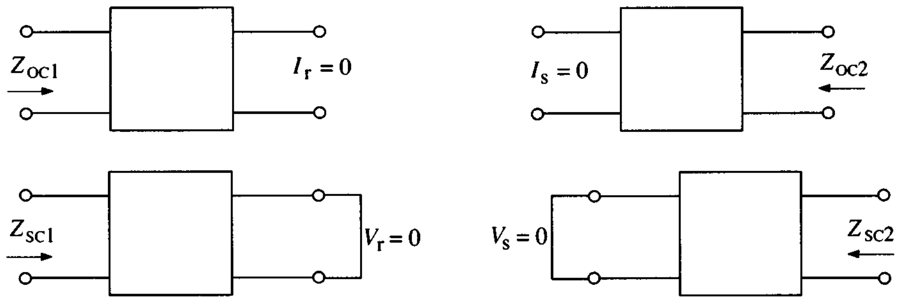
$$Z_{I1} = Z_{I2} = Z_{it1} = Z_{it2} = \sqrt{\left(\frac{B}{C}\right)}$$

This common value applying to a symmetrical network is frequently referred to as the *characteristic impedance*.

Equations (8.43, 8.44) may be more meaningfully expressed in terms of the open- and short-circuit impedances of the two-port, defined in fig. 8.26. Straightforward application of the $ABCD$ matrix equation shows

$$Z_{oc1} = \frac{A}{C};\ Z_{sc1} = \frac{B}{D}$$

Fig. 8.26. Definition of open- and short-circuit impedances.



$$Z_{oc2} = \frac{D}{C};\ Z_{sc2} = \frac{B}{A}$$

We see that for equation (8.44) we may write

$$Z_{I1} = \sqrt{(Z_{oc1} Z_{sc1})} \tag{8.45}$$

and for equation (8.43)

$$Z_{I2} = \sqrt{(Z_{oc2} Z_{sc2})}$$

The most straightforward application of these concepts is to attenuator circuits composed only of resistors.

†8.15 Attenuators

Consider the symmetrical T-network shown in fig. 8.27(*a*). For this a characteristic impedance, Z_0, exists given by

$$Z_0 = \sqrt{(Z_{oc} Z_{sc})}$$

We have

$$Z_{oc} = R_1 + R_2$$

$$Z_{sc} = R_1 + \frac{R_1 R_2}{R_1 + R_2} = \frac{R_1^2 + 2R_1 R_2}{R_1 + R_2}$$

Hence

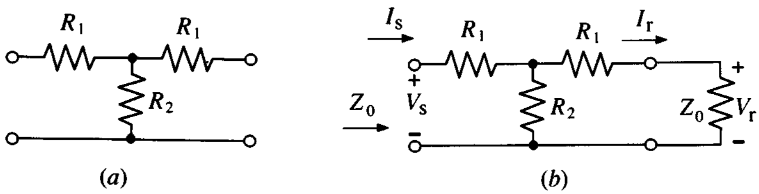
$$Z_0 = \sqrt{(R_1^2 + 2R_1 R_2)} \tag{8.46}$$

In use the attenuator section will be connected as in fig. 8.27(*b*), terminated in Z_0. Since by definition of Z_0, the impedance seen by the source V_s is also Z_0

$$I_s = \frac{V_s}{Z_0}$$

Thus the potential across R_2 is

Fig. 8.27. Attenuator section.



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$$V_s - \frac{R_1 V_s}{Z_0}$$

and finally

$$V_r = \frac{Z_0}{R_1 + Z_0} V_s \left(1 - \frac{R_1}{Z_0}\right)$$

or

$$\frac{V_s}{V_r} = \frac{Z_0 + R_1}{Z_0 - R_1} \tag{8.47}$$

The ratio

$$\frac{\text{power from source}}{\text{power to load}}$$

is usually measured in decibels and termed the attenuation A of the section

$$A = 10 \log_{10} \frac{V_s^2/Z_0}{V_r^2/Z_0}$$

$$= 20 \log_{10} \frac{Z_0 + R_1}{Z_0 - R_1} \tag{8.48}$$

†8.16 Worked example

Design an attenuator section having a characteristic impedance of 600 Ω with attenuation of 10 dB.

Solution

From equation (8.48)

$$\frac{Z_0 + R_1}{Z_0 - R_1} = 10^{\frac{1}{2}}$$

whence

$$\frac{R_1}{Z_0} = 0.519$$

or

$$R_1 = 311\,\Omega$$

Using equation (8.46)

$$R_2 = \frac{Z_0^2 - R_1^2}{2R_1} = 423\,\Omega$$

Consider the L-section of fig. 8.28. The T-section just designed can be regarded as two of these sections back-to-back. We now determine the image and iterative impedances for this section. From (8.45):

$$Z_{I1}^2 = (311 + 846)311 \qquad Z_{I1} = 600$$

$$Z_{I2}^2 = 846\left(\frac{1}{311} + \frac{1}{846}\right)^{-1} \qquad Z_{I2} = 439$$

The complete T-section is shown in fig. 8.28(*b*) and illustrates the use of image impedances: the right-hand section is terminated in its correct image impedance of 600 Ω and its input has impedance 439 Ω. This is the correct image impedance with which to terminate the left-hand section so that its input impedance is 600 Ω.

To evaluate the iterative impedance the *ABCD* parameters may be determined using table 8.1, but it is simpler to proceed directly from the circuit definition of fig. 8.24(*b*), (*c*). We have

$$Z_{it1} = 311 + \left(\frac{1}{Z_{it1}} + \frac{1}{846}\right)^{-1}$$

whence

$$Z_{it1}^2 - 311Z_{it1} - 311 \times 846 = 0$$

Choosing the positive root

$$Z_{it1} = 691\,\Omega$$

Similarly

$$\frac{1}{Z_{it2}} = \frac{1}{846} + \frac{1}{Z_{it2} + 311}$$

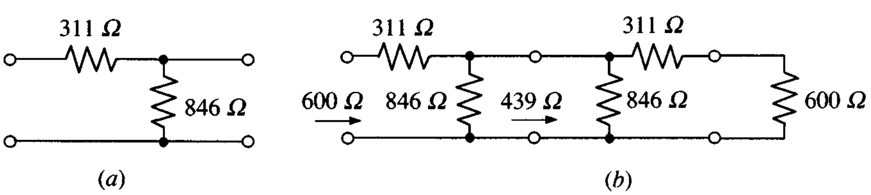
whence

$$Z_{it2}^2 + 311Z_{it2} - 311 \times 846 = 0$$

giving

$$Z_{it2} = 380\,\Omega$$

Fig. 8.28. Circuits for worked example (section 8.16).



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†8.17 Insertion loss

A principal procedure in electrical circuits is feeding power from a source to a load as indicated in fig. 8.29(*a*), in which the source and load impedances have been taken to be resistive. Frequently a two-port may be interposed between source and load, perhaps as a filter, and the voltage across the load will be a new value V_L (which may be calculated if parameters of the two-port are known). The ratio

$$\frac{V_{LO}}{V_L}$$

is known as the *insertion loss*. It is usually measured in decibels

$$I = 10\log_{10}\left(\frac{V_{LO}^2/R_2}{V_L^2/R_2}\right) = 20\log_{10}\left(\frac{V_{LO}}{V_L}\right) \tag{8.49}$$

It is clear that the attenuator section designed in section 8.16 has, when operated between source and load impedances of 600 Ω, an insertion loss of 10 dB.

†8.18 Worked example

The attenuator section designed in section 8.16 is mistakenly worked between source and load of 50 Ω. Determine the insertion loss.

The circuit is shown in fig. 8.30. The simplest way to determine the output voltage is to proceed as follows: 423 Ω in parallel with (311 + 50) Ω is 195 Ω.

Fig. 8.29. Illustrating insertion loss.

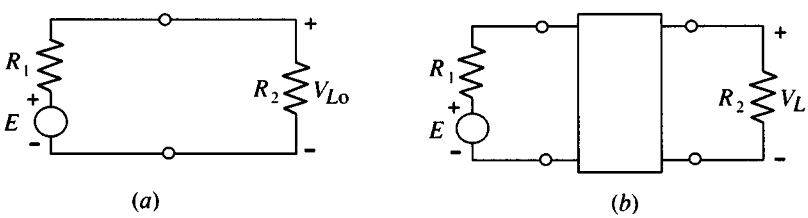
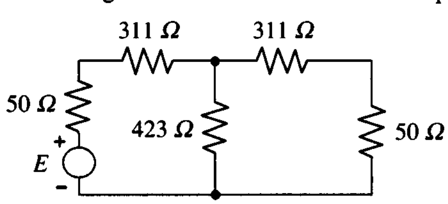


Fig. 8.30. Circuit for worked example (section 8.18).



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Thus

$$V_L = \frac{50}{(311+50)} \times E \times \frac{195}{50+311+195} = 0.0486\,E$$

Since $V_{L0} = 0.5\,E$, the insertion loss is

$$\frac{0.5}{0.0486} = 10.3$$

or

$$I = 20.2\,\text{dB}$$

8.19 Summary

The two-port network, or two-terminal pair network, is one of the most frequently used circuit configurations found in electrical and electronic engineering practice. The theory of such networks relates the voltage and current variables at the two ports of the network; depending upon which two of these four variables is chosen to be the independent variables, six possible sets of parameters may be defined, any one of which completely characterizes the behaviour of the network so far as externally impressed voltages and currents are concerned. Any of the sets of parameters may be expressed in terms of any other set, however, for a particular application, one of the six sets of parameters is often found to be the most convenient and is chosen in preference to the others.

For each parameter set, equivalent circuits may be derived which conform to the two circuit equations corresponding to that particular parameter set. The elements (sources and impedances) of these equivalent circuits are functions of the parameters and of the terminal variables. Such equivalent circuits are of great practical value in the analysis of circuits part of which consists of a two-port network. They are also commonly used as a basis for modelling the small-signal characteristics of devices such as transistors.

A recurring problem in circuit analysis is to determine the voltage–current relationships between input and output of several two-port networks connected in cascade. This may be achieved by finding the *ABCD* parameters (modified transmission parameters) of each individual two-port and expressing these in matrix form – the so-called chain matrix. Multiplication of the individual chain matrices yields the overall matrix for the cascade from which voltage–current relationships between input and output may be found. Series and parallel interconnections of two-ports also arise (fig. 8.22) and for these cases matrix addition of, respectively, the impedance and admittance parameters (expressed in matrix form) is an appropriate technique for determining the overall properties of the interconnected networks.

Finally, the concepts of iterative and image impedances are useful for circuits consisting of identical two-ports connected in cascade, and when it is desired to achieve matching between a source and a load by means of a two-port network.

8.20 Problems

1. Find the hybrid parameters of the circuit shown in fig. 8.10.

2. Show that if a two-port network, described by its hybrid parameters, is reciprocal then $h_{12} = -h_{21}$. (Hint: apply the Reciprocity theorem to the relations (8.8).)

3. Find the z-parameters of the circuit shown in fig. 8.7; hence, express the elements of this circuit in terms of its z-parameters.

4. Determine the y-parameters for the circuit shown in fig. 8.31.

5. (a) Obtain the transmission ($ABCD$) matrices for the networks shown in fig. 8.32. If the two are connected in cascade, obtain the overall $ABCD$ matrix.

Fig. 8.31. Circuit for problem 4.

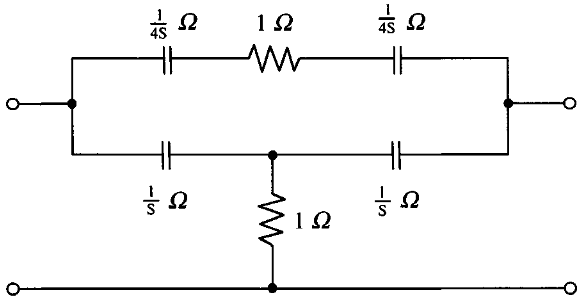
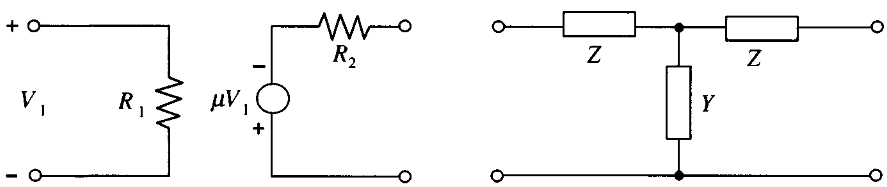


Fig. 8.32. Circuit for problem 5.



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(b) If $R_1 = 100\,\Omega$; $R_2 = 1\,\mathrm{k}\Omega$; $Y = \mathrm{j}100\,S$; $Z = \mathrm{j}20\,\Omega$ and $\mu = 20$, calculate the overall current gain when the output is short-circuited.
(University of Kent)

6. Derive the transfer ($ABCD$) matrix of:
(a) a simple series impedance;
(b) a simple shunt admittance.
Using these transfer matrices derive any one matrix representation of the parallel twin-tee network shown in fig. 8.33. Prove any matrix conversion you require.

What is the condition for infinite attenuation for this network?
(Sheffield University)

7. (i) For the cascade connection of the two-port networks shown in fig. 8.34(a), show that the short-circuit transfer admittance of the overall circuit is given by

$$y_{12} = -\frac{(y_{12})_{\mathrm{A}}(y_{12})_{\mathrm{B}}}{(y_{11})_{\mathrm{B}} + (y_{22})_{\mathrm{A}}}$$

(ii) Using this result or otherwise, find the transfer admittances of the network shown in fig. 8.34(b) ($T = RC$).
(University of Wales)

8. Find the iterative and image impedances of the circuit shown in fig. 8.35.

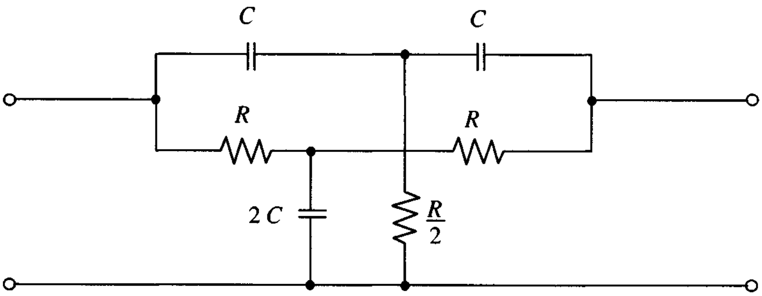
9. Show that when the symmetrical two-port described by the matrix

$$\begin{bmatrix} A & B \\ C & A \end{bmatrix}$$

is terminated in its image impedance, the ratio $V_{\mathrm{in}}/V_{\mathrm{out}}$ is given by

$$A + \sqrt{(A^2 - 1)}$$

Fig. 8.33. Circuit for problem 6.



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Use this result to find the ratio V_{in} V_{out} for the circuit shown in fig. 8.36 when it is terminated in its image impedance. Evaluate this ratio and the image impedance if $R = 1\,k\Omega$, $L = 1$ H, and $\omega = 100^3$ rad/s.

10. The insertion loss of a two-port is defined as:

$$\frac{V_{out} \text{ with network removed}}{V_{out} \text{ with network inserted}}$$

Show that for the circuit given in fig. 8.37 the insertion loss is:

$$\frac{(z_{11}+Z_s)(z_{22}+Z_r)-z_{12}{}^2}{z_{12}(Z_r+Z_s)}$$

(Manchester University)

Fig. 8.34. Circuit for problem 7.

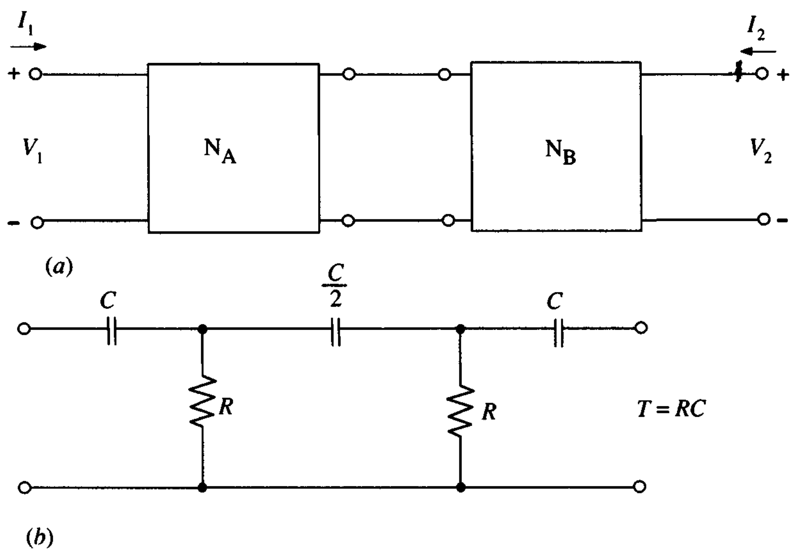

Fig. 8.35. Circuit for problem 8.

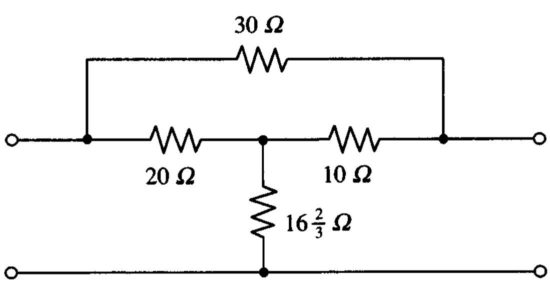

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Fig. 8.36. Circuit for problem 9.

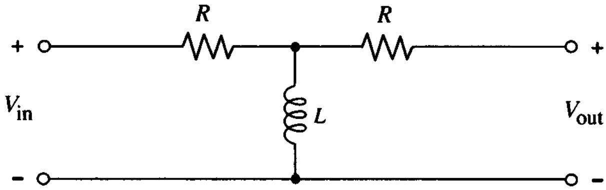
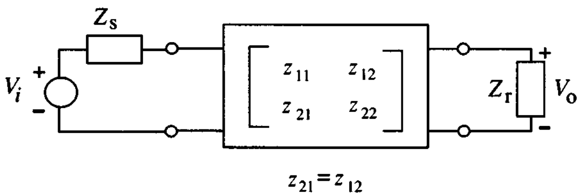


Fig. 8.37. Circuit for problem 10.



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