8 Power Supplies and Storage

8.1 Introduction

Electronic circuits are designed to operate with certain voltage supply levels, ranging typically from 0.9 V to 5 V for low-power circuits related to wireless communication and sensing applications. Therefore, the output of an energy harvesting device must be converted to a suitable supply voltage in order to power the electronics connected to it. Power converter circuits are necessary both in order to convert the energy harvester output to a desired useful voltage value but also to regulate the output voltage of the energy harvester to a constant value insensitive to variations. Power converter circuits are classified into regulated or unregulated depending on whether they have functionality to maintain a constant output voltage and attenuate any ac ripple or variation at their input. One characteristic measure of a regulator is the line regulation (LNR) expressed as the ratio of the output voltage variation ΔV_L to a corresponding change in the input voltage ΔV_i at a constant output current I_L and temperature T_A,

$$\text{LNR} = \left.\frac{\Delta V_L}{\Delta V_i}\right|_{I_L, T_A = \text{const.}} \tag{8.1}$$

The line regulation is typically measured in mV/V.

When the input power to the harvester device is very small, it is often the case that the output voltage of the energy harvester is less than the desired operating voltage. This is the case, for example, of an RF energy harvester, a rectenna comprising a single-diode rectifier when the input power to the rectifier is in the order of −20 dBm or less (see Section 7.4). Alternatively, certain types of energy harvesters such as electrostatic or piezoelectric energy harvesters (see Section 4.6) provide very high voltage values at their output that need to be converted to a lower value suitable for the subsequent electronic circuits. Power converter circuits are also classified as step-down or step-up, depending on whether they provide an output voltage that has a value that is less or higher than the voltage applied at its input respectively. Power converter circuits may have both a step-down and step-up functionality, as we will see in the next sections.

Finally, power converter circuits are classified into linear or switched mode depending on their operating principle. There are other ways to classify power converters, and furthermore, both linear and switching power converters can be

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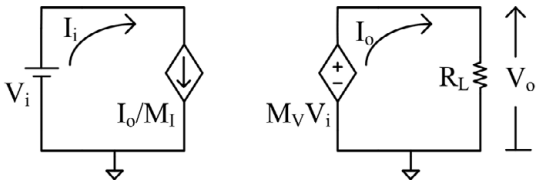

Figure 8.1 Simple circuit model of a dc–dc power converter.

classified into subcategories based on their topology and functionality [232]. One of the most important characteristics of the dc–dc power converter circuits is the efficiency η defined as

$$\eta = \frac{P_L}{P_i} = \frac{P_L}{P_L + P_d}, \tag{8.2}$$

where P_L is the dc power delivered to a load R_L connected at its output and P_i is the input power to the power converter circuits, which, in contrast to the energy harvester circuits of the previous chapters, is also a dc electrical power same as the output power P_L. P_d is the dissipated power of the dc–dc converter circuit given by

$$P_d = \left(\frac{1}{\eta} - 1\right) P_L. \tag{8.3}$$

The dc voltage and current gain of a dc–dc converter are defined as

$$M_V = \frac{V_L}{V_i} \tag{8.4}$$

$$M_I = \frac{I_L}{I_i}. \tag{8.5}$$

Using the preceding gain expressions, the efficiency can be expressed as

$$\eta = M_V M_I. \tag{8.6}$$

This way, one can define a dc circuit model of a dc–dc power converter as shown in Figure 8.1 [232].

The input dc resistance of the switched mode converter is defined as

$$R_i = \frac{V_i}{I_i}. \tag{8.7}$$

Using (8.4) through (8.6), one can write

$$R_i = R_L \frac{\eta}{M_V^2} \approx \frac{R_L}{M_V^2}. \tag{8.8}$$

An ideal switched mode converter has an efficiency of 100%, and therefore, using (8.8), we can find the input resistance of a switched mode converter based on the output load and the voltage gain.

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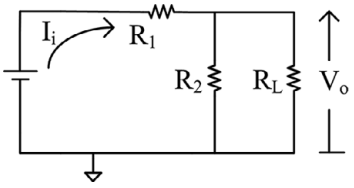

Figure 8.2 Step-down converter principle using a resistive voltage divider circuit.

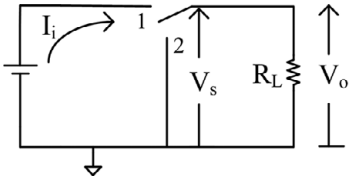

Figure 8.3 Step-down converter principle using an SPDT switch [233].

The simplest type of a step-down dc–dc power converter circuit is a resistive voltage divider circuit, shown in Figure 8.2. It is well known that the load voltage V_L is related to the input voltage by the simple formula

$$V_L = \frac{R_L /\!/ R_2}{R1 + R_L /\!/ R_2} V_i. \tag{8.9}$$

The circuit of Figure 8.2, albeit simple, typically results in low efficiency due to the power dissipated in resistors R_1 and R_2. Alternatively, one can produce a lower dc value using the circuit topology of circuit (8.3) [233]. A single-pole double-throw (SPDT) switch is used to connect the output load R_L for a fraction D of a period T_s of a control voltage v_s to the input voltage V_i, while it shorts the load to the ground for the remaining fraction $1 - D$ of the period of v_s. It is easy to verify that the average (dc) output voltage is equal to

$$V_L = \frac{1}{T_s} \int_0^{T_s} v_L(t) dt = DV_i. \tag{8.10}$$

A switch device connects, in a closed position, or disconnects, in an open position, a galvanic electrical path in a circuit. In its simple form, it has two contacts or terminals. Fundamental electrical switch components are a diode and a transistor device. A control signal is necessary to set the switch to the closed or open state. In the case of the diode, the control signal is the voltage, which is applied to its terminals, whereas in a transistor device it can be a voltage or a current applied to its third terminal, depending on the transistor technology. The number of poles represents how many switch circuits are controlled simultaneously by the control signal. The number of throws defines how many different closed paths are adopted by the switch. In the case of Figure 8.3, there is one circuit, hence a single pole switch is used, and furthermore there are two closed paths involved, hence the switch is a double throw switch. The elementary diode

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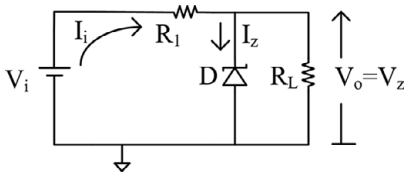

Figure 8.4 Step-down converter using a Zener diode.

and transistor components define single-pole single-throw (SPST) switches. An SPDT switch can be constructed from two elementary SPST switches that are controlled by a single control signal. As we will see in Section 8.3, the SPDT switches of switched mode dc–dc power converters are commonly implemented using a combination of a transistor and a diode device.

If there is no power dissipated in the switch, one can achieve a very high efficiency switched mode dc–dc power converter. This is done at the expense of an increased circuit complexity, in terms of the control signal circuitry and filtering circuitry in order to attenuate signal components created by the switching process at the switching frequency harmonics. One however must also consider the power lost in implementing the switching signal, which lowers the efficiency and could be important in implementing energy harvesting circuits.

8.2 Linear Power Converters

Linear power converters are step-down power converters. The simplest form of a regulated step-down dc–dc power converter is one using a Zener diode in place of the resistor R_2 of Figure 8.2, as shown in Figure 8.4. When the input voltage is larger than the Zener breakdown voltage V_Z, the output voltage V_L remains constant at V_Z. It therefore forms a regulated step-down supply. Naturally, all the power that is dissipated in the Zener diode $P_d = V_Z I_Z$ is lost. The efficiency of the supply is reduced as the difference between the input and output voltage is increased.

The Zener diode represents a variable resistor connected in parallel to the output load. The variation of the resistance of the Zener diode results in the regulation of the output load voltage. Alternatively, one can implement a variable resistor using a transistor device that is biased in its active region [232, 233]. The resulting circuit is a linear regulator circuit. A bipolar transistor biased in its active linear region can be used in place of either the resistor R_1 or R_2, resulting in a series or shunt linear regulator topology as shown in Figure 8.5 [232].

In Figure 8.5, a feedback loop is created using a voltage divider comprising resistors R_1 and R_2 which sense the output voltage and compare it to a reference value V_{ref} with the help of an operational amplifier. The output of the amplifier drives the base of the bipolar transistor, thus controlling its collector current. This way, the collector to emitter resistance of the transistor changes according

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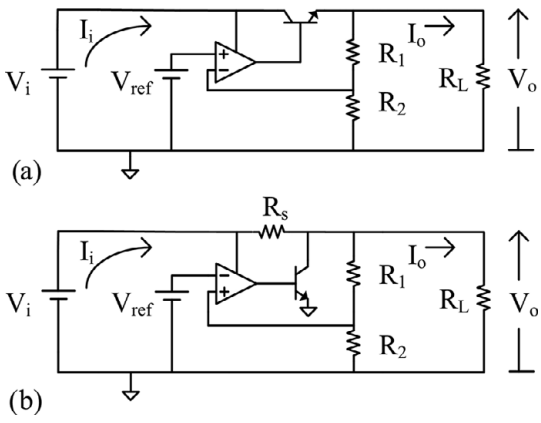

Figure 8.5 Linear voltage regulators: (a) series and (b) shunt topologies.

to the output voltage, thus maintaining a regulated output voltage V_L. In the case of the series linear regulator, the output voltage V_L is calculated as follows:

$$V_{R_2} = \frac{R_2}{R_1 + R_2} \approx V_{ref} \tag{8.11}$$

$$V_L = \left(\frac{R_1}{R_2} + 1\right) V_{ref}. \tag{8.12}$$

The output voltage is determined by the feedback resistive divider and the reference voltage. Furthermore, the efficiency of the linear regulator is easily calculated using the fact that $I_I \approx I_L$ as

$$\eta = \frac{P_L}{P_I} = \frac{V_L I_L}{V_i I_i} \approx M_V. \tag{8.13}$$

The closer the output voltage V_L is to the input voltage V_i, the higher the efficiency is. However, the efficiency can never become 100% due to the fact that there is always a small voltage drop V_{CE} associated with the transistor terminals. The minimum voltage difference between the input and the output voltage of the regulator is called the dropout voltage. The dropout voltage typically takes a value of 2V; however, there also exist low dropout (LDO) linear regulators with a dropout voltage as low as 0.1 V [232].

It is straightforward to compute the output voltage and the efficiency of the shunt linear regulator with similar circuit equations. The efficiency of the shunt linear regulator is less than the efficiency of the series linear regulator due to the fact that in addition to the transistor there is also power dissipated in resistor R_1 [232].

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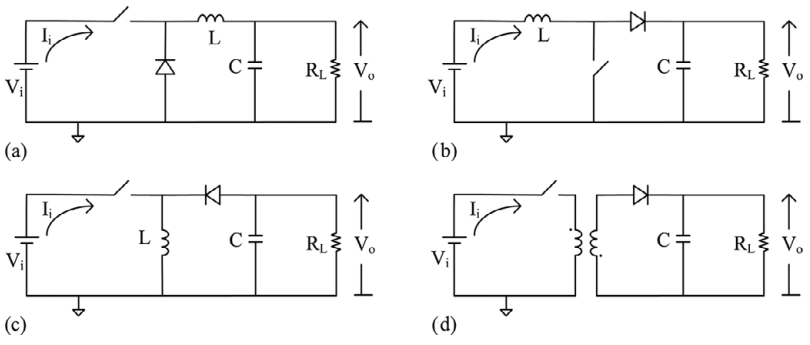

Figure 8.6 Switched mode power converter topologies: (a) buck, (b) boost, (c) buck-boost, and (d) flyback.

8.3 Switched Mode Power Converters

There exist a number of different switched mode power converter topologies. Some of the most common ones are the buck, boost, buck-boost, and flyback converter, all shown in Figure 8.6. The buck converter is a step-down converter, and the boost converter is a step-up converter, whereas the buck-boost and the flyback converters are step-up/down converters. The switch element in Figure 8.6 is an SPST switch comprising a transistor controlled by a periodic switching waveform. Combined with the second SPST switch comprising the diode, they implement the SPDT switch required for the converter circuit. The flyback converter is a buck-boost converter where the inductor has been substituted by a transformer. One should further note that the output voltage of the buck-boost converter has opposite polarity to the input voltage. There exist many more switched mode converter topologies [232, 233].

8.3.1 Steady-State Analysis

The steady state of the switched mode power converter circuits can be approximately analyzed employing three principles [233]. The first principle is the small ripple approximation, where it is assumed that under steady-state conditions, the ripple of the current and voltage at the circuit output node are small compared to the dc current or voltage and are ignored in the analysis. In other words,

$$v_L(t) = V_L + u_l(t) \approx V_L, \tag{8.14}$$

where V_L represents the average dc component and $v_l(t)$ the ac ripple component of the total output voltage $v_L(t)$. The second principle is that of inductor flux linkage balance or volt-second balance. This principle states that the average

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voltage through the inductor is equal to zero. This assumption is correct assuming an ideal inductor, where there are no thermal dissipation losses:

$$< v_L(t) >= \frac{1}{T_s}\int_0^{T_s} v_L(t)dt = 0. \tag{8.15}$$

The third assumption is the capacitor charge balance or ampere second balance, which defines that the average current through the capacitor is equal to zero:

$$< i_C(t) >= \frac{1}{T_s}\int_0^{T_s} i_C(t)dt = 0. \tag{8.16}$$

Applying these three principles, one can compute an estimate of important circuit parameters of the various switched mode converters under steady-state conditions, such as the voltage gain and efficiency. Furthermore, one can estimate the dc input resistance of the converter, which is essential when interfacing an energy harvester circuit such as a rectenna with a switched mode dc–dc converter in order for it to present an optimum load to the harvester circuit ensuring maximum power transfer. The steady state of switched mode power converter circuits is classified into two modes: the continuous conduction mode (CCM) and the discontinuous conduction mode (DCM) . In the former, the current in the magnetic energy storage component (inductor or transformer) is always nonzero, whereas in the latter it goes to zero for a fraction of the switching period T_s. The two modes result in substantial differences in the performance of the converter circuits, and they can be analyzed using the principles defined in this section. In the next sections, we will study the boost converter in detail and present a summary of the voltage gain and input resistance of the different converter topologies.

8.3.2 The Boost Converter

Let us analyze the steady state of the boost converter, shown again for completeness in Figure 8.7 [232, 233]. In the continuous conduction mode, the circuit takes one of two possible configurations based on the position of the switch, shown in Figure 8.8

Let us further assume that the switch is in the first position for a fraction D of the switching period T_s while it remains in the second position for a fraction $D_1 = 1 - D$. In the first position, the inductor voltage and the capacitor current are

$$\begin{aligned} v_L &= V_i \\ i_C &= -\frac{V_L}{R_L}, \end{aligned} \tag{8.17}$$

where the small ripple approximation has been invoked for the output voltage V_L according to (8.14). Similarly, during the second position of the switch, the inductor voltage and the capacitor current become

$$\begin{aligned} v_L &= V_i - V_L \\ i_C &= I_L - \frac{V_L}{R_L}. \end{aligned} \tag{8.18}$$

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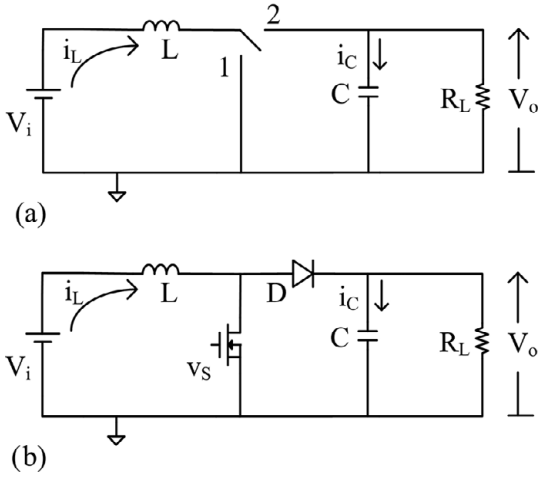

Figure 8.7 Boost converter circuit using (a) an ideal switch and (b) a switch implemented by a power transistor and a diode.

If we invoke the volt-second balance for the inductor L, we have

$$\frac{1}{T_s} = \int_0^{T_s} v_L(t)dt = V_i D + (V_i - V_L)D_1 = 0 \Rightarrow \frac{V_L}{V_i} = M(D) = \frac{1}{1-D}. \quad (8.19)$$

We can then solve for the voltage gain of the boost converter at CCM,

$$M(D) = \frac{V_L}{V_i} = \frac{1}{1-D}, \quad (8.20)$$

which is plotted in Figure 8.9.

Application of the capacitor charge balance gives an expression for the average inductor or output current

$$\frac{1}{T_s} = \int_0^{T_s} i_C(t)dt = -\frac{V_L}{R_L}D + \left(I_L - \frac{V_L}{R_L}\right)D_1 = 0 \Rightarrow I_L = \frac{V_L}{(1-D)R_L}. \quad (8.21)$$

The inductor current is the input current to the converter and therefore we can use it to calculate the input resistance of the boost converter as

$$R_i = \frac{V_i}{I_L} = \frac{(1-D)R_L}{M_V} = (1-D)^2 R_L. \quad (8.22)$$

The inductor L and capacitor C values are selected based on the maximum desirable or allowable current $2\Delta i_L$ (Figure 8.10) or voltage $2\Delta v_C$ (Figure 8.11) variation respectively. In each state, the inductor current has a linear slope that is determined by the equation for the current through the inductor. For example, the current slope in the first state is given by

$$v_L \approx V_i = L\frac{di_L}{dt} = L\frac{2\Delta i_L}{DT_s} \Rightarrow \frac{di_L}{dt} \approx \frac{2\Delta i_L}{DT_s} = \frac{V_i}{L}. \quad (8.23)$$

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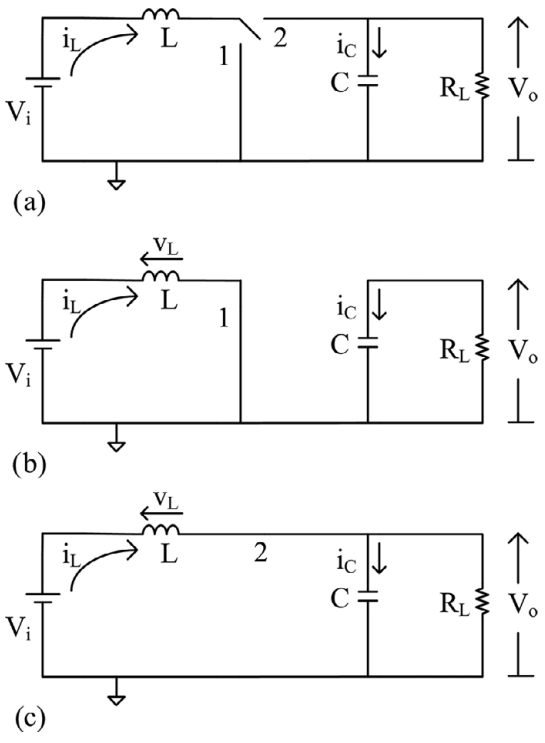

Figure 8.8 Boost converter circuit under CCM operation: (a) converter using an ideal switch, (b) switch in position 1, and (c) switch in position 2.

In the second state, the current slope is

$$\frac{di_L}{dt} \approx \frac{2\Delta i_L}{D_1 T_s} = \frac{V_i - V_L}{L}. \tag{8.24}$$

We can solve (8.23) for the inductance

$$L = \frac{V_i D T_s}{2\Delta i_L}. \tag{8.25}$$

Similarly, the capacitor voltage is linearly increasing and decreasing during the first and second states respectively, and the slope of the voltage curve can be determined from the capacitor current equation (Figure 8.11). The desired capacitor voltage variation Δv_C can be used to determine the capacitance value C. Specifically, during the first position the capacitance current equation takes the form

$$i_C \approx -\frac{V_L}{R_L} = C\frac{dv_C}{dt} = C\frac{-2\Delta v_C}{DT_s} \Rightarrow C = \frac{V_L D T_s}{2R\Delta v_C}, \tag{8.26}$$

which is solved for the capacitance value C.

In the DCM mode, the steady state comprises an additional interval D_2, where the current in the inductor is equal to zero. In this case, the three intervals sum to

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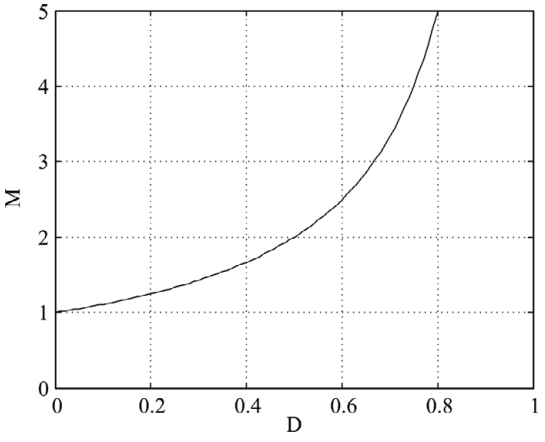

Figure 8.9 Boost converter voltage gain under CCM operation.

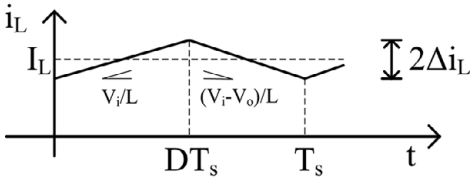

Figure 8.10 Boost converter steady-state current variation under CCM operation.

one period $D+D_1+D_2 = 1$. The current through the inductor in the three states is shown graphically in Figure 8.12. Comparing the inductor current curves in CCM (Figure 8.10) and DCM (Figure 8.12) modes, we can determine a boundary condition to distinguish between the two modes. In fact, the boundary between the two modes is when the average inductor current becomes equal to the current variation $I_L = \Delta i_L$. Using (8.21) and (8.23) for I_L and Δi_L respectively, we obtain

$$I_L = \Delta i_L \Rightarrow \frac{V_L}{(1-D)R_L} = \frac{V_i D T_s}{2L} \Rightarrow K = K_c = D(1-D)^2, \tag{8.27}$$

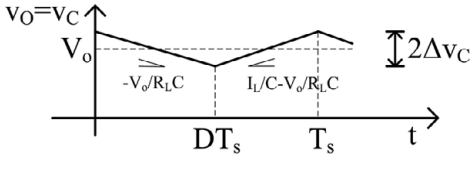

Figure 8.11 Boost converter steady-state output voltage variation under CCM operation.

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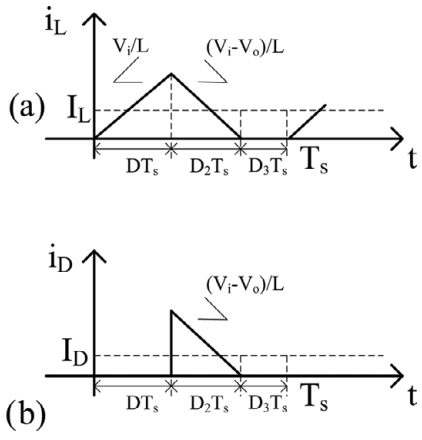

Figure 8.12 Boost converter (a) inductor and (b) diode current at DCM mode.

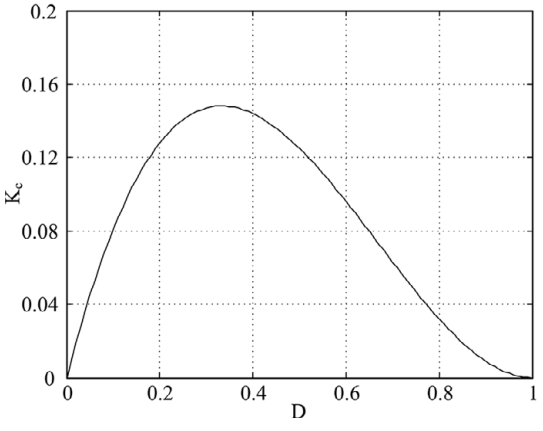

Figure 8.13 Critical value K_c defining the boundary between CCM and DCM.

where

$$K = \frac{2L}{R_L T_s}. \tag{8.28}$$

When $K > K_c$, the converter operates in CCM, and when $K < K_c$, the converter operates in DCM. The critical value $K = K_c = D(1-D)^2$ is plotted in Figure 8.13. Selection of $K > 0.1481$ guarantees operation in CCM mode for every fraction D of the switching period.

Having defined the boundary between CCM and DCM operation, we can now analyze the DCM operation. The equivalent circuit of the boost converter corresponding to the three states is shown in Figure 8.14. We proceed in the same way as in the CCM mode by writing the inductor current and the capacitor voltage equations in the three positions. The current and voltage equations in

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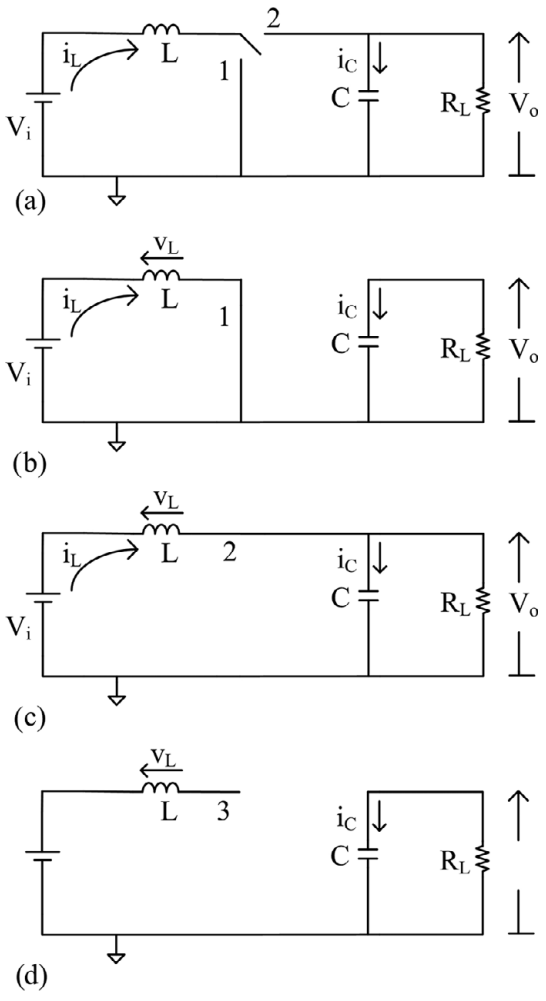

Figure 8.14 Boost converter equivalent circuit at DCM mode: (a) subinterval 1, (b) subinterval 2, and (c) subinterval 3.

the first and second switch positions at DCM are the same as in the CCM (8.17) and (8.18) valid for a fraction D and D_1 of the control signal period respectively. In the third switch position, we obtain

$$\begin{aligned} v_L &= 0 \\ i_C &= -\frac{V_L}{R_L}, \end{aligned} \tag{8.29}$$

valid for a third fraction D_2 of the control signal period. Invoking the volt-second balance for the inductor L, we have

$$\frac{1}{T_s}\int_0^{T_s} v_L(t)dt = V_i D + (V_i - V_L)D_1 + D_2 \cdot 0 = 0 \Rightarrow M(D) = \frac{D + D_1}{D_1}. \tag{8.30}$$

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In this case, however, we have $D + D_1 + D_2 = 1$, and therefore we need one more equation in order to obtain a relation between D_1 and D_2. This is done applying Kirchhoff's current law in the output node [233]:

$$i_D = i_C + \frac{v_L}{R_L} \Rightarrow < i_D >= I_D = \frac{V_L}{R_L}, \tag{8.31}$$

where we invoked the capacitor charge balance $< i_C >= 0$. The average diode current can be computed using the help of Figure 8.12. The diode current is equal to zero during position 1 and position 3, whereas it is equal to the inductor current during position 2 (Figure 8.14. The average current during position 2 is evaluated by computing the area under the triangle formed by the current plot and the time axis in Figure 8.12 and dividing it by the period T_s. The peak current I_p at the end of fraction D is found using the inductor current increase rate at position 1 from 8.26 as

$$I_p = \frac{V_i}{L} D T_s. \tag{8.32}$$

The average diode current is then found to be

$$I_d = \frac{1}{2} I_p D_1 T_s = \frac{V_i D D_1 T_s}{2L}. \tag{8.33}$$

Using this value in (8.31), we obtain

$$\frac{V_i D D_1 T_s}{2L} = \frac{V_L}{R_L} \Rightarrow V_i D D_1 = V_L K. \tag{8.34}$$

This is the equation relating D and D_1 that we needed. We can solve (8.34) for D_1 and substitute the result in (8.30) to obtain a quadratic equation for V_L

$$V_L^2 - V_L V_i - \frac{V_i^2 D^2}{K} = 0. \tag{8.35}$$

The voltage gain M_V in the DCM case is computed by solving (8.35) and selecting the positive root

$$M_V(D, K) = \frac{V_L}{V_i} = \frac{1 + \sqrt{1 + 4D^2/K}}{2}. \tag{8.36}$$

In the event $2D/\sqrt{K} \gg 1$

$$M_V(D, K) \approx \frac{D}{\sqrt{K}}. \tag{8.37}$$

The combined voltage gain plot for CCM and DCM operation is shown in Figure 8.15.

Once we have found the voltage gain of the boost converter, we can easily compute the input resistance using (8.8) as

$$R_i = \frac{4R_L}{\left(1 + \sqrt{1 + 4D^2/K}\right)^2}. \tag{8.38}$$

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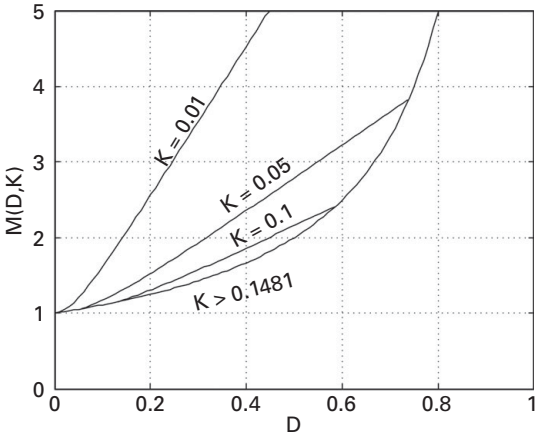

Figure 8.15 Boost converter voltage gain $M_V(D, K)$ for different values of K resulting in CCM or DCM operation.

The input resistance can be approximated as

$$R_i \approx \frac{R_L K}{D^2} \tag{8.39}$$

when $2D/\sqrt{K} \gg 1$.

8.4 Summary of Switched Mode Power Converter Properties

We can apply the small ripple approximation and volt-second and charge balance principles in the circuits of the buck and buck-boost converters in order to calculate the voltage gain and input resistance under CCM and DCM operation. The results are summarized in Tables 8.1 [233] and 8.2 [232, 233].

Table 8.1 Voltage gain of switched mode converters of Figure 8.6 [232, 233].

Converter	$K_c(D)$	$M_V(D)$ CCM	$M_V(D, K)$ DCM
Buck	$1 - D$	D	$\frac{2}{1+\sqrt{1+4K/D^2}}$
Boost	$D(1 - D)^2$	$\frac{1}{1-D}$	$\frac{1+\sqrt{1+4D^2/K}}{2}$
Buck-boost	$(1 - D)^2$	$-\frac{D}{1-D}$	$-\frac{D}{\sqrt{K}}$
Flyback	$n^2(1 - D)^2$	$\frac{D}{n(1-D)}$	$\frac{D}{n\sqrt{K}}$

In Table 8.1, n is the transformer turn ratio and $K = 2L/(T_s R_L)$ has been defined in (8.28). In the case of the flyback transformer, n is the transformer secondary to primary ratio, and the inductance $L = L_1/n^2$ used in K is the

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inductance L_1 of the transformer primary reflected in the secondary [232]. CCM operation corresponds to $K > K_c$.

The input resistance of the switched mode converters is found using (8.8) and summarized in Table 8.2.

Table 8.2 Input resistance of ideal switched mode converters of Figure 8.6 [232, 233, 234].

Converter	R_i CCM	R_i DCM
Buck	$\frac{1}{D^2}R_L$	$\frac{\left(1+\sqrt{1+4K/D^2}\right)^2}{4}R_L$
Boost	$(1-D)^2R_L$	$\frac{4}{\left(1+\sqrt{1+4D^2/K}\right)^2}R_L$
Buck-boost	$\frac{(1-D)^2}{D^2}R_L$	$\frac{K}{D^2}R_L$
Flyback	$\frac{(1-D)^2}{n^2D^2}R_L$	$\frac{n^2K}{D^2}R_L$

The product $KR_L = 2L/T_s$ cancels the output load R_L, and therefore the input resistance of the buck-boost and flyback converters in DCM operation is independent of the output load. It is straightforward to show that the same thing happens in buck and boost converters in DCM operation, when $2\sqrt{(K)}/D \gg 1$ or $2D/\sqrt{K} \gg 1$ respectively. This fact has been explored in [235] to design a 2.4 GHz rectifier circuit comprising a buck-boost converter that exhibited high efficiency over a wide range of load values.

In energy harvesting applications where the input available power is scarce, the design of the switching circuit is very challenging in order to minimize the power that is dissipated in the switching circuit itself, so that the overall circuit efficiency is not compromised. In [236], a rectifier with a boost converter operating in DCM with a very low-power switching circuit is demonstrated, harvesting ambient RF power used to power a thin film lithium battery. The boost converter operates with a $D = 0.5$ duty cycle provided by a two-stage oscillator circuit. The first oscillator is a low-frequency 250 Hz oscillator stage designed using a low-power comparator circuit. The first oscillator is used to power a second higher oscillating frequency stage with an oscillating frequency of approximately 100 KHz, which drives the gate of a power metal–oxide–semiconductor (MOS) transistor switch. The selected input resistance of the boost converter is 750 Ω. A circuit schematic representation is shown in Figure 8.16.

The oscillator circuit is powered from the output of the boost converter. One can therefore see the paradox in designing such circuits because the converter is designed to provide dc power but it also requires dc power itself in order to power the switching circuit, which is fundamental for its operation. The output energy storage component loading the converter circuit must therefore have a minimum stored energy in order for the energy harvester circuit to operate. An alternative circuit topology is to design the converter itself to comprise an oscillating input stage, which is powered by the input dc signal to the converter. Such oscillating

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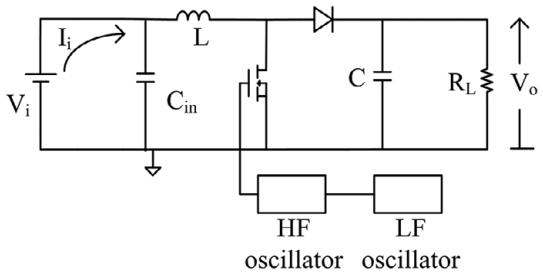

Figure 8.16 Representation of boost converter with a two-stage oscillating low-power switching circuit for ambient RF energy harvesting based on [236].

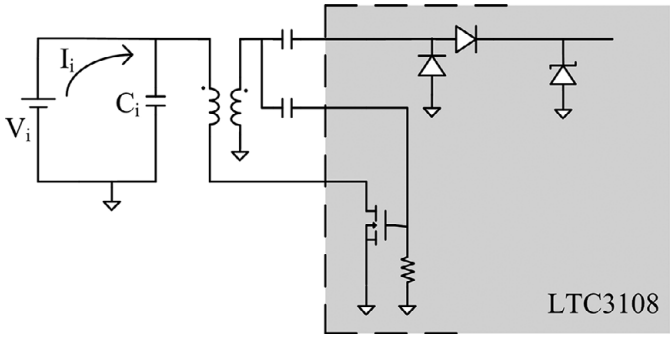

Figure 8.17 Representation of ultralow-power energy harvesting circuit LT3108 with an input oscillating converter stage, based on [106].

converter circuits have been proposed based on oscillating flyback converters that require very low dc input voltage in the order of tens of millivolts for the oscillation to start up. A popular such commercial circuit by Linear Technology designed for harvest thermoelectric energy harvesters is shown in Figure 8.17 [106]. When a transformer with a turns ratio of $n = 100$ is used, the oscillation can start with an input voltage as low as 20 mV [106]. Several similar circuits have been demonstrated in the scientific literature [237, 238, 239].

In Figure 8.17, we can also identify a Zener regulator circuit, which limits the voltage to values below 5.25 V and acts as overvoltage protection device [106]. In order to regulate the output voltage to a constant value, a feedback circuit was implemented (not shown in Figure 8.17) that sampled the output voltage using a resistive voltage divider and controlled the duty cycle of the switching waveform based on the difference between the sampled output voltage compared to a reference value. The voltage gain of the switching converter is directly dependent on the duty cycle of the switching waveform as shown in Table 8.1, and therefore the feedback circuit compensates any variations in the output voltage by adjusting the voltage gain of the converter in order to maintain a constant output voltage. The regulating control loop can be implemented either using analog circuitry

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or digital circuitry. In addition to regulation of the output voltage, a control loop may be designed in order to optimize the efficiency or the output power of the switching converter. Such loops are known as maximum power point tracking (MPPT) loops. MPPT tracking is commonly employed in solar energy harvesting systems [240] because the output power of the solar cell strongly depends on the output voltage, as we have seen in Figure 3.4. The tracking loop itself results in added complexity and unavoidably in added power dissipation, and therefore such loops are not typically employed in energy harvesting systems where the amount of harvested power is very low, such as in ambient RF energy harversting.

8.5 Batteries and Supercapacitors

The output of an energy harvesting is typically connected to some type of energy storage device. Commonly used energy storage devices are batteries or capacitors. Although the concept of energy harvesting is intimately related to the elimination or to the limitation of battery usage in order to mitigate the waste problems associated with spent batteries or the difficulty in certain application scenarios in substituting batteries, the time-varying nature of both the ambient energy forms and the power dissipation requirements of electronic devices requires the use of some form of energy storage device. In certain applications such as passive RFID tags [6, 241], a capacitor is sufficient to provide the required energy storage and completely eliminate the use of batteries. In typical application scenarios, however, a battery is still required. Supercapacitors share properties of capacitor and battery systems and can provide an attractive alternative to batteries. In this paragraph, we review some of the fundamental properties of battery and supercapacitor systems.

Batteries and supercapacitors are both electrochemical energy storage devices [242]. They both comprise two electrodes that are in contact with an electrolyte solution having positive and negative ions, as shown in Figure 8.18. An ion permeable separator membrane is used to separate the two electrodes in order to prevent electrical shorting between the electrodes. However, although in batteries the energy is generated by conversion of chemical energy through a redox reaction taking place at the surface of the two electrodes, this may not be the case in a supercapacitor, where ions form electrical double layers (EDLs) in the electrolyte–electrode interfaces that result in charge and consequently energy storage [242]. The two electrodes are called the anode and the cathode depending on whether they are at a higher or a lower electrical potential.

The amount of energy that is stored in an energy storage system is measured by the specific energy measured in watt-hours per kilogram (Wh/kg) or the energy density measured in watt-hours per liter (Wh/L). The power capability of the energy system is measured instead as specific power (W/kg) or power density (W/L). The different sets of energy and power measures are called gravimetric (per kg) or volumetric (per L) measures respectively. A Ragone

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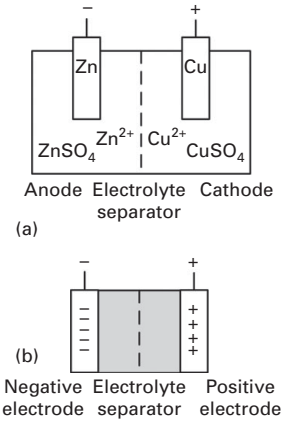

Figure 8.18 Schematic representation of (a) battery and (b) supercapacitor, based on [242].

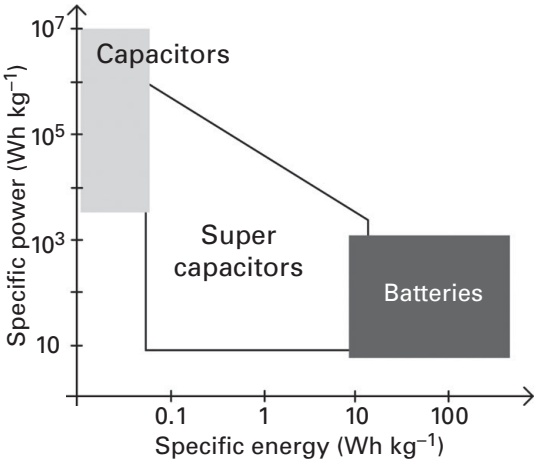

Figure 8.19 Ragone diagram of energy storage systems, based on [242].

diagram is used to compare the energy and power capability of an energy storage system. Such a Ragone diagram is shown in Figure 8.19. Batteries have a higher energy generation capability than supercapacitors, whereas supercapacitors have a higher power generation capability than batteries.

A primary battery is assembled in a charged state, and it is discharged when its terminals are connected to an electrical circuit. Primary batteries cannot be discharged. In contrast, a secondary battery is a rechargeable battery and it is usually assembled in a discharged state. Secondary batteries must be first charged before they are operated. A typical discharge curve of a battery looks like the one shown in Figure 8.20. When the terminals of a battery are open, the voltage of the battery takes its open-circuit voltage (OCV) value. When a load

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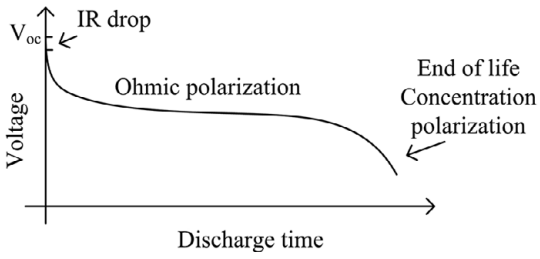

Figure 8.20 Representation of a battery discharge diagram, based on [242].

that draws some current is connected to its terminals, usually a small voltage IR drop is observed associated with the internal thermal resistance mechanisms of the battery such as electrolyte thermal resistance, contact resistance, electrode resistance, etc. The battery is then able to provide a relatively constant output voltage independent of the output current for a range of currents until a limiting value corresponding to the inability of the electrolyte redox reactions to provide further energy, where the battery output voltage begins to drop. The typical operating voltage of a battery under load is called the nominal voltage of the battery [243]. The end or cutoff voltage is the voltage of the battery at the end of the discharge. The nominal voltage of the battery depends on the battery technology and the topology (series/parallel) of the interconnected battery cells in a battery system.

The capacity C of the battery is a measure of the charge stored by the battery. It is measured in ampere-hour (Ah). Together with the nominal voltage, they represent (arguably) the most important characteristics of the battery. The C rate is typically used to represent the discharge (and the charge) current of a battery [243]. The C rate is expressed via the equation

$$I = M \times C_n, \tag{8.40}$$

where I is the current (A), C is the rated battery capacity (in Ah), n is the time base in hours for which the rated capacity is declared, and M is a multiple or fraction of C. For example, the $0.1C$ or $C/10$ discharge rate of a 1,000 mAh rated battery is 100 mA. Conversely, a 1,000 mAh rated battery discharged at the $0.2C$ or $C/5$ rate is discharged at 250 mA.

Finally, the $0.1C$ discharge rate for a battery rated at 1,000 mAh at a 5 h rate is designated as $0.1C_5 = 100$ mA [243]. Such a battery is capable of delivering 100 mA for a 5 h time interval. The capacity of the battery must not be estimated by scaling linearly a known rated value at different discharge conditions because the battery capacity typically decreases with increasing discharge current [243]. For example, the battery rated $0.1C_5 = 100$ mAh will run for more than ten hours when discharged at 50 mAh or it will run for less than one hour when discharged at its $C = 1{,}000$ mAh rate. Selected common commercial battery systems are listed in Table 8.3 [242]. It addition, lithium polymer (LiPo) batteries

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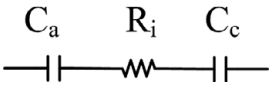

Figure 8.21 Electrical equivalent circuit of a supercapacitor.

are secondary batteries of lithium-ion technology which use a polymer electrolyte instead of a liquid electrolyte. LiPo batteries have found an increasingly large application in mobile and portable electronic devices especially due to their lower weight compared to other battery technologies.

Table 8.3 Selected commercial battery systems [242].

Name	Nominal voltage	Anode	Cathode	Electrolyte
Primary				
Alkaline	1.5	Zinc powder	Electrolytic MnO_2	aq KOH
Zinc – air	1.2	Zinc powder	Carbon (air)	aq KOH
Lithium – manganese dioxide	3.0	Lithium foil	treated MnO_2	$LiCF_3SO_3$ or $LiClO_4$
Secondary				
Lead acid	2.0	Lead	PbO_2	aq H_2SO_4
Nickel – cadmium	1.2	Cadmium	NiOOH	aq KOH
Lithium ion	4.0	Li(C)	$LiCoO_2$	$LiPF_6$

The electrical equivalent circuit of a supercapacitor, otherwise known as an ultracapacitor, is shown in Figure 8.21. The overall capacitance of the supercapacitor device is the series connection of two capacitances associated with the two double layers formed at the anode and the cathode electrode of the supercapacitor. The series resistance represents internal thermal losses of the supercapacitor, similarly to the battery. Due to the series connection of the capacitances, the overall capacitance C of a symmetric supercapacitor comprising electrodes of the same material is reduced in half compared to the capacitance of the single anode C_a and cathode C_c electrodes [242].

$$\frac{1}{C} = \frac{1}{C_a} + \frac{1}{C_c} \Rightarrow C = \frac{C_a}{2} = \frac{C_c}{2}. \tag{8.41}$$

The voltage of supercapacitors using an aqueous electrolyte is approximately 1 V, whereas using an organic-based electrolyte results in a voltage of approximately 2.7 V. Asymmetric supercapacitors comprise a battery electrode as one of the electrodes, for example the cathode electrode, which due to the redox reaction comprises a capacitance approximately ten times larger than the electrical double

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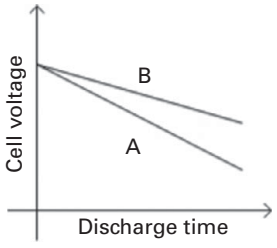

Figure 8.22 Supercapacitor discharge diagram [242].

layer capacitance. As a result, the overall capacitance of the series connection is approximately equal to the capacitance of the electrical double layer capacitance,

$$\frac{1}{C} = \frac{1}{C_a} + \frac{1}{C_c} \approx \frac{1}{C_a} + \frac{1}{10C_a} \Rightarrow C \approx C_a. \tag{8.42}$$

Asymmetric supercapacitors therefore achieve approximately double capacitance values compared to their symmetric counterparts. Finally, the output voltage of a supercapacitor reduces linearly with time, as shown in Figure 8.22. This behavior is different from batteries as compared to Figure 8.20. As we can see in Figure 8.22, the discharge slope is smaller in the case of asymmetric supercapacitors.

8.6 Problems and Questions

1. Describe what is a linear and a switch mode power converter.
2. What are the three principles used to analyze approximately the performance of switching power converters?
3. What is the inductor flux linkage balance or volt-second balance?
4. What is the capacitor charge balance or ampere-second balance?
5. Describe what is the continuous conduction mode (CCM) and the discontinuous conduction mode (DCM) of a switched mode power converter.
6. Compute the voltage gain and input resistance of a buck converter in CCM operation.
7. Compute the voltage gain and input resistance of a buck converter in DCM operation.
8. Compute the voltage gain and input resistance of a buck-boost converter in CCM operation.
9. Compute the voltage gain and input resistance of a buck-boost converter in DCM operation.
10. What is the capacity of a battery, and what is the C-rate specification of a battery?
11. How much is the $0.2C_{10}$ rate of a battery rated as 800 mAh at a 10 h rate?

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