7 Electromagnetic Energy Harvesting

7.1 Introduction

The recent interest in batteryless sensors and sensors with increased energy autonomy has led to the concept of ambient electromagnetic energy harvesting or energy scavenging, where rectennas [127] are used as sources of dc electrical power by capturing available RF power from existing ambient low-power electromagnetic sources not intentionally transmitting to power a sensor and converting it to dc electrical power [132, 134]. We classified in Chapter 6 as energy harvesting the wireless power transmission scenarios operating in low power levels, which is typically the case when we are trying to power a sensor from an ambient RF signal.

7.2 Ambient Electromagnetic Energy

The average magnitude of the power density S of a plane electromagnetic wave with electric field E propagating in a medium of characteristic impedance η is

$$S = \frac{1}{2\eta}|E|^2. \tag{7.1}$$

Ambient electromagnetic power density S is typically measured in $\mu W/cm^2$. Alternatively, one may specify the electrical field strength $|E|$ in V/m. The characteristic impedance of air is equal to $\eta = 377\ \Omega$. The symbol η is typically used both for the characteristic impedance of a medium and for efficiency measures; however, the characteristic impedance is only used in this section and in section 7.4 in the book and, furthermore, the text should be clear enough to avoid any confusion between the two. It is straightforward to show that an electric field of $1\ V/m$ in air corresponds to a power density of $0.26\ \mu W/cm^2$. The amount of ambient power density depends strongly on the application scenario and the environment that is under consideration. Therefore, it is bound to vary significantly between rural areas and cities where the number of operating wireless transmitters is very different. It addition, it is expected to strongly depend on frequency, based on the existing operating wireless communication systems, including TV, cellular, and Wi-Fi networks, to name a few. Measurement

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campaigns have appeared in the literature aiming to estimate the available power density in different scenarios [13, 14, 15]. As an example, [13] reported measured power densities in the 0.01–0.3 $\mu W/cm^2$ range for distances of 25 m–100 m from a GSM900 base station. Additionally, the authors of [13] report measurements of approximately one order of magnitude less than the GSM900 measurements, for an indoor measurement setup involving a Wi-Fi network. Such measurement campaigns are necessary as measurements depend strongly on the experiment setup and network traffic. In [14, 15, 189], the availability for harvesting digital TV signals was evaluated in Tokyo, Atlanta, and Seattle respectively. In [190], the amount of available energy from EM signals in the digital TV, the Global System for Mobile Communicatins (GSM) GSM, Wi-Fi, and 3G frequency bands is measured in the London area. In [191], a Worldwide Georeferenced Map containing the available EM signals levels was developed, where the recorded information may come from mobile devices or from laboratory equipment.

The available power that is collected by the radiating element of the rectenna is proportional to its effective aperture. The antenna effective aperture depends on the operating wavelength and gain of the antenna [120]. As an example, a square patch antenna with 3.4 cm side length and operating at 2.45 GHz has a simulated effective aperture of approximately 80 cm^2 [12]. There are several challenges in the design of the radiating element of a rectenna. One may consider various trade-offs between compact, dual polarized [12, 134] or circularly polarized rectennas [192] capable of receiving signals with arbitrary polarization and single-frequency band versus multiband [193, 194] and ultrawideband [132] designs aiming to simultaneously harvest electromagnetic power from as many as possible of the existing operating wireless systems.

The amount of dc power that can be harvested from the existing available power is proportional to the rectenna RF-to-dc conversion efficiency η_{RFdc}. The rectenna efficiency varies with the different rectifying circuit topologies and devices used, and it is dependent on the available power and the load resistance at the rectifier output. Low-power rectifier circuits typically use Schottky diodes to convert microwave power to dc power. Low and zero barrier diodes are required in order to rectify low-power input signals, similar to the ones used in detector applications. Nonetheless, rectifiers based on pseudomorphic high-electron-mobility transistor (p-HEMT) devices have also been proposed showing comparable efficiency values [185, 195]. Typically, envelope detectors and voltage multiplier or charge pump circuits based on diode or transistor devices are implemented, as shown in Figure 6.26. Reported rectenna efficiencies for available input power levels in the order of 10 μW (−20 dBm) are between 10% and 25%, and increase to 30% to 60% for available power levels of 100 μW (−10 dBm) [12, 132, 134, 193].

There have been recent studies in the literature aiming to estimate the available RF power density in ambient environments [13, 14, 190, 191, 196, 197].

Table 7.1 presents a nonexhaustive summary of the obtained results based mainly on the summary reported in [197] but also in [14, 191, 198].

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Table 7.1 Selected reported ambient RF power densities [14, 191, 197, 198].

Reference	Year	Location	Power density nW/cm^2	DC power μW	Freq. band
Visser et al. [13]	2008	indoors	0.03	1,900	WLAN
Sample and Smith [189]	2009	Seattle, USA, outdoors		60	DTV
Olgun et al. [198]	2012	indoors	370	18	WLAN
Vyas et al. [15]	2013	Tokyo, JP, outdoors	> 26	0.93-29	DTV
Mimis et al. [199]	2015	Bristol, UK, outdoors	1,400	n/a	GSM900
Piñuela et al. [190]	2013	London, UK, outdoors	84	7400	GSM1800
Guenda et al. [191]	2014				

Consequently, electromagnetic energy harvesters have been proposed in the literature in order to enable wireless powering of sensors and other devices [134, 192, 196, 200]. Needless to say, the imagination, or rather, the ingenuity of the designer plays an important role in visualizing application scenarios where one can take advantage of the availability of ambient RF power and harvest it toward powering of sensors. For example, Figures 7.1 and 7.2 show two laboratory experiments, performed in 2009, where we investigated whether we could capture some of the RF energy leaking from a microwave oven or when a mobile phone is receiving a call. We used a rectenna comprising an ultrawideband printed monopole antenna connected with RF connectors to a series diode rectifier. In both cases, we were able to measure an output dc voltage of about 200 mV over a 2 KΩ resistor corresponding to approximately 20 μW or harvested power at a distance of about 1 m from the microwave oven and the phone. One may appreciate the difficulty in drawing reliable conclusions from such experiments due to the large number of parameters that affect the experiment, such as, for example, the propagation scenario, the state of the microwave oven (i.e., whether there is something inside the oven), the RF transceiver inside the phone, the antenna and the rectifier used in the rectenna, the propagation environment, etc.

Table 7.2 lists some examples of electronic devices and the amount of power that is required to power them up [197].

7.3 Low-Power Rectifier Circuits

As we have seen in Section 6.6, there exists a significant amount of literature regarding the theoretical performance analysis of rectifier circuits. It is possible to classify rectifier detector circuits into small signal and large signal detectors depending on the operating conditions of the nonlinear devices [202, 203].

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Figure 7.1 Harvesting the leaked signal from a commercial kitchen microwave.

Figure 7.2 Harvesting the signal from a mobile phone.

In the latter case, the nonlinear device behaves as a switch, and we have seen in Section 6.6 that we need to model separately the different switching states. In [137, 141], a diode model including a series resistance and a parallel combination of a nonlinear resistance and capacitance was used to model a single shunt diode rectifier connected to a load. The voltage across the diode nonlinear resistance was modeled as a constant voltage drop when the diode is on and a harmonic signal containing a dc term and a fundamental frequency term when the diode is off. A harmonic expansion using dc and fundamental frequency terms was used for the nonlinear capacitor, the linear diode resistance, and the total voltage across the shunt diode and rectifier load. The analysis for a harmonically terminated diode and transistor rectifiers was presented in [181], whereas in [180]

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Table 7.2 Selected electronic devices and their operating power [197].

Device	dc power (μW)
Small calculator	2
Monza 6R RFID tag [201]	6.2
Wristwatch	20
Digital thermometer	20
Smoke detector	55
Computer mouse	20,000
LED	60,000
Smartphone	500,000

fundamental limits of different diode-based rectifier circuit RF-dc conversion efficiency were derived.

In the former case, it is possible to apply a series approximation in the current-to-voltage characteristic of the nonlinear device in order to obtain meaningful and intuitive results about the rectifier circuit behavior [202]. A harmonic expansion using modified Bessel functions is often used for the diode current [204, 205, 206], while the dc power is evaluated by averaging over the input signal period [204, 205, 206, 207].

Let us focus on the simplest rectifier circuit, the series diode rectifier, shown in Figure 7.3. In the case of a small voltage signal applied across the diode terminals as shown in Figure 7.4a, the rectifier operation depends on the slope and the curvature of the current-to-voltage characteristic of the diode at the dc bias point [203]. The dc voltage output of the circuit is proportional to the power of the input signal, and the circuit is known as a "square law" detector. One characteristic measure of diode detectors is the current responsivity β

$$\beta = \frac{1}{2}\frac{d^2 i/dv^2}{di/dv} \tag{7.2}$$

given by the half of the ratio between the second and the first derivatives of the current-to-voltage characteristic at the dc operating point. The current responsivity is equal to the dc current that is generated by the detector over the average RF power that is absorbed by the detector when the nonlinear current-to-voltage characteristic of the detector is approximated by a power series where only terms up to second order are considered [208]. The dc output power of the detector and the detector RF-to-dc conversion efficiency are thus proportional to β^2. As we will see in the next paragraphs, another important characteristic is the input resistance of the detector, which is critical in order to be able to implement a good impedance matching circuit between the rectifier and the antenna. Finally, the asymmetry of the current-to-voltage characteristic is important in order to be able to operate the rectifier at zero dc bias. In other words, a high responsivity at zero dc bias voltage and an input resistance around 50 ohms are the characteristics of an ideal rectifier circuit.

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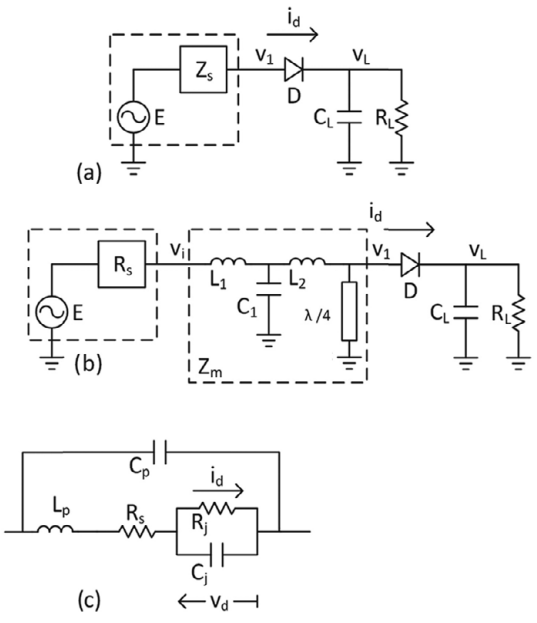

Figure 7.3 Block diagram of the rectifier setup in harmonic balance: (a) general model of the source, rectifier, and output filter; (b) model including source, matching network with harmonic termination, rectifier, and output filter; and (c) Schottky diode model. ©2016 IEEE. Reprinted with permission from [209]

In the case of a large voltage signal applied across the diode terminals as shown in Figure 7.4b, the diode conducts current only at a fraction of the input signal period and the current follows the peaks of the applied signal, resulting in a linear relationship instead between the output voltage and the input voltage to the rectifier [203].

Let us look at the series diode rectifier of Figure 7.3 in more detail. In a preliminary setup, a source with a desired harmonic impedance profile Z_s is connected in series with a Schottky diode D, which is followed by a shunt capacitor C_L and resistive load R_L, shown in Figure 7.3a. The rectifier efficiency η_A is defined as the ratio of the dc power P_L delivered to the output load R_L over the average available RF power from the source P_A.

$$\eta_A = \frac{P_L}{P_A}. \tag{7.3}$$

As we have seen in (6.23), alternatively an efficiency expression η using the input RF power can be used.

A harmonic balance simulation with seven harmonics has been set up in a commercial simulator. A nonlinear Schottky diode model has been considered corresponding to the Skyworks SMS7630-040 diode, which was selected for the analysis. The main parameters of the model are a nonlinear resistance R_j, a nonlinear capacitance C_j, and a series resistance R_s, shown in Figure 7.3c. The diode

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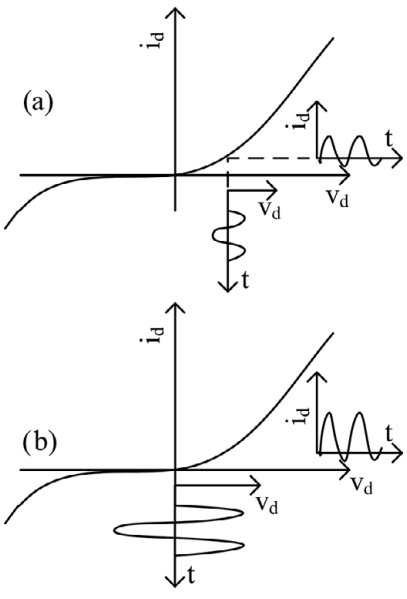

Figure 7.4 Diode rectifier/detector operation: (a) small signal and (b) large signal [202].

saturation current is I_s. Additionally, the diode has a breakdown voltage V_B. The diode package parasitics consist of an inductor L_p and a capacitor C_p.

Let us consider an ideal diode with $R_s = C_j = 0$, $V_B = 100V$, and $L_p = C_p = 0$. Furthermore, the load capacitance is sufficiently large ($C_L = 10$ nF) so that V_L consists only of dc voltage. In a first simulation, the source impedance is set to a real value $Z_s = R_s = 10$ KΩ that is constant at all frequencies, i.e., dc, the fundamental and the harmonics of the fundamental. The value of Z_s was selected arbitrarily and does not have effect in the qualitative behavior of the obtained results. The load resistance $R_L = rR_s$ is optimized to maximize the RF-dc conversion efficiency for an input signal with available power −20 dBm. In Figure 7.5, the efficiency n_A is plot versus the available input power P_A. It is seen that given enough input RF power, a maximum efficiency limit of 48.5% is obtained. If one sets the dc source impedance to 0Ω and performs the same experiment, one obtains a maximum efficiency of 80.9% for a sufficiently large input power. This is consistent with the theoretical limit obtained in [180]. Furthermore, proper harmonic termination can lead to a maximum theoretical efficiency of 100% as noted by [180] and demonstrated by [181]. Setting the source impedance to zero or to infinity at harmonic frequencies results in a maximum simulated efficiency of 99.5%, as shown in Figure 7.5. It should be emphasized that the preceding maximum efficiency values require an input signal with sufficiently large available average input RF power, and they are reduced by the diode series resistance, nonlinear capacitance and breakdown voltage, and the diode package parasitics, as well as losses in the source impedance network.

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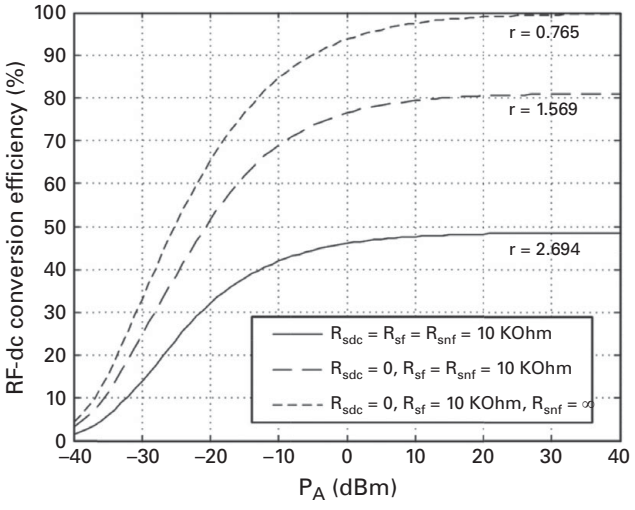

Figure 7.5 Simulated RF-dc conversion efficiency versus available input power of a continuous wave (CW) input signal.

The RF-dc conversion efficiency depends on the load resistance R_L. Figure 7.6 shows the obtained efficiency values versus R_L for an input available power of -20 dBm of a continuous wave (CW) signal for the three cases of different source impedance terminations considered in Figure 7.5. The peak efficiency values of each of the curves of Figure 7.6, correspond to the efficiency value listed in Figure 7.6 for $P_A = -20$ dBm. It can be seen that the optimal load leading to the peak efficiency is strongly affected by the source impedance at dc and the harmonics of the fundamental frequency.

Let us focus on the effect of the input signal on the optimal load and RF-dc conversion efficiency. In order to derive an approximate expression for the rectifier efficiency under small signal excitation, it is assumed

$$v_1(t) = V_{10} + \sum_{n=1}^{N} V_{1n}\cos(n\omega_o t) \approx V_{11}\cos(\omega_o t) \tag{7.4}$$

$$v_L(t) = V_{L0} + \sum_{n=1}^{N} V_{Ln}\cos(n\omega_o t) \approx V_{L0} \tag{7.5}$$

and

$$i_d(t) = I_{d0} + \sum_{n=1}^{N} I_{dn}\cos(n\omega_o t) \approx I_{d0} + I_{d1}\cos(\omega_o t). \tag{7.6}$$

The first equation (7.4) relies on the fact that the stub of the matching network (Figure 7.3b) leads to zero dc and even harmonic voltage components at the input of the diode, and it is assumed that odd harmonic voltage components are very small compared to the fundamental voltage. Similarly, it is assumed that

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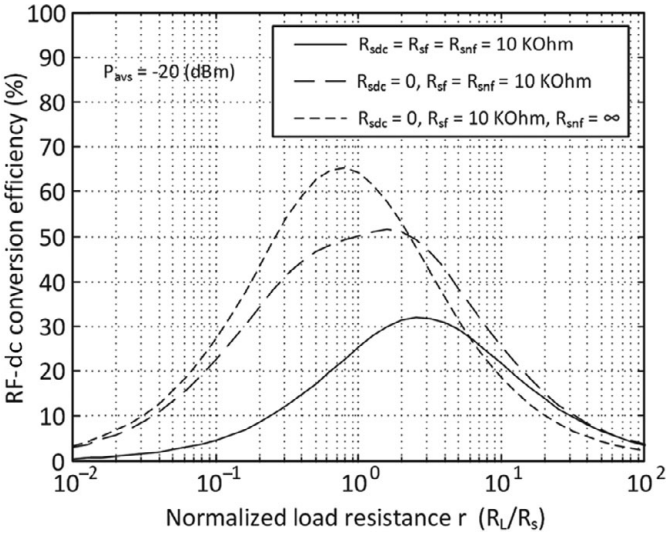

Figure 7.6 Simulated RF-dc conversion efficiency versus available input power of a CW input signal.

the output capacitor C_L minimizes the fundamental and harmonic components of the output voltage v_L. The phasors of the harmonic expressions are considered constant with time as a CW excitation has been considered.

Assuming $R_s = C_j = 0, V_B = 100V$, and $L_p = C_p = 0$, the diode current is

$$i_d(t) = I_s \left[e^{\alpha(v_1 - v_L)} - 1 \right], \tag{7.7}$$

where $\alpha = 1/nV_T$, $V_T = kT/q$ is the thermal voltage, n the diode ideality factor, k the Boltzman constant, T the junction temperature, and q the electron charge. It is easily verified that α is proportional to the current responsivity of the diode $\alpha = 2\beta$. Using (7.4) and (7.5) and the modified Bessel function of the first kind B_n series expansion [205]

$$e^{z\cos(x)} = B_o(z) + 2\sum_{n=1}^{+\infty} B_n(z)\cos(nx), \tag{7.8}$$

one obtains for the rectifier diode dc current

$$I_{d0} = I_s \left[e^{-\alpha V_{L0}} B_o(\alpha V_{11}) - 1 \right] \tag{7.9}$$

and for the rectifier diode RF current at the fundamental frequency ω_o

$$I_{d1} = 2I_s e^{-\alpha V_{L0}} B_1(\alpha V_{11}). \tag{7.10}$$

The input RF impedance of the rectifier is then equal to

$$R_1 = \frac{V_{11}}{2I_s e^{-\alpha V_{L0}} B_1(\alpha V_{11})} \Rightarrow x_1 = \frac{z}{2e^{-y} B_1}, \tag{7.11}$$

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where we normalized the various parameters as $y = \alpha V_{L0}$, $x_1 = \alpha I_s R_1$, and $B_1 = B_1(z)$ with $z = \alpha V_{11}$. Using $V_{L0} = I_{d0} R_L$, one obtains the dc output voltage from (7.9)

$$V_{L0} = I_s R_L \left[e^{-\alpha v_L} B_o(\alpha V_{11}) - 1 \right] \Rightarrow y = x \left[e^{-y} B - 1 \right], \tag{7.12}$$

where again we normalized $x = \alpha I_s R_L$ and $B = B_o(z)$. It is possible to solve (7.12) for the output dc load voltage y using the Lambert W function [206]

$$y = W_o(x e^x B) - x. \tag{7.13}$$

Due to the even symmetry of the modified Bessel function of the first kind of order 0, $B = B_o(\alpha V_{11}) = B_o(\alpha |V_{11}|) > 0$, the argument of the Lambert function in (7.13), is always positive and the principal branch W_o of the Lambert function is used. The output dc power is $P_{L,dc} = V_{L0}^2 / R_L$, and using (7.13) it is calculated as

$$P_{L,dc} = \frac{I_s}{\alpha} y (B e^{-y} - 1). \tag{7.14}$$

The value of $y = y_m$, which leads to a maximum dc output power, is calculated by taking the derivative of (7.14) with respect to y and setting it equal to zero. It is straightforward to find that y_m fulfills

$$B e^{-y_m} (1 - y_m) = 1 \Rightarrow e^{1-y_m} (1 - y_m) = e B^{-1}. \tag{7.15}$$

Using the definition of Lambert function $q = p e^p \Rightarrow p = W(q)$, one has

$$y_m = 1 - W_o(e B^{-1}), \tag{7.16}$$

where again the principal branch of the Lambert function is used due to the fact that $B > 0$. The optimum value of the load $x = x_m$ is obtained from (7.15) and solving (7.12) for x as $x_m = 1 - y_m$, or

$$x_m = W_o(e B^{-1}). \tag{7.17}$$

The input impedance x_{1m} corresponding to the optimum load x_m becomes

$$x_{1m} = \frac{z_1 B W_o(e B^{-1})}{2 B_1}. \tag{7.18}$$

If $V_{11} \to 0$, then $B \to 1$ and $x_m \to W_o(e) = 1$. Furthermore, $B_1 \approx z/2$, resulting in $x_{1m} \to 1$ as well. In the event that $V_{11} \to +\infty$, then $e B^{-1} \to 0$ and $x_m \to 0$. This demonstrates that at the low input power limit, the optimum load of the rectifier circuit depends on the diode saturation current $x_m \to 1 \Rightarrow R_{Lm} \to (\alpha I_s)^{-1}$ and is reduced with increasing average input signal power. Due to the monotonic nature of W_o, one has $0 \le x_m \le 1$. In (7.17), we have derived a closed-form expression for the load value corresponding to maximum efficiency as

$$R_{Lm} = \frac{W_o(e B_o^{-1}(\alpha V_{11}))}{\alpha I_s}. \tag{7.19}$$

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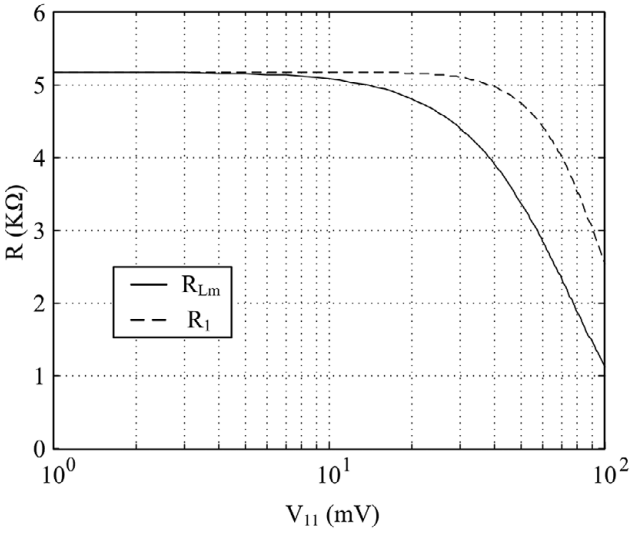

Figure 7.7 Calculated rectifier optimum load R_{Lm} and RF input resistance R_1 corresponding to the optimum load ($I_s = 5\ \mu$A).

The maximum dc output power becomes

$$P_{Lm} = \frac{I_s}{\alpha}\frac{y_m^2}{1-y_m} = \frac{I_s}{\alpha}\frac{(1-x_m)^2}{x_m} = \frac{I_s}{\alpha}\frac{\left[1 - W_o(eB_o^{-1}(\alpha V_{11}))\right]^2}{W_o(eB_o^{-1}(\alpha V_{11}))}. \tag{7.20}$$

The dc output voltage is

$$V_{Lm} = \frac{1 - W_o(eB_o^{-1}(\alpha V_{11}))}{\alpha}. \tag{7.21}$$

Finally, the input RF impedance of the rectifier at the optimum load becomes

$$R_1 = \frac{V_{11}B_o(\alpha V_{11})W_o(eB_o^{-1}(\alpha V_{11}))}{2I_s B_1(\alpha V_{11})}. \tag{7.22}$$

The calculated optimum load R_{Lm} and optimum input resistance R_1 versus the RF amplitude V_{11} of a CW signal using (7.19) and (7.22) is shown in Figure 7.7, for $I_s = 5\mu$A, which corresponds to the SMS7630 diode ($V_T = 25.85$ mV at 300 K). In this case, both the optimum load and the input impedance of the rectifier corresponding to the optimum load to the limit of small input power become $R_{Lm} = R_{1m} = 5.43\ k\Omega$. This high input resistance value poses a significant challenge to the designer trying to implement an impedance matching circuit over a wide bandwidth at low input power levels.

7.4 Nonlinear Optimization of Rectenna Circuits

Depending on the targeted application and attending to the maximum harvesting range and available frequency sources, different operation frequencies may be chosen for the rectenna element. The antenna and the rectifier elements have to

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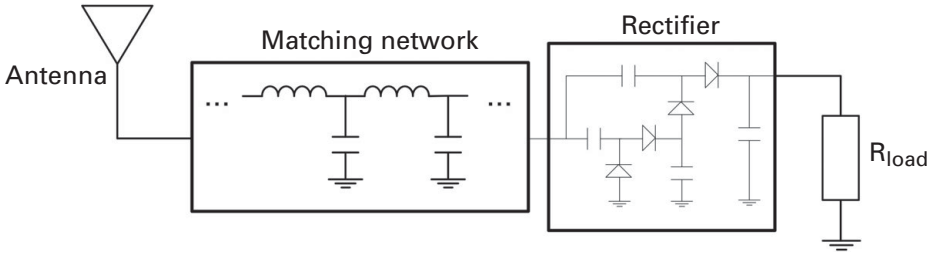

Figure 7.8 Schematic representation of the building blocks of a rectenna element.

be designed in order to maximize the amount of dc power that can be obtained at the selected operation frequency. The antenna has to be designed to operate and have good performance at the selected frequency, and the rectifier circuit has to be optimized to have its maximum RF-to-dc conversion efficiency at this frequency.

In the simplest scenario, one needs to design a single-frequency band rectenna. However, in some cases, it may be of interest to have dual-band, triple-band, and in general multiple-band or broadband rectenna designs in order to harvest energy from different frequency sources. The optimized design of a rectenna requires the simultaneous synthesis of several elements: (1) antenna, (2) rectifier circuit, and (3) matching network (Figure 7.8). In the case of the antenna element, it has to be designed to operate at the selected frequency bands leading to single-band, multiple-band, or broadband antenna designs. As previously mentioned, in order to maximize the RF-to-dc conversion efficiency of the rectenna, an adequately designed matching network has to be selected and optimized aiming to maximize the power transfer from the antenna port to the rectifier circuit. The optimum design of the matching network requires consideration of both the antenna and the rectifier circuit in the design stage. For a specific load R_L and for a selected topology of the rectifier circuit and of the antenna element, the matching network can be optimized to maximize the RF-to-dc conversion efficiency of the rectenna.

In order to be able to consider the antenna and the rectifier simultaneously in the design stage, the antenna must be introduced in the nonlinear circuit simulation. This is done by considering the antenna as a loaded scatterer and introducing the Thevenin or Norton equivalent circuit of the antenna in the receiving mode using the theory developed in [210]. This approach applied in rectenna circuits was implemented in [12, 193]. In Figure 7.9, for example, the Thevenin equivalent circuit is used, comprising an open-circuit voltage source V_{oc} in series with an impedance Z_A. The antenna impedance Z_A in the receiving mode is equal to the antenna impedance in the transmitting mode and can be computed using an electromagnetic simulator, for example, or by measuring the s-parameters using a network analyzer. The open-circuit voltage V_{oc} can be computed by considering reciprocity theory [211]. If one considers a plane wave with vector amplitude $\mathbf{E_o}$ arriving at the antenna terminals from a direction (θ, ϕ),

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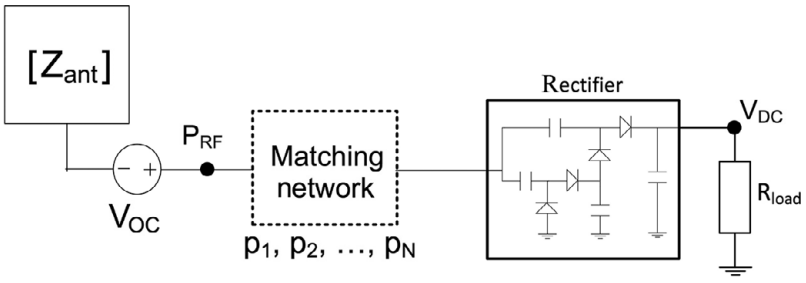

Figure 7.9 Rectenna simulation setup using the Thevenin equivalent representation for the receiving antenna.

then reciprocity theory dictates that the open-circuit voltage at the antenna terminals is given by

$$V_{oc}(\theta,\phi) = \frac{\lambda}{j60\pi}\mathbf{F}(\theta,\phi)\mathbf{E_o}, \tag{7.23}$$

where λ is the free space wavelength. $\mathbf{F}(\theta,\phi)$ is the electric far-field vectors of the antenna at the direction (θ,ϕ) when a unit current excitation is applied at its port [120, 210]. The antenna far-field can be also computed by an electromagnetic circuit simulator with the antenna operating in the transmitting mode. The impressed field has a magnitude $E_o = \sqrt{2\eta S}$, where S is the power density at the antenna terminals. This way, the Thevenin equivalent of the antenna can be introduced in a commercial circuit simulator in order to take into account the antenna structure when optimizing the rectifier. This setup allows one to separately address the antenna, which requires an electromagnetic analysis, and the rectifier, which requires a nonlinear circuit analysis, and subsequently link the two together.

Due to the nonlinear nature of the used rectifying devices, nonlinear simulation tools such time domain integration or harmonic balance must be employed for the analysis and optimization of the rectifier circuit. Harmonic balance provides an efficient simulation tool that can be combined with optimization goals in order to optimize a desired parameter, such as the maximizing the output dc voltage, or the RF to dc conversion efficiency of the rectifier.

In this last case, (7.3) can be used to define the RF-to-dc conversion efficiency η_a. It is noted that using the available power in the efficiency expression provides an equation that is easier to compute because the available power does not depend on the rectifier circuit or the matching network. In order to maximize η_a, a minimum value of RF-to-dc conversion efficiency at the desired frequency is imposed using optimization goals and the values of the matching network components $p_1, p_2, \ldots p_N$ as well as the rectifier load R_L is calculated in order to fullfil this goal.

The harmonic balance analysis of different rectifier circuits is shown in Figure 7.10. In order to compare different circuit topologies, a lossless matching

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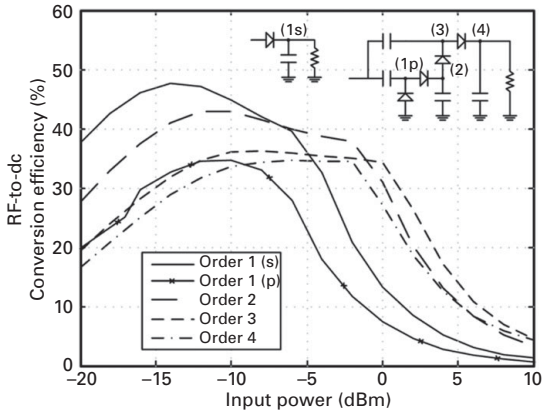

Figure 7.10 Rectifier efficiency versus the input available power for different rectifier circuits.

network was considered and the rectifier efficiency η_A was maximized for an available input power of −20 dBm. Five different topologies were considered, a single series diode rectifier, a shunt diode rectifier, and three voltage multiplier topologies with two, three, and four diodes respectively. The SMS7630 diode model was considered in the simulation. After the optimization at −20 dBm, the matching network parameters and the output load were fixed, the input power was sweeped from −20 dBm to 10 dBm. The obtained efficiency is plotted in Figure 7.10.

Based on the results, we can draw several conclusions regarding the performance of rectifier circuits. We can identify three regions based on the input power levels. First, at low input powers, the efficiency increases relatively linearly with the input power. Comparing the different circuit topologies, we can see that the single series diode rectifier has the higher efficiency, and as the number of diodes increases, the efficiency is reduced. This is intuitive because there is some power lost in each diode and therefore the more diodes one uses the more power is lost and the lower the efficiency becomes. However, as one increases the number of diodes, the output voltage of the rectifier increases. The designer is therefore presented with a trade-off between desired output load voltage and efficiency.

As the input power increases, the efficiency begins to reach a plateau. This is due partially to reflection losses associated with impedance mismatch between the rectifier and the matching network. Due to the nonlinear nature of the rectifier, the input impedance changes as the input power varies from its original value at −20 dBm where the matching network was designed.

Finally, as the input power increases further, there is a point where efficiency begins to drop suddenly. This is because the voltage across the diode begins to reach the diode breakdown voltage value, which results in a sudden increase in the current through the diode and significant power losses in the diode. Furthermore, the rectrifier circuits with fewer diodes reach this efficiency drop point faster than

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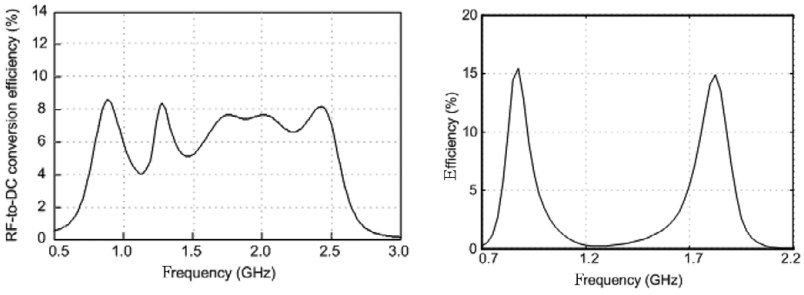

Figure 7.11 Multiband versus wideband rectifier efficiency.

the ones with a larger number of diodes. This is also intuitive because a larger voltage across the rectifier terminals is necessary to bring all the diodes to the breakdown voltage zone.

We have already seen in Figure 7.6 that there is an optimum load value that maximizes efficiency for a given input power level. Furthermore, the optimum load varies with the input power. We can see that due to the nonlinear nature of the rectifier circuits, the designer is faced with several challenges defined by the operating frequency, the operating power, and the output load. How to address these challenges is the focus of the next sections.

7.5 Multiband Rectifiers and Rectennas

We have seen that the available power density due to ambient RF sources is quite low. In order to be able to harvest a sufficient amount of power, one has to consider a large aggregate bandwidth covering either a number of different disjoint frequency bands or a large, wide bandwidth. The first scenario is suitable when the sources of RF power are known a priori, i.e., mobile phone bands, Wi-Fi bands, or TV bands. Consequently, one aims to design a multiband rectifier. The second scenario becomes attractive when the frequency of RF sources is not known a priori and one needs to design a rectifier with high efficiency over a wide bandwidth covering multiple frequency bands. The two cases are presented conceptually in Figure 7.11. The design process becomes essentially that of an impedance matching problem over a desired aggregate frequency bandwidth, with the additional constraints over the input power and output load impedance. Due to a fundamental theoretical limitation in the achievable impedance matching over a frequency band studied by Bode and Fano [212], which we will discuss in more detail in the next section, it is generally possible to achieve a higher maximum efficiency over a number of narrow frequency bands with a smaller aggregate bandwidth than over a wider continuous frequency band.

It is possible to compare different rectennas by expressing the obtained efficiency over either the input power density (in e.g. μW/cm^2) or the input power

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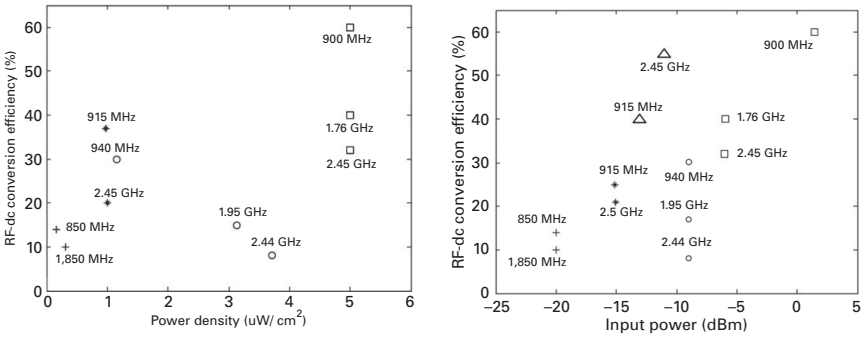

Figure 7.12 Selected published dual-band rectenna efficiencies plot versus (a) input power density (©2013 IEEE, reprinted with permission from [213]) and (b) available input power (∘ [214], + [131], ∗ [213], □ [193], △ [215]).

(in e.g. dBm) at the rectifier antenna terminals. An example of such plots related to multiband rectennas is shown in Figure 7.12.

In the first case, when the input power density is considered one takes into account the antenna gain in the rectenna comparison and effectively considers both the antenna and the rectifier circuit combination, whereas in the second case the comparison is made only between rectifier circuits, therefore excluding the effect of the antenna circuit. Due to the fact that the antenna gain depends on the size of the antenna, one may want to additionally consider the size of the rectenna, when comparing different designs. In an attempt to define a figure of merit taking into account all these parameters, the authors introduced at the wireless power transmission student design competition of the 2011 IEEE Microwave Theory and Techniques Society (MTT-S), International Microwave Symposium (IMS), the following expression

$$\mathrm{FoM} = 10\log_{10}\left(\frac{P_L}{10}\right) - 10\log_{10}\left(\frac{D^2}{25}\right) \tag{7.24}$$

in dB of the rectenna dc output power P_L (μW) normalized over 10 μW, divided by the area calculated as the square of the largest dimension D (cm) of the rectenna normalized over 25 cm^2. The expression includes the size of the rectenna in an attempt to define an objective FoM figure. Although not widely accepted, it is indicative of the multiple challenges in designing a rectenna circuit.

7.6 Ultrawideband Rectifiers

The input impedance Z_e of a rectifier circuit contains a resistive component and a reactive, typically capacitive, component. Furthermore, both components vary with the input power. For a given input power level, it is possible to provide

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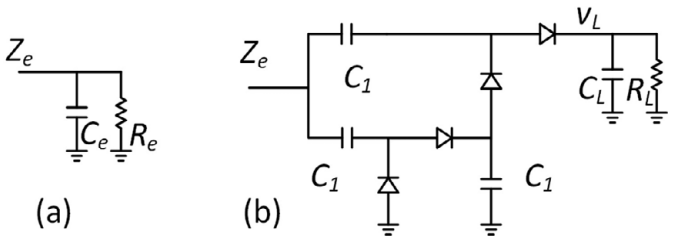

Figure 7.13 Equivalent circuit model of a rectifier: (a) shunt RC equivalent, and (b) charge pump rectifier. ©2017 IEEE. Reprinted with permission from [216]

the input impedance of a rectifier by defining an equivalent circuit model that comprises a shut resistor and a shunt capacitor, as shown in Figure 7.13.

The equivalent resistance and capacitance of rectifier circuits with a different number of diodes is simulated in Figure 7.14 [216]. The circuit schematic was the one shown in Figure 7.13b with a varying number of diodes $N = 1, 2, 4$, and 6, where $N = 1$ corresponded to a series diode rectifier. The equivalent resistance and capacitance were extracted by minimizing the difference between the input impedance of the rectifier circuit and a shunt RC circuit over the frequency band 0.4–1.0 GHz. The Skyworks SMS7630 diode model was used, and capacitors $C_1 = 100$ pF and $C_L = 10$ nF were selected such that they presented an effective RF short within the frequency band 0.4–1.0 GHz. Finally, the load resistance was fixed at 1 KΩ.

The input resistance varies significantly with the input power whereas the input capacitance variation becomes more visible at higher input power levels. As we have verified in the theoretical analysis of the previous sections, the input resistance of the rectifier circuits is larger at low input power levels and for a smaller number of diodes. In fact, it appears that for the given diode model and circuit topology, a rectifier with six diodes already presents an input resistance close to 50 Ω at low input power levels of approximately −20 dBm, and therefore it should be easier to design an impedance matching network for this circuit. Although not visible from Figure 7.14, the input impedance depends strongly also on the load resistance.

Having obtained a simple equivalent circuit for the rectifier input impedance, we can address the problem of designing an impedance matching network over a desired frequency band. Precisely, the theory developed by Bode and extended by Fano [212] addresses this problem and derives that the minimum reflection coefficient magnitude $|\Gamma_m|$, which can be obtained when attempting to match a shunt RC load impedance comprising R_e and C_e, over a bandwidth B, using a lossless matching network, is limited by

$$|\Gamma_m| \geq e^{\frac{1}{2BR_eC_e}}. \tag{7.25}$$

Using the results of Figure 7.14 in (7.25), we can obtain an estimate of the minimum achievable theoretical reflection coefficient magnitude over a desired

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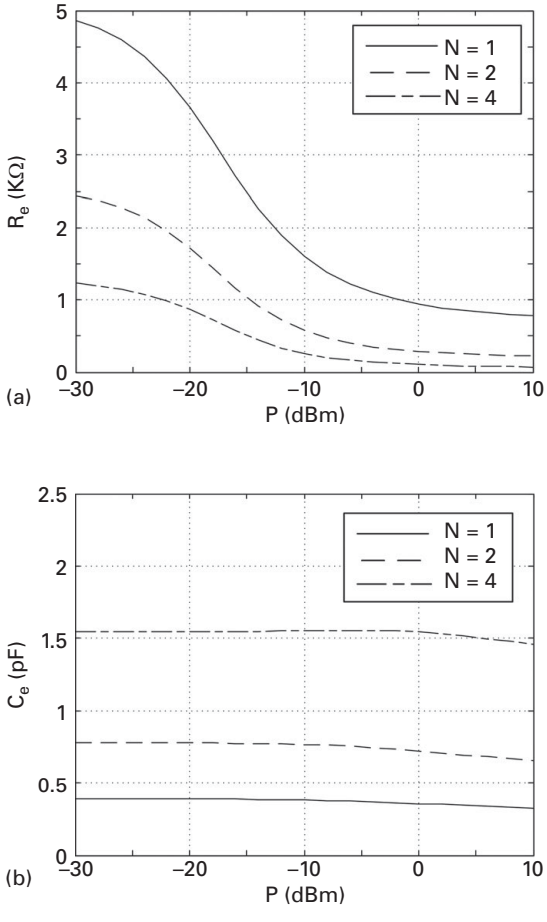

Figure 7.14 Equivalent input impedance of a rectifier circuit: (a) resistance and (b) capacitance [216].

bandwidth of 0.4–1.0 GHz. The result in shown in Figure 7.15, verifying that it is more challenging to design a wideband impedance matching network at low input power levels and for a rectifier with fewer diodes.

The theoretical results help select a rectifier topology for a given input power and output load resistance. The challenge remains, however, how to implement such an impedance matching network. There is a vast amount of literature related to filter design and impedance matching that the designer can apply. For example, a nonuniform transmission line is one topology that traditionally has been used for broadband impedance matching [217]. We demonstrated an octave band and a decade band rectifier based on a printed nonuniform microstrip transmission line using harmonic balance optimization [216]. First, a charge pump rectifier topology using four diodes was selected based on Figures 7.14 and 7.15. The design process consisted of considering a number of microstrip

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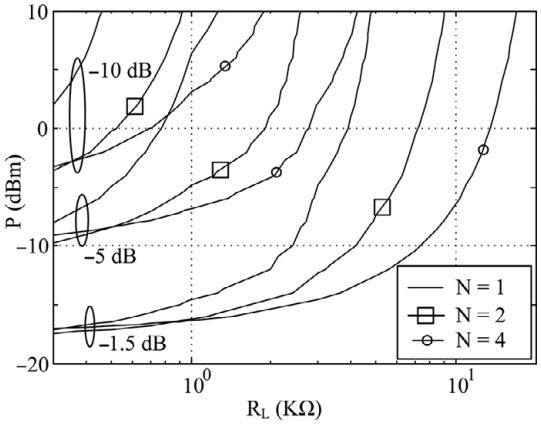

Figure 7.15 Contours of theoretical minimum reflection coefficient magnitude over input power and load resistance for different rectifier circuits [216].

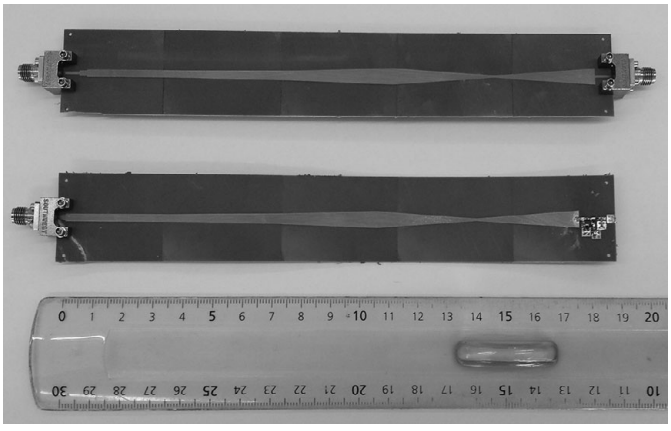

Figure 7.16 Octave band rectifier using a nonuniform transmission line matching network: transmission line prototype (top) and transmission line with rectifier (bottom) [216].

segments of fixed legth and width, hence impedance, and then optimizing the width and the number of sections while placing minimum efficiency goals at different frequency points covering the desired frequency band. The optimization process was done for an input powet of −20 dBm. A series inductor was placed at the input of the rectifier to facilitate the optimization process. The resulting rectifier is shown in Figure 7.16, while its input impedance and RF-dc conversion efficiency are shown in Figures 7.17 and 7.18 respectively.

As expected, the input matching is improved as the input power increases because the rectifier input resistance is reduced to values closer to 50 ohms (Figure 7.18). The input impedance and resulting efficiency are optimized over an octave bandwidth. One disadvantage of a nonuniform transmission line is its large

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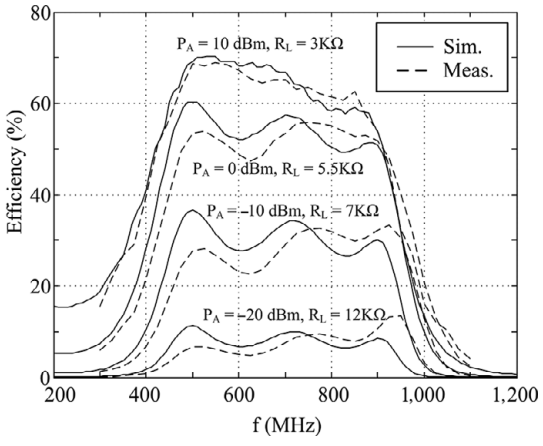

Figure 7.17 Efficiency of ultrawideband rectifier using a nonuniform transmission line matching network [216].

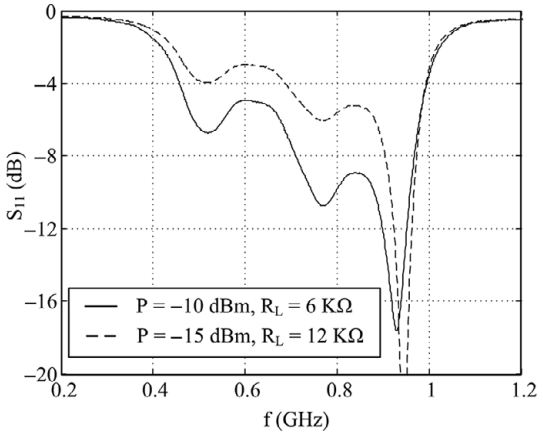

Figure 7.18 Measured input s-parameters of ultrawideband rectifier using a non-uniform transmission line matching network [216].

size; however, meandering can help reduce its overall layout area. Alternatively, one may approximate a nonuniform line using cascaded series inductor L and shunt capacitor C sections [218].

7.7 Load Resistance and Input Power Effects on Rectifier Efficiency

We have seen in Section 7.4 that the rectifier efficiency depends strongly both on the output load resistance and on the input power. However, it is reasonable to consider variable load conditions at rectifier circuits depending on the power requirements of the circuits following the rectifier. Therefore, reduced sensitivity

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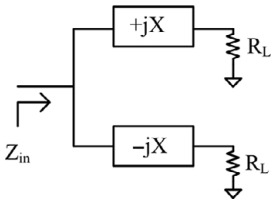

Figure 7.19 Resistance compression network [219].

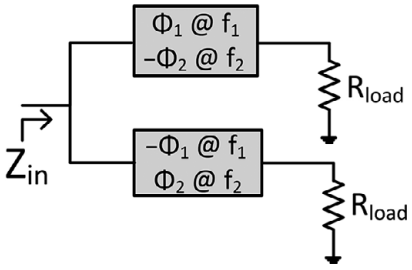

Figure 7.20 Dual-band resistance compression network. ©2014 IEEE. Reprinted with permission from [220]

to load variations is a desirable property for a rectifier circuit. One possible way to achieve this is using a resistance compression circuit [219]. An example of a resistance compression circuit proposed by [219] is shown in Figure 7.19. It comprises of two branches that are connected in parallel and they are each terminated to identical variable resistive loads R. Reactance components with opposite values $\pm X$ are connected in series with the resistive loads. A straightforward analysis shows [219]

$$R_{in} = \frac{X^2}{2R}\left[1 + \left(\frac{R}{X}\right)^2\right]. \tag{7.26}$$

The reactance elements of the branches can be implemented, for example, with one series inductor L at one branch and a series capacitor C at the second branch such that at a desired operating frequency $LC\omega_o^2 = 1$. It is easy to verify that a variation in R is translated to a smaller variation at the input of the resistance compression circuit at the expense of a more complex circuit comprising a larger bill of components and two identical loads. It is possible to cascade more than one such network in order to optimize the resistance compression [219].

It is possible to synthesize multiband resistance compression networks by synthesizing reactive networks with opposite reactance values at the desired frequency points. A dual-band topology is pictured in Figure 7.20.

The implemented resistance compression network and the fabricated prototype are shown in Figures 7.21 and 7.22. The operating bands were 915 MHz and 2.45 GHz. The reactive network comprised two cells each comprising a series LC

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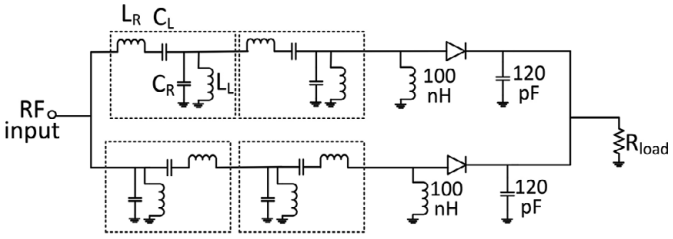

Figure 7.21 Dual-band resistance compression network circuit implementation operating at 915 MHz and 2.45 GHz ($L_R = 8.7$ nH, $L_L = 100$ nH, $C_R = 0.8$ pF, $C_L = 2.7$ pF). ©2014 IEEE. Reprinted with permission from [220]

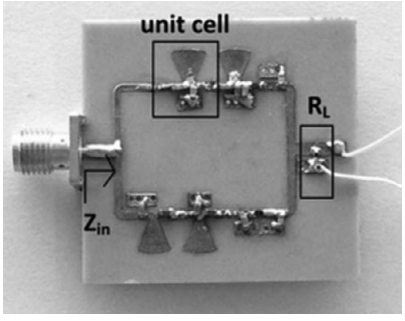

Figure 7.22 Dual-band resistance compression network prototype operating at 915 MHz and 2.45 GHz. ©2014 IEEE. Reprinted with permission from [220]

and a shunt LC circuit providing the desired reactances at the two frequency bands. Two cells were used in order to obtain a better impedance match at the two frequencies. It is interesting to see that one load R_L is used, however, two rectifier circuits are necessary to implement the two branches that are required for the resistance compression network.

Due to the fact that the impedance matching network of the rectifier is designed for a specific load value, load variations result in input impedance variations that lead to impedance mismatch and reflection losses reducing the rectifier efficiency. The dual cell reactive network introduces both the necessary reactance for the resistance compression and transforms the impedance of the rectifier in order to provide impedance matching. The obtained efficiency is compared to a standard dual-band two-diode rectifier without a resistance compression network, shown in Figure 7.23. A plateau in the efficiency is observed at both frequencies for a range of load values demonstrating the effectiveness of the resistance compression.

It turns out that the resistance compression network additionally slightly reduced the sensitivity of the efficiency in variations in the input power levels. The property of the efficiency being insensitive to input power variations is particularly attractive because ambient RF sources have an inherently random

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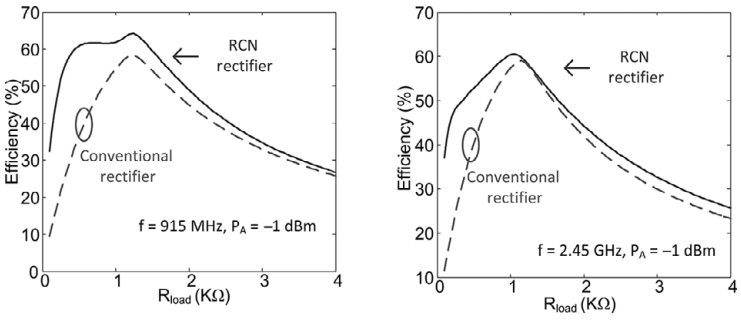

Figure 7.23 Efficiency of a dual-band resistance compression network [220].

and time varying nature due to propagation effects but also modulation present in the RF signals. One way to reduce the sensitivity to input power variation that has been proposed in [221] is to implement a composite rectifier comprising a number of additional diodes and other switching transistor devices that are connected in series with a single shunt diode. The single diode rectifier has a high efficiency at low input power level, but its efficiency drops as the input power increases beyond the point that it drives the diode to its breakdown region. In contrast, a rectifier that contains many diodes in a series has a low efficiency at low input power levels, but it can tolerate a much higher input power before it reaches its breakdown voltage and therefore maintains a high efficiency at higher input power levels than the single diode rectifier. A FET switch is connected in parallel to the additional diodes in such a way that it is at its "On" state, shorting the additional diodes at low input power levels and allowing only the single diode to operate. When the input power increases beyond a critical level, the FET is switched to the "Off" state and the additional diodes are introduced in the rectifier circuit, resulting in a high efficiency for a larger range of input power values.

7.8 Rectification and Angle of Arrival of Incoming Waves

When it comes to harvesting ambient RF energy, the location of the source of the RF energy is typically unknown to the harvester. Consequently, it is necessary to use in the rectenna device an antenna that does not have a directional radiation pattern; rather, an approximately spherical or omnidirectional pattern is desirable. Naturally, in order to maximize the harvested power, it is desirable to form arrays of rectennas, such as [132, 145]. Increasing the number of antennas increases the available effective area for the collection of RF energy, and thus the total RF energy that is being harvested is multiplied by the number of antenna elements. The question arises as to whether it is preferable to sum the harvested energy at the RF level or at the dc level. RF power combining results in forming a directional radiation pattern, therefore sacrificing the omnidirectional

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characteristic of the harvester. dc power combining maintains the omnidirectional characteristic of the antennas as each antenna is considered individually (with some loading effect from the unavoidable mutual coupling with its neighboring elements). The dc output of each rectenna element can be combined in series or parallel, resulting in a desired output voltage and efficiency [145]. The overall efficiency depends, however, on the loading that each rectenna presents to the rest, and it is affected by variations in dc output to the individual elements due to tolerances or, more importantly, due to variations in the RF power illuminating each array element [222, 223].

As we have seen, however, the RF-dc conversion efficiency of the rectifier depends on the input power, and specifically at low input power levels it increases with the input powet. Therefore, one is tempted to perform some RF combining before converting to dc. As a result, one might consider rectenna systems where one rectifier is connected to an antenna subarray and have each subarray radiation pattern point to a different direction, thereby achieving the superposition of RF energy before the RF-to-dc conversion and covering a wide angular area [224]. Another way around the angular coverage problem could be to employ beam-steering architectures, but such systems consume energy in steering the antenna beam, and therefore, one needs to take into account the amount of energy spent in the beam-steering process in order to compute the overall RF-to-dc conversion efficiency of the system.

An alternative rectifier topology based on a Wilkinson power combiner was proposed in [225]. It comprises a two-branch rectifier, which is capable of maintaining an approximately constant RF-to-dc conversion efficiency over any arbitrary phase shift between the RF signals present at its input terminals and, therefore, over any angular direction. Furthermore, it is scalable, employing combiner modules connected to a large number of antenna elements or subarrays and subsequently combining the output in series or parallel configuration. The circuit performs both RF and dc power combining and is shown in Figure 7.24. It comprises two inputs that would be connected to the antenna elements. A Wilkinson combiner combines the two inputs, and the combined signal is rectified by a first series diode rectifier circuit. The Wilkinson combiner circuit includes a resistor connected across its two inputs, which helps isolate the two inputs. When the two inputs are in phase, there is no current flowing through the resistor, and the two inputs are combined at the output port. When, however, there is a phase difference at its inputs, there is some current flowing in the resistor that helps maintain input matching and isolation at the expense of the power dissipated in the resistor. In the topology of Figure 7.24, a second rectifier is used in place of the resistor, which maintains the input matching of the ports but additionally converts (a fraction) of the RF power flowing into dc power and minimizes the dissipated RF power. The two rectifier outputs are summed in parallel in order to obtain a single dc output.

The input matching networks of the rectifiers are optimized in such a way that the efficiency of the rectifier remains relatively constant independently

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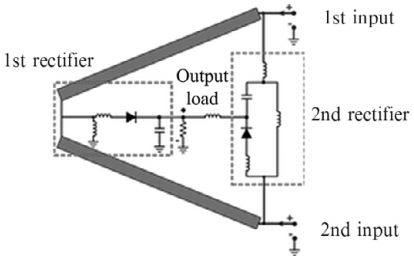

Figure 7.24 Circuit schematic of RF and dc combining rectifier based on a Wilkinson power combiner that is insensitive to phase differences at its inputs. ©2019 IEEE. Reprinted with permission from [225]

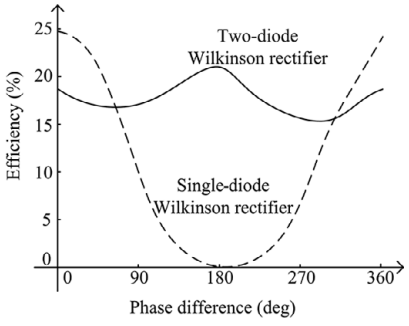

Figure 7.25 RF and dc combining rectifier efficiency versus the phase difference at its input terminals for an input power of −20 dBm at each RF input port [225].

of the phase difference between the two RF input signals. As a result, the circuit achieves both a higher antenna gain due to the RF power combining and maintains a high dc combining efficiency. Because of the fact that the rectifier is a nonlinear circuit, its efficiency increases nonlinearly with the input power. Consequently, because the RF combining results in a higher RF input power to the rectifiers, it is possible to operate at a higher RF-dc conversion efficiency than a topology where each antenna is individually connected to a rectifier without performing any RF power combining. The rectifier efficiency is plotted in Figure 7.25 versus the phase difference, compared to a Wilkinson-based rectifier with a single two-diode rectifier at the power-combining output of the Wilkinson power divider, where the shunt resistor is maintained. The prototypes of the two circuits that were used to obtain the measured results of Figure 7.25 are shown in Figure 7.26. Using a rectifier in place of the shunt resistor allows one to maintain good efficiency for any phase difference between the input RF signals.

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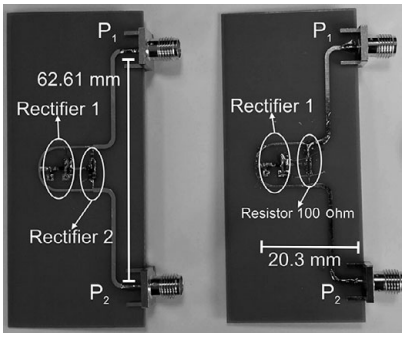

Figure 7.26 RF and dc combining rectifier prototypes. ©2019 IEEE. Reprinted with permission from [225]

7.9 Signal Optimization for RF Energy Harvesting

Wireless power transmission is associated with transferring microwave power using a continuous wave (CW) carrier signal. Ambient RF signals, however, are not necessarily continuous wave signals. In fact, wireless communication signals are modulated signals that typically have a finite frequency bandwidth and a time varying envelope. It is therefore natural to ask the question of whether the properties of modulated signals affect the power transfer efficiency or, alternatively, what are the characteristics of an optimum signal for wireless power transmission.

Measurements of RF signals with a time-varying envelope have appeared in the literature to the best of our knowledge as early as 2005 [132], where measurements with a two-tone composite RF signal were performed, while later in 2010 measurements of RF-dc power conversion using a quadrature phase shift keying (QPSK) signal showed a small efficiency improvement relative to a CW tone signal [226].

We can describe such signals with a time-varying envelope using a complementary cumulative distribution function (CCDF) plot. In the case of randomly varying signals such as digitally modulated signals, the CCDF curve $\overline{F}_p(p)$ represents the probability Pr that a random variable, in this case the instantaneous power P of a signal, has a certain value that is larger than a value p [227],

$$\bar{F}_p(p) = \Pr\{P > p\}. \tag{7.27}$$

The CCDF is related to the cumulative distribution function (CDF), $F_p(p) = \Pr\{P < p\}$ as $\bar{F}_p(p) = 1 - F_p(p)$. The ratio of the instantaneous power over the average power in dB is the abscissa of a CCDF plot [228]. In the case of deterministic periodic signals such as multitone signals (also called multisine signals), the CCDF curve represents the fraction of the envelope period that the instantaneous power takes a desired value that is larger than the average. As an example, CCDF curves of multitone signals with two, three, four, and eight

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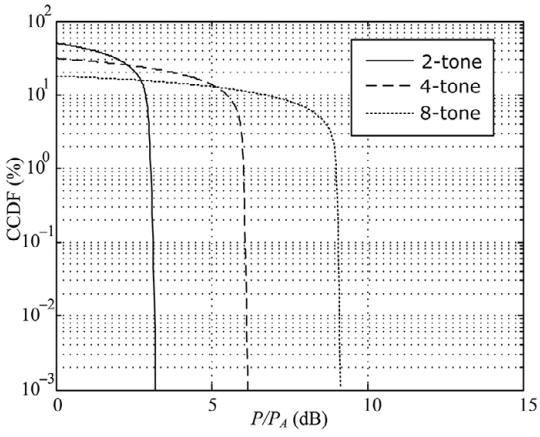

Figure 7.27 Measured CCDF curves of multitone signals with two, four, and eight tone carriers [209].

carriers is shown in Figure 7.27 [209]. A carrier spacing of 0.5 MHz was used around an RF carrier value of 915 MHz. The measurements were performed using a Keysight ESG 4438C Digital vector signal generator with multitone signal generation capability and a Vector Signal Analyzer (VSA) running on a PSA E4448A Spectrum Analyzer as a receiver. The CCDF curves have a shape resembling a waterfall curve. The rightmost point of the curve represents the peak-to-average power ratio (PAPR) value of the signal. Usually, for practical reasons, a specific value of CCDF probability (or time fraction) such as 0.1% is used to determine the PAPR value. One can verify that as the number of tones increases, the PAPR value also increases. It should be emphasized, however, that the PAPR and CCDF curves in general depend on the relative phase value between the carriers. In this case, all tones were synchronized in phase with each other.

Selected measured CCDF curves of digitally modulated signals are shown in Figure 7.28 [209]. In digitally modulated signals, a pulse-shaping filter is used in order to limit the bandwidth of the transmitted waveforms [229]. A commonly used filter is a square root cosine filter, which is characterized by the roll-off factor $0 \leq \beta \leq 1$. The CCDF curves were created using a roll-off factor $\beta = 0$, which limits the bandwidth of the transmitted signals to f_s, where f_s is the symbol rate. The roll-off factor affects the PAPR, as shown in Figure 7.29.

Until this section, we have seen that both the average input power and the output load affect the RF-dc conversion efficiency of a rectifier. In Figure 7.30, we created contours corresponding to an RF-dc conversion efficiency of 20% versus the available average input power P_A and the output load R_L of a series rectifier [209]. The contours appear to be suddenly interrupted and overlap each other at high load and high power values due to the fact that the diode breakdown voltage is reached and efficiency suddenly drops. One important conclusion that can be drawn from these contours is that as the PAPR of the signal increases the efficiency contours are shifted toward higher load values. This is an important

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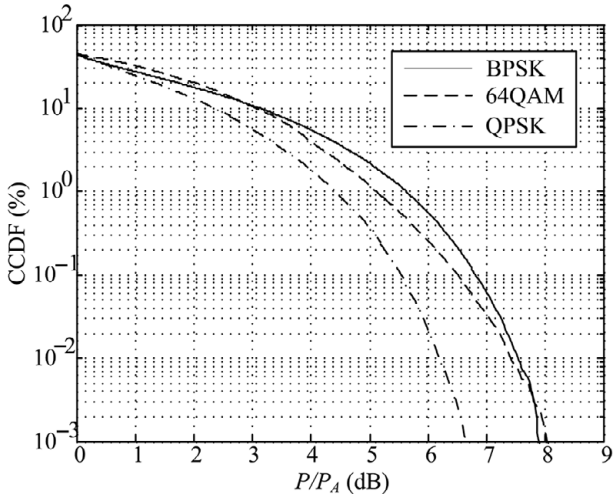

Figure 7.28 Measured CCDF curves of digitally modulated signals with pulse-shaping roll-off factor $\beta = 0$ [209].

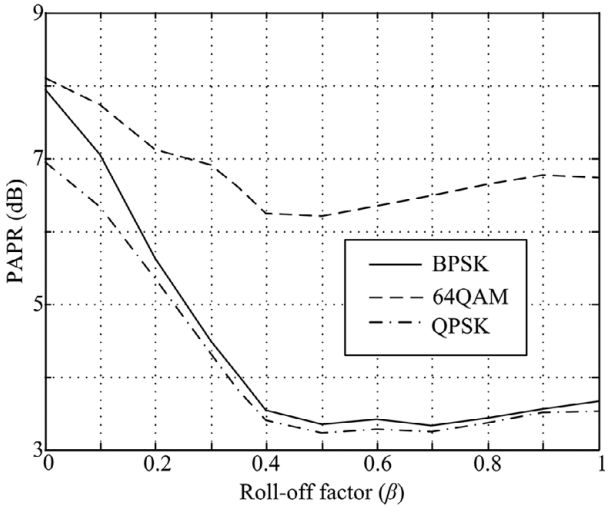

Figure 7.29 Measured PAPR of digitally modulated signals versus the pulse-shaping roll-off factor β [209].

result because it shows that one can control the efficiency by selecting a signal with a certain PAPR. Results demonstrating that a higher RF-dc conversion efficiency can be obtained using multitone signals have been presented in [147] and later in [202]. The multitone signals were described as power-optimized waveforms and a theoretical analysis of the RF-dc conversion efficiency was presented in [230].

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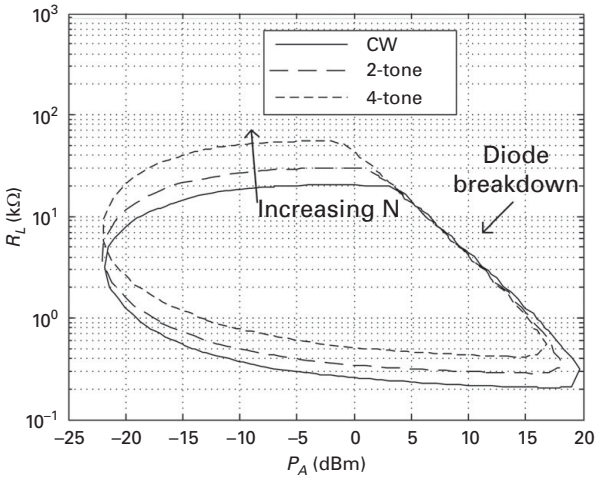

Figure 7.30 Contours of 20% RF-dc conversion effficiency of different multitone signals applied to a series diode rectifier [209].

A similar behavior occurs for randomly modulated signals with a time-varying envelope. Measurements comparing the RF-dc conversion efficiency of a rectifier to which we applied different modulated waveforms of the same bandwidth but with different PAPR were first presented in [149]. The different waveforms where an orthogonal frequency-division multiplexing (OFDM) signal, white noise and a chaotic signal generated from a properly biased Colpitts oscillator [149]. Each of these signals has a different, increasing PAPR value that was determined experimentally, as shown in Figure 7.31. The RF-dc conversion efficiency measured over a 5.6 KΩ load is plot in Figure 7.32. Similarly with the multitone signals, we observed that a higher conversion efficiency is obtained at low input power levels for signals with a higher PAPR. Once the power increases, the signals with a high PAPR first result in the rectifier reaching the breakdown voltage of the diode and their efficiency begins to drop. It should be emphasized, however, that, as Figure 7.30 showed, the efficiency contours shift toward higher load resistance values with increasing PAPR, and therefore the observed efficiency improvement is contingent on the load resistance that has been used. However, high load resistance values are typically associated with low power sensors because of the inherent low power dissipation requirement, and therefore having a high efficiency at high load values appears to be an attractive property.

The PAPR value, although important, does not fully describe the rich nature of the signal envelope variations. For example, we experimentally synthesized two signals with the same PAPR but otherwise having a different CCDF curve behavior. These two signals were a four-tone signal with in-phase tones and a 64QAM signal with a roll-off $\beta = 0.5$. The measured CCDF of the signals is shown in Figure 7.33. Although the two signals have the same PAPR, the four-tone signal has a wider CCDF curve, implying a stronger instantaneous power

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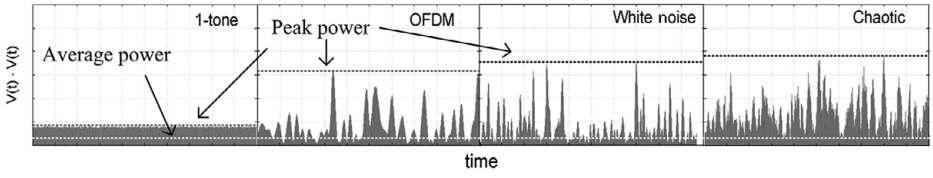

Figure 7.31 Instantaneous power of different randomly modulated signals with a time-varying envelope and different PAPR values. ©2014 IEEE. Reprinted with permission from [149]

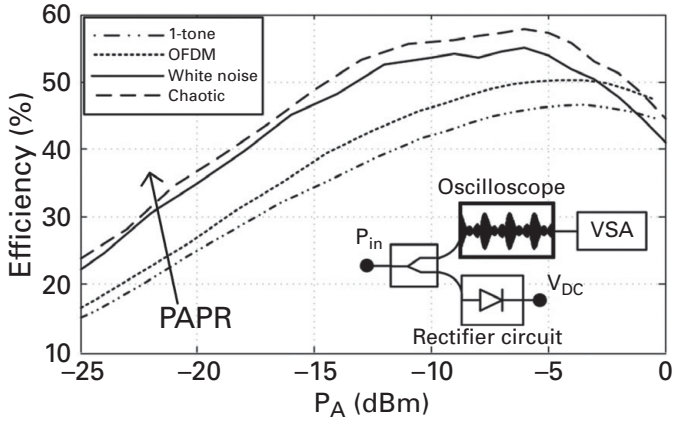

Figure 7.32 RF-dc conversion effficiency of different randomly modulated signals with a time-varying envelope and different PAPR values. ©2014 IEEE. Reprinted with permission from [149]

variation where the instantaneous power of the four-tone signal takes values closer to its peak value more times than the 64 QAM signal. We then applied the signals to a rectifier and measured the RF-dc rectifier efficiency, shown in Figure 7.34.

One can see that even though the two signals have the same PAPR, the obtained efficiency curves are very different. Specifically, the efficiency of the four-tone signal is shifted toward higher load values. It is possible to distinguish between these two signals by using a different parameter, the instantaneous power variance [231]. The instantaneous power variance is defined as

$$\sigma_P^2 = \mathrm{E}\left[(P - P_A)^2\right] = \int_0^{+\infty} (P - P_A)^2 dF_p = -\int_0^{+\infty} (P - P_A)^2 d\bar{F}_p, \quad (7.28)$$

where E[] denotes expectation and P_A is the average power value,

$$P_A = \int_0^{+\infty} P dF_p = -\int_0^{+\infty} P d\bar{F}_p. \quad (7.29)$$

The instantaneous power variance measures the "width" of the CCDF curve and describes in a sense more accurately than the PAPR the envelope of the signals.

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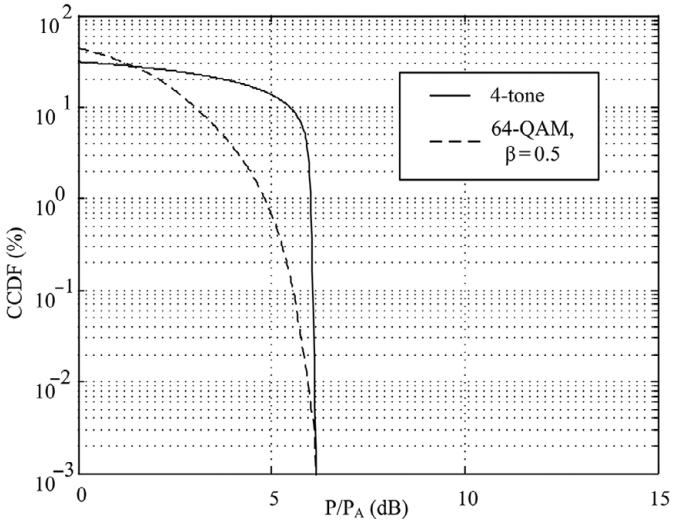

Figure 7.33 CCDF comparison of a four-tone signal and a 64QAM signal with $\beta = 0.5$ with the same PAPR $\approx$ 7dB. ©2016 IEEE. Reprinted with permission from [209]

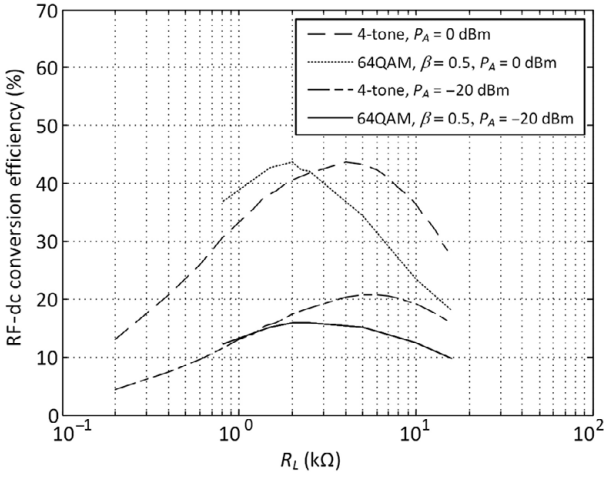

Figure 7.34 RF-dc efficiency comparison obtained using the signals of Figure 7.33. ©2016 IEEE. Reprinted with permission from [209]

It is possible to compute the instantaneous power variance using the CCDF values; however, one should be careful that measurement equipment typically plots the CCDF curve only for values that correspond to power levels that are higher than the average power, and therefore access to the rest of the CCDF values corresponding to power levels below the average power is required. The four-tone signal of Figure 7.33 has a larger instantaneous power variance than the 64 QAM signal and in accordance with the previous measurements it results in the RF-dc conversion efficiency shifting toward higher load values.

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7.10 Problems and Questions

1. What is the power density of an electric field with strength $1V/m$?
2. What is the current responsivity of a detector circuit?
3. What is approximately the state-of-the-art diode rectifier efficiency (based on the available input power) in the low GHz frequency range and for low available input power levels around -20 dBm?
4. Starting from (7.22), compute an approximate expression of the input RF resistance of a series diode rectifier to the limit of small input voltage V_{11}.
5. What is (are) the reason(s) that the efficiency of a diode rectifier is reduced at high input power levels?
6. Consider a charge pump rectifier with $N = 4$ diodes according to Figure 7.14. What is the theoretical maximum bandwidth that can be achieved with a maximum input reflection coefficient magnitude of 0.1 for an available input power of -20 dBm and -10 dBm?
7. What is a resistance compression network? Compute the required inductance L and capacitance C of a resistance compression network operating at 0.9 GHz, where the load resistance varies from 25 Ω to 100 Ω and the input resistance only varies between a value R_{in} and $2R_{in}$.
8. What is the PAPR ratio and the instantaneous power variance of a signal? What can they tell us in terms of the performance of a signal in RF energy harvesting?
9. Based on Figure 7.29, how do BPSK, 8PSK, and QPSK with a roll-off factor $\beta > 0.4$ compare in terms of their performance as RF energy harvesters? Similarly, based on Figure 7.33 how do 64QAM and a four-tone signal compare in terms of PAPR and instantaneous power variance and in terms of their performance as RF energy harvesters?

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