CHAPTER

12 Phase lock loops and synthesizers

Oscillators whose frequencies are derived from a stable reference source are used in transmitters and receivers as L.O.'s for accurate digital tuning. A VCO in a loop that tracks the frequency excursions of an incoming FM signal is a commonly used FM detector. The first widespread use of phase lock loops was in television receivers where they provide noise-resistant locking of the horizontal sweep frequency to the synchronization pulses in the signal.

12.1 Phase locking

A phase lock loop (PLL) circuit forces the phase of a voltage-controlled oscillator (VCO) to follow the phase of a reference signal. Once lock is achieved, i.e., once the phases stay close to each other, the frequency of the VCO will be equal to the frequency of the reference. In one class of applications, the PLL is used to generate a stable signal whose frequency is determined by an unstable (noisy) reference signal. Here the PLL is, in effect, a narrow bandpass filter that passes a carrier, while rejecting its noise sidebands. Examples include telemetry receivers that lock onto weak pilot signals from spacecraft and various "clock smoother" circuits. It is often necessary to lock an oscillator to the suppressed carrier of a modulated signal, an operation known as carrier recovery. In yet another class of applications the PLL is designed to detect all the phase fluctuations of the reference. An example is the PLL-based FM demodulator where the VCO reproduces the input signal, which is usually in the IF band. The voltage applied by the loop to the VCO is proportional to the instantaneous frequency (in as much as the VCO has a linear voltage-to-frequency characteristic), and this voltage is the audio output.

12.1.1 Phase adjustment by means of frequency control

In a PLL, the VCO frequency, rather than phase, is determined by the control voltage, but it is easy to see how frequency control provides phase adjustment.

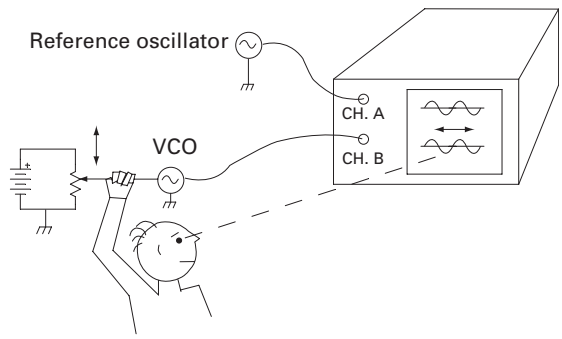


Figure 12.1. Phase lock loop concept.

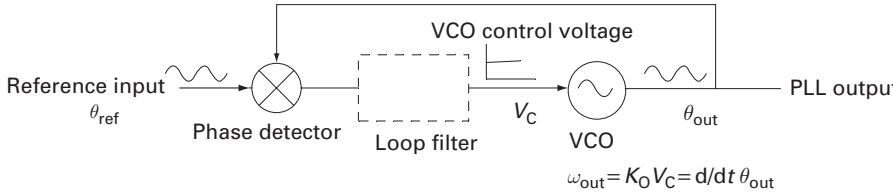


Figure 12.2. Phase lock loop block diagram.

Suppose you have two mechanical clocks. You want to make Clock *B* agree with Clock *A*. You notice that Clock *B* is consistently five minutes behind Clock *A*. You could exert direct phase control, using the time adjustment knob to set Clock *B* ahead 5 min to agree with Clock *A*. Or you could use frequency control, regulating the speed of Clock *B* to run somewhat faster. Once Clock *B* catches up with Clock *A*, you reset the frequency control to its original value. You may have done an electronic version of this in the lab (Figure 12.1). Suppose you have a two-channel oscilloscope. The first channel displays a sine wave from a fixed-frequency reference oscillator. The scope is synchronized to this reference oscillator so Channel *A* displays a motionless sine wave. Channel *B* is connected to a variable frequency oscillator which might be a laboratory instrument with a frequency knob or a VCO fitted with a potentiometer. Suppose the frequencies are the same. Then the sine wave seen on Channel *B* is also motionless. If you lower the VCO frequency slightly, the Channel *B* trace will drift to the right. And if you raise the VCO frequency, the trace will drift to the left. To align the two traces, you can shift the frequency slightly to let the Channel *B* trace drift into position, and then return the VCO frequency to the reference frequency value to stop the drift. The operator keeps the traces aligned and is therefore an element of this phase lock loop.

To automate the loop we use an electronic phase detector, i.e., an element that produces a voltage proportional to the phase difference between the reference and the VCO. Figure 12.2 shows the block diagram for a PLL.

If the VCO phase gets behind (lags) the reference phase, the phase detector will produce a positive "error voltage" which will speed up the VCO. As the phase error then decreases, the error voltage also decreases and the VCO slows

back down. The exact way in which equilibrium is established, i.e., the mathematical form of the VCO phase, $\theta_{out}(t)$, depends on the yet-unspecified loop filter or "compensation network," shown as a dotted box in Figure 12.2. We will examine phase detectors and loop filters below.

12.1.2 Mechanical analog of a PLL

The PLL is a feedback control system – a servo. The electromechanical system shown in Figure 12.3 is a positioning servo. If an operator adjusts the input crank angle, the output shaft automatically turns so that the output angle, θ_{out}, tracks the input shaft angle, θ_{ref}. The gear teeth are in constant mesh but the top gear can slide axially. A dc motor provides torque to turn the output shaft. The input shaft might be connected to the steering wheel of a ship while the output shaft drives the rudder.

Consider the operation of this servo system. Assume for now that the voltage, V_{bias}, is set to zero, and that the system is at rest. When the input and output angles are equal, the slider on the potentiometer is centered and produces zero error voltage. But suppose the reference phase gets slightly ahead of the output phase – maybe the input crank is abruptly moved clockwise. During this motion, the threads on the input shaft have caused the top gear to slide to the left, producing a positive voltage at the output of the potentiometer. This voltage is passed on by the loop filter to the power amplifier and drives the motor clockwise, increasing θ_{out}. This rotates the top gear clockwise. The input shaft is now stationary, so the top gear moves along the threads to the right, reducing the potentiometer output voltage back to zero. The output angle (output phase) is again in agreement with the input or "reference" angle (input phase). In this system the gear/screw thread mechanism is the phase detector. Note that the

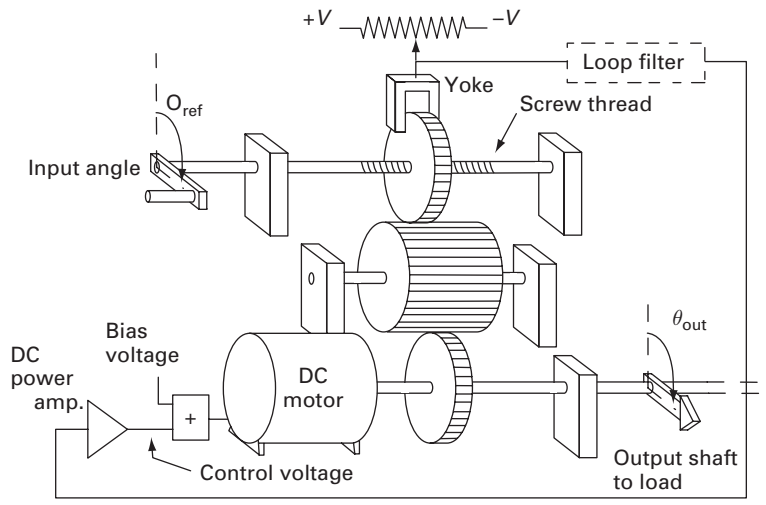


Figure 12.3. Positioning system with feedback control – a mechanical phase lock loop.

range of this phase detector can be many turns – the number of threads on the shaft. The negative feedback error signal provides the drive to force the (high-power) output to agree with the (low-power) input command.

We see how this mechanical system operates as a power-steering servo. To see that it can also operate as a PLL, suppose that an operator is cranking the input shaft at a constant or approximately constant rate (input frequency). We will now set the bias voltage so that, with the bias voltage alone, the motor turns at the nominal input frequency. (A VCO can be regarded as having an internal bias that determines its nominal frequency, i.e., its frequency when the control voltage is zero.) At equilibrium, the top gear is being turned by the middle gear but the threaded shaft is turning just as fast. The top gear therefore does not move along the threads, but stays at an equilibrium position. The output frequency is locked to the input frequency. How about the phases; will they also agree exactly? They did in the power steering model,[1] but now, with continuous rotation, they may not. The key is the loop filter. Suppose the loop filter is just a piece of wire (no filter at all). If the input frequency changes from its nominal value, there will have to be a constant phase error in order to keep the potentiometer off-center and produce a control voltage which will add to or subtract from the bias voltage. How much phase error (*tracking* error) is necessary depends on the gain of the power amplifier. Increasing the gain of the amplifier/motor and/or the gain (sensitivity) of the phase detector will reduce the error. But, if the loop filter contains an integrator, the control voltage will be the integral of the error voltage history. The steady-state error voltage can be zero. In fact, it *must* be zero, on average, or the integrator output, and hence the output frequency, would increase indefinitely.

Note: a servo's *type* is given by the number of integrators contained in its loop. Even without an integrator in the loop filter block, a PLL contains one integrator, the VCO, since phase is the time integral of frequency. In the mechanical analog, rotation angle is the integral of angular velocity.

12.1.3 Loop dynamics

Let us now look at how a PLL responds to disturbances in the input phase. We have already described qualitatively the response to a step function; the loop catches up with the reference. The way in which it catches up, i.e., quickly, slowly, with overshoot, or with no overshoot, depends on the loop filter and the characteristics of the phase detector, amplifier and motor. An exact analysis is straightforward if the entire system is *linear*, i.e., if the system can be described with linear differential equations. In this case it can be analyzed with the standard techniques applied to linear electronic circuits, i.e., complex numbers, Fourier and Laplace transforms, superposition, etc. In the PLL, the loop filter is linear since it consists of passive components: resistors, capacitors, and

[1] We will assume the motor speed is proportional to the applied voltage, independent of load.

op-amps. The VCO is linear if its frequency is strictly proportional to the control voltage. Of course, over a small operating region, any smooth voltage–frequency characteristic is approximately linear. The most commonly used phase detector is a simple multiplier (mixer). You can show[2] that it produces an error voltage proportional to $\sin(\theta_{\text{out}}(t) - \theta_{\text{ref}}(t) + \pi/2)$. For small x, $\sin(x) \approx x$, so a multiplier is a fairly linear phase detector over a restricted region around $\pi/2$. The phase detector in our mechanical analog is linear over a range limited only by the length of the screw thread.

To describe the loop dynamics, we will find its response to an input phase disturbance, $\theta_{\text{dist\_in}} = e^{j\omega t}$. The complete input function is therefore $\theta_{\text{ref}}(t) = \omega_0 t + e^{j\omega t}$. Since the system is linear, we invoke superposition to note that the output will consist of a response to the $\omega_0 t$ term plus an output response to the $e^{j\omega t}$ disturbance term. The input term, $\omega_0 t$, results in an output contribution $\omega_0 t + \Theta$, where the constant Θ might be 90°, if the phase detector is a mixer, and might include another constant, if the nominal frequency of the VCO is not quite ω_0 and the loop filter includes no integrator. Since the input disturbance function is sinusoidal, the output response to it will also be sinusoidal, $A(\omega)e^{j\omega t}$, where the complex amplitude $A(\omega)$ is known as the input-to-output transfer function. Before we can calculate the transfer function, we must specify the loop filter.

12.1.4 Loop filter

A standard filter for type-II loops uses an op-amp to produce a weighted sum of the phase detector output plus the integral of the phase detector output. Figure 12.4 shows the circuit commonly used.

Note that if we let C go to infinity and set $R_2 = R_1$, the response of this filter is just unity (except for a minus sign) so this circuit will serve to analyze the type-I PLL as well as the type-II PLL. Remembering that the negative input of the op-amp is a virtual ground, we can write the transfer function of this filter.

$$\frac{-V_2}{V_1} = \frac{R_2 + 1/j\omega C}{R_1} = \frac{R_2}{R_1} + \frac{1}{j\omega C R_1} = \frac{\tau_2}{\tau_1} - \frac{j}{\omega \tau_1}. \tag{12.1}$$

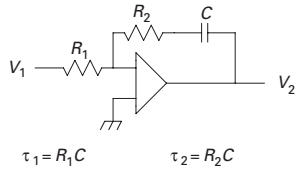


Figure 12.4. Loop filter circuit.

[2] Just expand the product $\cos(\omega_0 t + \theta_{\text{out}}(t))\cos(\omega_0 t + \theta_{\text{ref}}(t))$ and ignore (filter off) components at $2\omega_0$.

In the time domain, the relation between V_2 and V_1 is given by

$$\frac{dV_2}{dt} = \frac{-R_2}{R_1}\frac{dV_1}{dt} - \frac{V_1}{R_1 C}. \tag{12.2}$$

12.1.5 Linear analysis of the PLL

Figure 12.5 is a block diagram of the loop, including the loop filter of Figure 12.4.

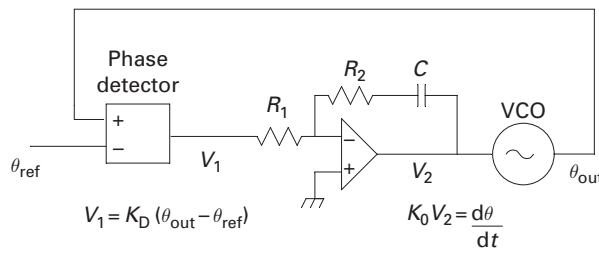


Figure 12.5. Type-II, second-order PLL block diagram.

For this linear system, let us find the frequency response of the output phase to a sinusoidal disturbance of the reference phase, $\theta_{dist}e^{j\omega t}$, where ω is the disturbing frequency. From inspection of Figure 12.5 we can write

$$-K_D(\theta_{out} - \theta_{dist})\left(\frac{\tau_2}{\tau_1} - \frac{j}{\omega\tau_1}\right)K_O = j\omega\theta_{out}. \tag{12.3}$$

Solving for θ, we have the frequency response

$$\frac{\theta_{out}(\omega)}{\theta_{dist}(\omega)} = \frac{1}{1 - \left[K_D K_O/(\omega^2\tau_1) + jK_D K_O\tau_2/(\omega\tau_1)\right]^{-1}}. \tag{12.4}$$

12.1.5.1 Frequency response of the type-I loop

We will look at the frequency response for the type-I loop by letting C go to infinity and letting $R_1 = R_2$, effectively eliminating the loop filter. The frequency response, Equation (12.4), becomes

$$\frac{\theta_{out}(\omega)}{\theta_{dist}(\omega)} \to \frac{1}{1 + j\omega/K}, \tag{12.5}$$

where $K = K_D K_O$, and is called the *loop gain*. The frequency response is identical to that of a simple RC lowpass filter with a time constant $RC = 1/K$. We saw earlier that a type-I PLL (a PLL with no integrator in the loop filter) needs high loop gain to have good tracking accuracy (the ability to follow a changing reference frequency without incurring a large phase error). Here we see that high gain implies a large bandwidth; the type-I PLL cannot have both high gain (for good tracking) and a narrow bandwidth (to filter out high-frequency reference phase noise).

12.1.5.2 Frequency response of the type-II loop

To deal with the type-II loop (the most common PLL) it is standard to define two constants, the *natural frequency*, ω_n, and the *damping coefficient*, ζ, as follows:

$$\omega_n = \sqrt{\frac{K_O K_D}{\tau_1}} \quad \zeta = \frac{\tau_2 \omega_n}{2}. \tag{12.6}$$

We will see soon that these names relate to the transient response of the loop but, for now, we will substitute them into Equation (12.4), the expression for the frequency response, to get

$$\frac{\theta_{out}(\omega)}{\theta_{dist}(\omega)} = \frac{{\omega_n}^2 + 2j\omega\zeta\omega_n}{{\omega_n}^2 + 2j\omega\zeta\omega_n - \omega^2}. \tag{12.7}$$

This transfer function is plotted vs. ω/ω_n in Figure 12.6 for several different damping coefficients.

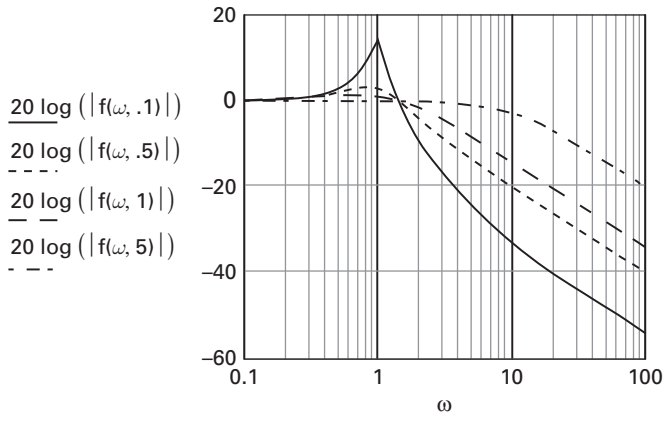


Figure 12.6. Frequency response vs. ω/ω_n for a second-order type-II loop with various damping coefficients.

12.1.5.3 Transient response

The transient response can be determined from the frequency response by using Fourier or Laplace transforms, but this loop is simple enough that we can work directly in the time domain. Equation (12.2) gives the time response for the loop filter. We assume the loop has been disturbed but the reference is now constant. By inspection of Figure 12.5 we can write

$$\frac{dV_1}{dt} = K_D K_O V_2 = K V_2. \tag{12.8}$$

Combining this with Equation (12.2) we get

$$\frac{d^2V_1}{dt^2} + K\frac{\tau_2}{\tau_1}\frac{dV_1}{dt} + \frac{K}{\tau_1}V_1 = 0 \quad \text{or} \quad \frac{d^2V_1}{dt^2} + 2\omega_n\zeta\frac{dV_1}{dt} + {\omega_n}^2 V_1 = 0. \tag{12.9}$$

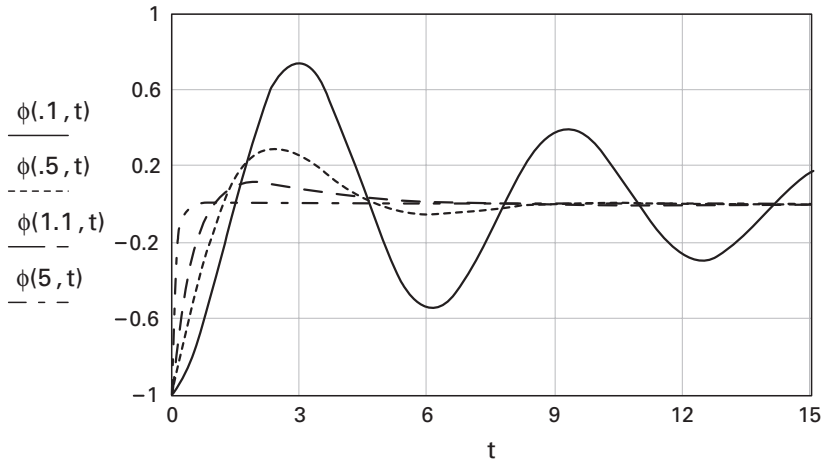


Figure 12.7. Phase error for a step of −1 radian in the reference phase at $t = 0$.

Assuming a solution of the form $e^{j\omega t}$, we find an equation for ω:

$$-\omega^2 + 2j\omega_n\zeta\omega + \omega_n^2 = 0. \tag{12.10}$$

The roots of this equation are

$$\omega = -\omega_n\zeta \pm \omega_n\sqrt{\zeta^2 - 1}. \tag{12.11}$$

When ζ is less than unity, the two solutions for ω are complex conjugates, giving sine and cosine oscillations with damped exponential envelopes. This is the underdamped situation. When ζ is greater than unity, the two solutions for ω are both damped exponentials, but with different time constants. If ζ is exactly unity, the two solutions are $e^{-\omega t}$ and $te^{-\omega t}$. In every case, a linear combination of the two appropriate solutions can match any given set of initial conditions, i.e., the $t = 0$ values of V_1 and $\mathrm{d}/\mathrm{d}t\, V_1$. Figure 12.7 shows the transient phase response to a step function in the reference phase of one radian at $t = 0$. This initial condition, $V_1(0) = -1$, determines the other initial condition, $\mathrm{d}V_1/\mathrm{d}t = 2\zeta\omega_n$, through the action of the loop filter circuit. Curves are shown for the recovery from this transient for damping coefficients of 0.1, 0.5, 1.1 and 5. In each case, $\omega_n = 1$. The underdamped cases show the trademark oscillatory behavior. When the damping is 5, the fast exponential recovery is essentially that of a wideband type-I loop.

Note: Equation (12.10) (which is the same as the denominator of the transfer function) is known as the *characteristic equation* of the system. Here it is a second-order equation and this type-II loop is therefore also a second-order loop. Equivalently, the order of a given system is the order of the differential equation describing its transient response.

12.1.6 A multiplier as a phase detector

A multiplier (mixer) is the most commonly used phase detector, especially at higher frequencies. When the reference sine wave is multiplied by the VCO sine

wave, the usual sum and difference frequencies are generated. The desired baseband output is the difference component. If the VCO and reference frequencies are equal, this baseband component will be a dc voltage, zero when the VCO and reference phases differ by 90°, and linearly proportional to the phase difference in the vicinity of 90°. Therefore, when a multiplier is used as a phase detector, the loop will lock with the output phase 90° away from the reference phase. If this is a problem (in most applications it is not), a 90° phase shift network can be put at one of the multiplier inputs or in the output line. Note that a multiplier phase detector puts out zero volts when the phase shifts are different by 90° in either direction. One of these is a point of metastable equilibrium. As soon as it "falls off," the feedback will be positive, rather than negative, and the loop will rush to the stable equilibrium point.

As a phase detector, a mixer has a linear response of about $\pm \pi/4$, where $\sin(x) \approx x$. For somewhat larger phase differences, the sine curve flattens out and K_D begins to decrease. The system becomes nonlinear and the techniques of linear analysis fail. What is more important, if $\theta_{out} - \theta_{dist}$ needs to increase beyond $\pm \pi/2$, the $\sin(\theta_{out} - \theta_{dist})$ response of the mixer produces alternating positive and negative error signals, which will push the VCO frequency one way and then the other, and the loop will become unlocked. This is in contrast to the mechanical analog of Figure 12.3, whose phase detector range is 2π times the number of threads on the phase detector shaft. Electronic *phase/frequency detectors* (PFDs) are digital circuits that operate as linear phase detectors while the phase difference remains small, but then produce an output voltage proportional to the frequency difference, driving the loop in the correct direction to achieve lock. How a simple mixer-based PLL ever manages to lock without assistance is discussed below.

12.1.7 Frequency range and stability

The type-II loop can operate over the full range of the VCO since its integrator can build up as much bias as needed. The type-I loop, if $K_D K_O$ is small and if the phase detector has a limited range, may not be able to track over the full range of the VCO. Both the loops discussed above are unconditionally stable since the transient responses are decaying exponentials for any combination of the parameters K_D, K_O, R_1, R_2, and C. When you build one and it oscillates it is usually because you have high-frequency poles you did not consider (maybe in your op-amp or circuit parasitics) and you have actually built a higher-order loop.

12.1.8 Acquisition time

A high-gain type-I loop can achieve lock very quickly. A type-II loop with a small bandwidth can be very slow. Acquisition depends on some of the beat note from the phase detector getting through the filter to FM modulate the VCO. That beat note puts a pair of small sidebands on the VCO output. One of these

sidebands will be at the reference frequency and will mix with the reference to produce dc with the correct polarity to push the VCO toward the reference frequency. The integrator gradually builds up this dc until the beat frequency comes within the loop bandwidth. From that point the acquisition is very fast. This reasoning, applied to the type-II loop, predicts an acquisition time of about $4f^2/B^3$ seconds where f is the initial frequency error and B is the bandwidth of the loop (see Problem 12.6). If the bandwidth is 10 Hz and the initial frequency error is 1 kHz, the predicted time is about one hour. (In practice, unavoidable offsets in the op-amp would make the integrator drift to one of the power supply rails and never come loose.) Obviously in such a case some assist is needed for a lockup. One common method is to add search capability, i.e., circuitry that causes the VCO voltage to sweep up and down until some significant dc component comes out of the phase detector. At that point the search circuit turns off and the loop locks itself up. The integrator can form part of the sweep circuit. Another way to aid acquisition is to use a frequency/phase detector instead of a simple phase detector. This is a digital phase detector which, when the input frequencies are different, puts out dc whose polarity indicates whether the VCO is above or below the reference. This dc quickly pumps the integrator up or down to the correct voltage for lock to occur. You will see these circuits described in Motorola literature. In digitally controlled PLLs, it is common for a microprocessor with a lookup table in ROM to pretune the VCO to the commanded frequency. This pretuning allows the loop to acquire lock quickly.

12.1.9 PLL receiver

There are many inventive circuits and applications in the literature on PLLs. Here is an example: deep space probes usually provide very weak telemetry signals. The receiver bandwidth must be made very small to reject noise that is outside the narrow band containing the modulated signal. A PLL can be used to do the narrowband filtering and to do the detection as well. One simple modulation scheme uses slow-frequency shift keying (FSK) where the signal is at one frequency for a "0" and then slides over to a second frequency for a "1." The loop bandwidth of the PLL is made just wide enough to follow the keying. The control voltage on the VCO is used as the detected signal output. (With a wide loop bandwidth, such a circuit can demodulate ordinary FM audio broadcast signals.) In this narrowband example, the PLL circuit has the advantage that it will track the signal automatically when the transmitter frequency drifts or is Doppler shifted. Another modulation scheme uses phase shift keying (PSK). Suppose the transmitter phase is shifted 180° to distinguish a "1" from a "0." This would confuse the PLL receiver because, for random data, the average output from the phase detector would be zero and the PLL would be unable to lock. A simple cure is to use the "doubling loop" shown in Figure 12.8. The incoming signal is first sent through a doubler to produce an output that looks like the output of a full-wave rectifier. (The waveform loops are positive no

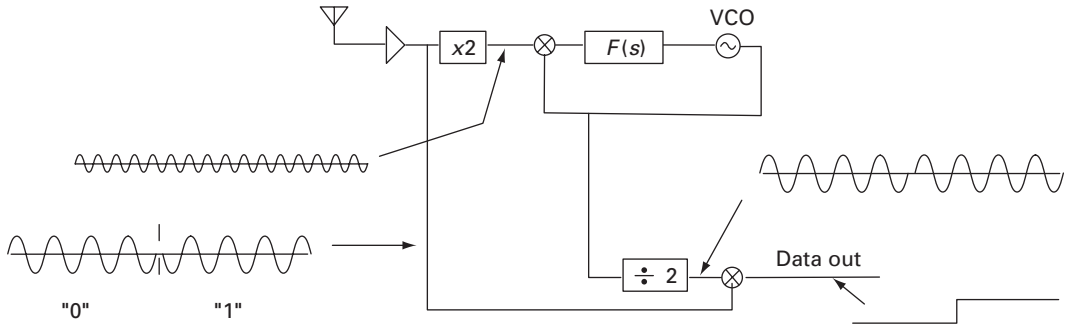


Figure 12.8. Doubling loop for detection of binary phase-shift modulation.

matter what the modulation does.) The VCO output frequency is then divided by two to produce a phase-locked reference. This reference is used as one input of a mixer. The other input of the mixer is the raw signal and the output is the recovered modulation.

12.2 Frequency synthesizers

By *frequency synthesizer* we usually mean a signal generator which can be switched to put out any one of a discrete set of frequencies and whose frequency stability is derived from a standard oscillator, either a built-in crystal oscillator or an external "station standard." Most laboratory synthesizers generate sine waves but some low-frequency synthesized function generators also generate square and triangular waves. General-purpose synthesizers have high resolution; the step between frequencies is usually less than 1 Hz and may be millihertz or even microhertz. Many television receivers and communications receivers have synthesized local oscillators. Special-purpose synthesizers may generate only a single frequency.

At least three general techniques are used for frequency synthesis. *Direct synthesizers* use frequency multipliers, frequency dividers, and mixers. *Indirect synthesizers* use phase lock loops. *Direct digital synthesizers* use a digital accumulator to produce a staircase sawtooth. A lookup table then changes the sawtooth to a staircase sinusoid, and a D-to-A converter provides the analog output. Some designs combine these three techniques.

12.2.1 Direct synthesis

The building blocks for direct synthesis are already familiar. Frequency multiplication can be done with almost any nonlinear element. A limiting amplifier (limiter) or a diode clipper circuit will convert sine waves into square waves, which include all the odd harmonics of the fundamental frequency. A delta function pulse train (in practice, a train of narrow pulses) contains all harmonics. When frequencies in only a narrow range are to be multiplied, class-C amplifiers can be used. (A child's swing does not need a push on each and every

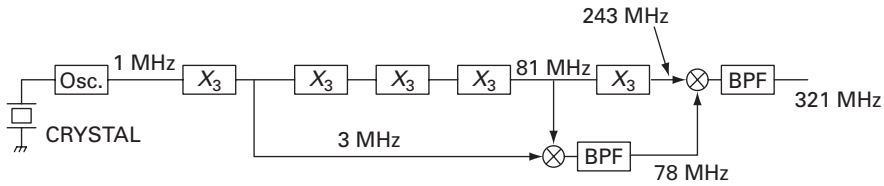


Figure 12.9. A direct synthesizer that produces 321 MHz from a 1-MHz reference.

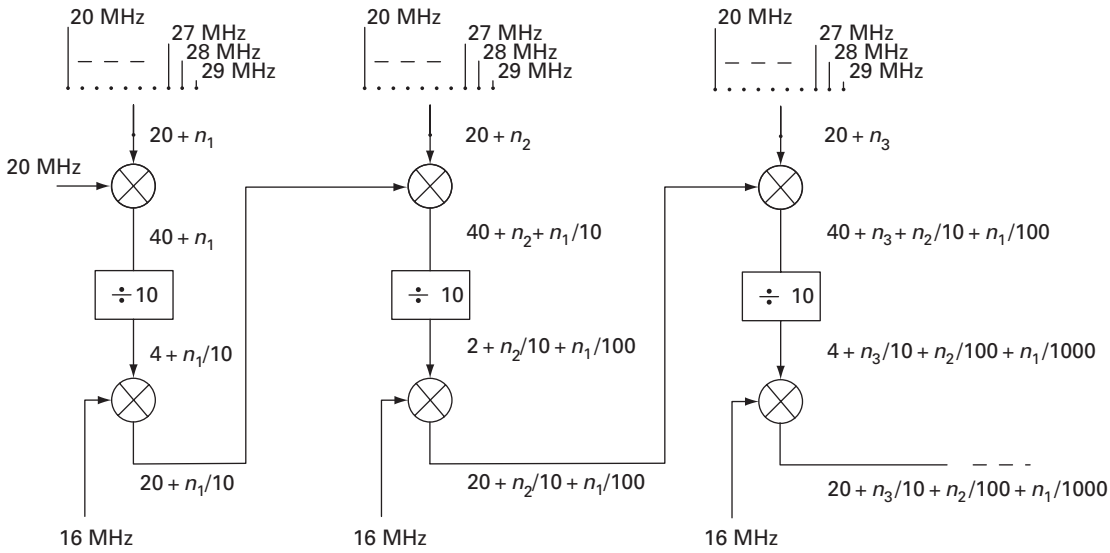
cycle.) Frequency division, used in all three types of synthesizers, is almost always done digitally; the input frequency is used as the clock for a digital counter made of flip-flops and logic gates. Frequency translation can be done with any of the standard mixer circuits.

Single-frequency synthesizers are usually ad hoc designs; the arrangement of mixers, multipliers, and dividers depends on the ratio of the desired frequency and the reference frequency. As an example of direct synthesis, the circuit of Figure 12.9 generates 321 MHz from a 1-MHz standard. A prime factor of 321 is 107. It would be difficult to build a times-107 multiplier. This design uses only triplers and mixers. Laboratory instruments that cover an entire range of frequencies must, of course, use some general scheme of operation.

12.2.2 Mix and divide direct synthesis

Some laboratory synthesizers use an interesting mix and divide module. An n-digit synthesizer would use n identical modules. An example is shown in Figure 12.10. Each module has access to a 16-MHz source and ten other

Figure 12.10. A mix-and-divide direct synthesizer.



reference sources from 20 to 29 MHz. (These references are derived from an internal or external standard, often at 5 MHz). In this kind of design the internal frequencies must be chosen carefully so that after each mixer the undesired sideband can be filtered out easily.

12.2.3 Indirect synthesis

The phase lock loop circuit of Figure 12.11 is an indirect synthesizer to generate the frequency Nf_{std}/M where N and M are integers. If the $\div N$ and/or the $\div M$ blocks are variable modulus counters, the synthesizer frequency is adjustable.

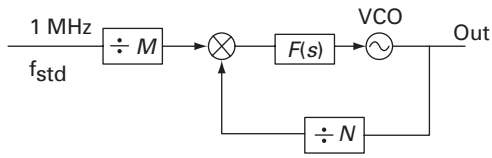


Figure 12.11. Basic indirect (PLL) synthesizer.

The 321-MHz synthesizer of Figure 12.9 could be built as the indirect synthesizer of Figure 12.11 by using a divide-by-321 counter (most likely a divide-by-3 counter followed by a divide-by-107 counter). Circuits like that of Figure 12.11 are used as local oscillators for digitally tuned radio and television receivers. For an AM broadcast band receiver, the frequency steps would be 10 kHz (the spacing between assigned frequencies). This requires that the phase detector reference frequency, f_{std}/M, be 10 kHz so only the modulus N would be adjustable. What about a synthesized local oscillator for a short-wave radio? We would probably want a tuning resolution of, say, 10 Hz. The reference frequency in the simple circuit of Figure 12.11 would have to be 10 Hz and the loop bandwidth would have to be about 2 Hz. This low bandwidth would make fast switching difficult. Moreover, with such a narrow loop bandwidth, the close-in noise of the VCO would not be cleaned up by the loop and the performance of the radio would suffer. For this application a more sophisticated circuit is needed. One method is to synthesize a VHF or UHF frequency with steps of 1 or 10 kHz, divide it to produce the necessary smaller steps, and then mix it to a higher frequency. Other circuits use complicated multiple loops. The newest receivers use L.O. synthesizers based on the principle of direct digital synthesis.

12.2.4 Direct digital synthesis (DDS)

This technique, illustrated in Figure 12.12, uses an adder with two n-bit inputs, A and B, together with an n-bit register to accumulate phase. The output of the adder is latched into the register on every cycle of a high-frequency clock. The inputs to the adder are the current register contents (the phase) and an adjustable addend (the phase increment). On every clock cycle, the accumulated phase increases by an amount given by the addend. Since the accumulator has a finite

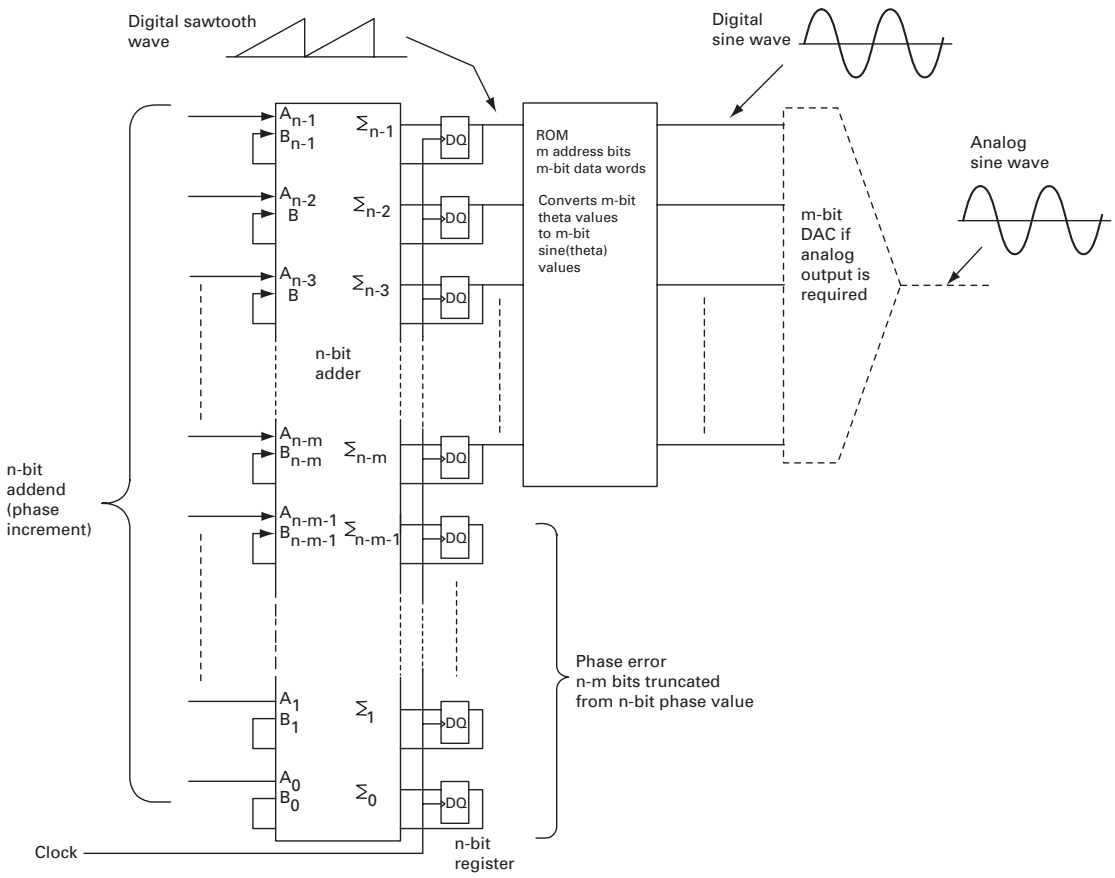


Figure 12.12. Direct digital synthesizer (DDS).

length, it rolls over, like an automobile odometer, and the sequence of its output values forms a sawtooth wave. The maximum addend value is 2^{n-1}, where n is the number of bits in the adder/accumulator. Therefore, the output frequency of the DDS extends up to one-half the clock frequency. At this maximum frequency, the MSB toggles on every clock pulse and the lower bits remain constant. The output of the accumulator is used to address a ROM (read-only memory) that converts the stairstep digital sawtooth into a stairstep digital sine wave.

Let us consider the operation of the DDS in some detail. Suppose the selected addend is the integer A. Let θ_i denote the number held in the register after the i-th clock pulse. Because the accumulator rolls over when the output value would have reached or exceeded 2^n, we can write $\theta_i = (\theta_{i-1} + A) \bmod 2^n$, a formula which lets us easily simulate the DDS. On average, it will take $2^n/A$ clock pulses to fill the accumulator,[3] so the average period of the sawtooth wave will be $f_{\text{clk}}{}^{-1}$ $2^n/A$ and the output frequency will be $f_{\text{clk}}\, A/2^n$. This frequency can be changed

[3] Consider that, after every $2^n A$ clock pulses, the accumulator must return to the same value. During that period, the value that would be accumulated without rollover is $A(2^n A)$. Thus the number of rollovers would be A^2. The average time per rollover is therefore $f_{\text{clk}}{}^{-1}$ $(2^n A)$ $/A^2 = f_{\text{clk}}{}^{-1}$ $2^n/A$.

in very fine increments if the number of bits in the accumulator is large. With a 32-bit accumulator, for example, the frequency resolution will be $f_{\text{clock}}/2^{32}$. For a clock frequency of 100 MHz the resolution will be $10^8/2^{32} = 0.023$ Hz.

One might think that, since the most significant bit (MSB) of the accumulator toggles at the desired output frequency, we could use it alone, simply filtering away its harmonics to obtain a sine wave at the desired frequency. However, while the MSB has the right *average* frequency it can be quite irregular. If the addend is a power of 2, the MSB will toggle at uniform time intervals but otherwise the MSB will have a jitter which depends on the value of the addend. A sine wave made from just the MSB would, therefore, contain too much phase noise (FM noise) for most RF applications.

The solution is to use more than just the top bit. If we use the top m bits, then the phase error is never greater than $360/2^m$ degrees. A table-lookup ROM uses these m-bit phase values, θm_i, as address bits to produce an output sequence, $\sin(\theta m_i)$, which has the desired wave shape (except for the roundoff error), together with low phase noise. An analog output can be provided by adding an m-bit D-to-A converter but, in digital radio applications, the digital sine wave is used directly. The more bits used to form the output sine wave, the lower the phase noise. Note that the DDS can incorporate the technique of digital pipelining in the adder/accumulator to achieve simultaneously high output frequencies and fine frequency resolution. The pipe delay is of no consequence for most system applications. Note also that the DDS can easily be modified to produce a chirped frequency by adding another accumulator to produce a sawtooth addend value. A precise FM modulator consists of a DDS whose addend is the digitized audio signal. Clock rates in DDS ICs have reached several GHz.

Output spectrum of the DDS

The exact spectrum of the DDS output can be calculated directly using Fourier analysis. For any value of the addend, the sequence of accumulator values will always repeat after at most 2^n clock pulses. Therefore, the sequence of digital values produced by the lookup ROM also repeats after at most 2^n cycles. This repetitive waveform can be represented as a Fourier series whose components are spaced in frequency by at least $f_{\text{clk}}/2^n$. The squares of the Fourier coefficients at each frequency are proportional to power. A simpler and more instructive approach is to note that the number contained in truncated accumulator bits (the bits below $n - m$) is just the phase error, $\delta\theta_i = \theta_i - \theta m_i$. The output sequence formed by the m-bit numbers can therefore be written as

$$\sin(\theta m_i) = \sin(\theta_i - \delta\theta_i) \approx \sin(\theta_i) - \delta\theta_i \cos(\theta_i), \tag{12.12}$$

where we have assumed $\delta\theta_i$ is small. The term $\sin(\theta_i)$ is the desired output, while the term $\delta\theta_i \cos(\theta_i)$ is the noise. The error sequence, $\delta\theta_i \cos(\theta_i)$, will repeat after, at most, 2^{n-m} clock pulses, so the noise forms a Fourier series with components separated in frequency by at least $f_{\text{clk}}/2^{n-m}$. The nature of the noise will depend on the value of the bottom part of the addend, i.e., the lowest $n - m$ bits of the

addend. If that number is a power of 2, the noise components will fall at harmonics of the output frequency, distorting the output waveform slightly, but contributing no phase noise. If the bottom part of the addend contains no factors of 2, the noise may be a grass of components at all multiples of $f_{clk}/2^{n-m}$. The more factors of 2 in the bottom part of the addend, the wider the spacing between noise components. Thus, the nature of the noise can change dramatically from one output frequency to the next.

12.2.5 Switching speed and phase continuity

Indirect synthesizers cannot change frequency faster than the time needed for their phase lock loops to capture and settle. Direct synthesizers and direct digital synthesizers can switch almost instantly. Sometimes it is necessary to switch frequencies without losing phase continuity. The DDS is perfect for this since the addend is changed and the phase rate changes but there is no sudden phase jump. Other times, when the synthesizer is retuned to a previously selected frequency, the phase must take on the value it would have had if the frequency had never been changed. This second kind of continuity might be called phase memory. A frequency synthesizer that provides the first kind of phase continuity clearly will not provide the second and vice versa. Continuity of the second kind can be obtained with a direct synthesizer that uses only mixers and multipliers (no dividers – which can begin in an arbitrary state).

12.2.6 Phase noise from multipliers and dividers

It is important to see how any noise on the reference signal of a synthesizer determines the noise on its output signal. Let us examine how noise is affected by the operations of frequency multiplication and division. We will assume the input noise sidebands are much weaker than the carrier. Suppose the input signal has a discrete sideband at 60 Hz. (Such a sideband would normally be one of a pair but for this argument we can consider them one at a time.) Let this sideband have a level of −40 dBc, i.e., its power is 40 dB below the carrier power. If this signal drives a times-N frequency multiplier, it turns out that the output signal will also have a sideband at 60 Hz but its level will be $-40 + 20\log(N)$ dBc. The relative sideband power increases by the *square* of the multiplication factor.

Let us verify this, at least for a specific case – a particular frequency tripler. Let the input signal be $\cos(\omega t) + \alpha\cos([\omega+\delta\omega]t)$, i.e., a carrier at ω having a sideband at $\omega+\delta\omega$ with relative power of α^2 or $20\log(\alpha)$ dBc. We assume that $\alpha \ll 1$. Here the tripler will be a circuit whose output voltage is the cube of the input voltage. Expanding the output and keeping only terms of order α or higher whose frequencies are at or near $3f$ we have

$$[\cos(\omega t) + \alpha\cos[(\omega+\delta\omega)t]]^3 \rightarrow \cos^3(\omega t) + 3\alpha\cos^2(\omega t)cos[(\omega+\delta\omega)t] \tag{12.13}$$

$$\rightarrow 1/2\ \cos(\omega t)\cos(2\omega t) + 3/2\ \alpha\cos(2\omega t)\cos[(\omega+\delta\omega)t]$$

$$\rightarrow 1/4\ \cos(3\omega t) + 3/4\ \alpha\cos[(3\omega+\delta\omega)t]$$
$$= 1/4\ [\cos(3\omega t) + 3\alpha\cos[(3\omega+\delta\omega)t]]. \quad (12.14)$$

Note that the carrier-to-sideband spacing is still $\delta\omega$ but the relative amplitude of the sideband has gone up by 3, the multiplication factor. The relative power of the sideband has therefore increased by 3^2, the square of the multiplication factor. A continuous distribution of phase noise $S(\delta\omega)$ is like a continuous set of discrete sidebands so, if the noise spectrum of a multiplier input is $S(\delta\omega)$, the noise spectrum of the output will be $n^2S(\delta\omega)$. Sideband noise enhancement is a direct consequence of multiplication. If the multiplier circuit itself is noisy, the output phase noise will increase by more than n^2. Fortunately, most multipliers contribute negligible additive noise.

Division, the inverse of multiplication, reduces the phase noise power by the square of the division factor. Mixers just translate the spectrum of signals; they do not have a fundamental effect on noise. Additive noise from mixers is usually negligible. If a direct synthesizer is built with ideal components, the relation between the output phase noise and the phase noise of the standard will be as if the synthesizer were just a multiplier or divider, no matter what internal operations are used. The phase noise produced by indirect synthesizers depends on the quality of the internal VCOs and the bandwidths of the loop filters.

Problems

*These more difficult problems could be used as projects.

Problem 12.1. How would you modify the gear train in Figure 12.3 so that the output shaft would turn N/M times faster than the input shaft?

Problem 12.2. Show that Equation (12.2) describes the time domain input/output relation for the loop filter circuit of Figure 12.4.

Problem 12.3. Suppose the VCO in the block diagram of Figure 12.5 is noisy and that its noise can be represented as an equivalent noise voltage added at the control input of the VCO. Redraw the block diagram showing a summing block just in front of the VCO. Find the frequency transfer function for this noise input. Show that the loop is able to "clean up" the low-frequency noise of the VCO.

Problem 12.4.* Write a computer program to numerically simulate the PLL shown in Figure 12.5. Use a multiplier type phase detector and investigate the process of lock-up. Let the phase detector output be proportional to $\cos(\theta-\theta_{\text{ref}})$. Use numerical integration on the simultaneous first-order differential equations for $V_1(t)$ and $V_2(t)$.

Problem 12.5.* Invent a phase detector circuit that would have a range of many multiples of 2π rather than the restricted range of the multiplier phase detector.

Problem 12.6.* Derive the formula given for lock-up time, $\tau_{LOCKUP} \approx 4(\Delta\omega)^2/B^3$, where $\Delta\omega$ is the initial frequency error and B is the loop bandwidth (in radians/sec). Consider the type-II loop of Figure 12.5. Find the ac component on the VCO control input. Assume that $\Delta\omega$ is high enough that the gain of the loop filter for this ac voltage is just $-R_2/R_1$. Find the amplitude of the sidebands caused at the output of the VCO from this ac control voltage component. Use this amplitude to find the dc component at the output of the phase detector caused by product of the reference signal and the VCO sideband at the reference frequency. This dc component will be integrated by the loop filter. Find dV/dt at the output of the loop filter. Find an expression for τ_{LOCKUP} by estimating the time for the dc control voltage to change by the amount necessary to eliminate the initial error.

Problem 12.7. Design a direct synthesizer (ad hoc combination of mixers, dividers, multipliers) to produce a frequency of 105.3 MHz from a 10-MHz reference. Avoid multipliers higher than ×5 and do not let the two inputs of any mixer have a frequency ratio higher than 5:1 (or lower than 1:5).

Problem 12.8. Design a direct digital synthesizer with 10-kHz steps for use as the tunable local oscillator in a middle-wave broadcast band (530–1700 kHz) AM receiver with a 455 kHz IF frequency. Assume a high-side L.O., i.e., the synthesizer frequencies range from 530 + 455 to 17800 + 455 An accurate reference frequency is available at 10.24 MHz.

Problem 12.9. Design a synthesizer with the range of 1–2 MHz that has phase memory, i.e., when the synthesizer is reset to an earlier frequency, its phase will be the same as if it had been left set to the earlier frequency. The required step size is 50 kHz and the available frequency reference is 5 MHz. Hint: one approach is to generate a frequency comb with a spacing of 50 kHz and then phase-lock a tunable oscillator to the desired tooth of the comb.

Problem 12.10. Explain why a direct synthesizer that includes one or more dividers will not have phase memory.

Problem 12.11. Draw a block diagram for an FM transmitter in which a phase locked loop keeps the average frequency of the VCO equal to a stable reference frequency.

Problem 12.12. Draw block diagrams for PM and FM generators based on the direct digital synthesizer (DDS) principle.

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