APPENDIX D

Component Data

This appendix gives data for most of the components that are used in the NorCal 40A. We appreciate the manufacturers giving us permission to copy data sheets. Often data sheets have a great deal of information, but it is important to make your own measurements to check them. Manufacturers vary greatly in how conservatively they rate their devices. In addition, they may be testing the devices under conditions that are different from yours. Often several manufacturers sell a device with same part number, and the performance between different manufacturers varies. These data sheets are no substitute for the data books and Web sites that give the complete list of products that a manufacturer sells. Many of these devices are part of a wide line of products that will cover a range of frequencies, functions, and power levels. For much more component information, see *Data Book for Homebrewers and QRPers,* by Paul Harden, published by Quicksilver Printing. The book is available from Five Watt Press, 740 Galena Street, Aurora, CO 80010-3922, email: qrpbook@aol.com.

Table D.1. Resistors, inductors and capacitors
Table D.2. Iron and ferrite cores

Motorola – http://mot2.indirect.com

1N5817 Schottky barrier rectifier
MVAM108 silicon tuning diode
P2N2222A general purpose npn silicon transistor
2N3553 2.5-W high frequency npn silicon transistor
2N3906 general purpose pnp silicon transistor
2N4124 general purpose npn silicon transistor
J309 n-channel VHF/UHF JFET
MC78L08AC three-terminal low-current, positive-voltage regulator

National Semiconductor – http://www.national.com

LM386N-1 National Semiconductor low-voltage audio power amplifier

Philips – http://www.semiconductors.philips.com

1N4148 high-speed diode
SA602AN double-balanced mixer and oscillator

Table D.1. Characteristics of the Resistors, Inductors and Capacitors in the NorCal 40A.

Type	±%	Range	ppm/°C	Q	Use
carbon film resistor	5	1 Ω–1 MΩ	−240		dividers, damping
inductors	5	220 nH–1 mH	+1,200	50 at 7 MHz	chokes, filters
small ceramic	5	10–1,000 pF	−800	600 at 7 MHz	RF filters
NPO ceramic	5	18–220 pF	−30	800 at 2 MHz	VFO resonator
large ceramic	20	1–47 nF	−30,000	20 at 7 MHz	RF bypass
polystyrene	5	100 pF–10 nF	−150	250 at 2 MHz	VFO resonator
polyester film	5	1–470 nF	+900	240 at 1 kHz	audio coupling
aluminum electrolytic	20	220 nF–10 mF	+2,000	6 at 1 kHz	audio filtering, supply filtering
air variable		2–24 pF	+50	1,000 at 2 MHz	VFO adjustment
ceramic trimmer		7–70 pF	−1,600	200 at 7 MHz	filter adjustment, crystal oscillator
varactor MVAM108		30–500 pF	+500	150 at 2 MHz (3 V bias)	VFO tuning

Note: ±% gives the tolerance. Parts with a tolerance of 5% are made with standard values, where the first two digits come from this list: 10, 11, 12, 13, 15, 16, 18, 20, 22, 24, 27, 30, 33, 36, 39, 43, 47, 51, 56, 62, 68, 75, 82, 91. For 20% parts, the standard values are typically 10, 22, 33, 47, and 68. The range of values are those listed in a catalog for the particular line of parts that we use. For variable components, "range" gives the extreme adjustable values that we measured. The column "ppm/°C" gives our measured values of the temperature coefficient for a representative part; "ppm" is parts per million. "NPO" designates a part with a low-temperature coefficient. The *Q*s are also our measured values. They vary with frequency. Perhaps it is surprising that even the air variable capacitor has a temperature coefficient, but you should remember that metals expand as the temperature goes up.

Table D.2. The Cores in the NorCal 40A Transceiver.

Core	A_l, nH/turn²	Q	ppm/°C	Material	Paint	Use
T37-2	4.0 (28 turns)	170	+100	iron powder	red	filter
T68-7	5.0 (60 turns)	200	+50	iron powder	white	oscillator
FT37-43	160 (14 turns)	1	−30	nickel–zinc ferrite	orange spot	transformer
FT37-61	66 (1 turns)	50	+500	nickel–zinc ferrite	none	tuned transformer

Note: There is a lot of information in the core number itself. For example, in FT37-43, "F" indicates a ferrite, "T" a toroidal core, "37" the outside diameter in hundredths of an inch, and "61" the manufacturing recipe. These are our measured values for A_l, Q, and the temperature coefficient. The values of A_l vary ±10% from lot to lot. All measurements are at 7 MHz, except for the T68-7 core, which is at 2 MHz. The values vary with frequency, and if the specific value of the inductance is critical, you should measure the inductance constant at the frequency you are interested in. Temperature coefficients are given for ferrites for completeness, but it is a poor idea to use ferrites in an application where temperature stability is important, because characteristics differ greatly over even a modest range of temperature.

MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

Order this document
by 1N5817/D

Axial Lead Rectifiers

1N5817
1N5818
1N5819

1N5817 and 1N5819 are
Motorola Preferred Devices

SCHOTTKY BARRIER
RECTIFIERS
1 AMPERE
20, 30 and 40 VOLTS

CASE 59–04

. . . employing the Schottky Barrier principle in a large area metal–to–silicon power diode. State–of–the–art geometry features chrome barrier metal, epitaxial construction with oxide passivation and metal overlap contact. Ideally suited for use as rectifiers in low–voltage, high–frequency inverters, free wheeling diodes, and polarity protection diodes.

- Extremely Low v_F
- Low Stored Charge, Majority Carrier Conduction
- Low Power Loss/High Efficiency

Mechanical Characteristics

- Case: Epoxy, Molded
- Weight: 0.4 gram (approximately)
- Finish: All External Surfaces Corrosion Resistant and Terminal Leads are Readily Solderable
- Lead and Mounting Surface Temperature for Soldering Purposes: 220°C Max. for 10 Seconds, 1/16″ from case
- Shipped in plastic bags, 1000 per bag.
- Available Tape and Reeled, 5000 per reel, by adding a "RL" suffix to the part number
- Polarity: Cathode Indicated by Polarity Band
- Marking: 1N5817, 1N5818, 1N5819

MAXIMUM RATINGS

Rating	Symbol	1N5817	1N5818	1N5819	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage	V_{RRM} V_{RWM} V_R	20	30	40	V
Non–Repetitive Peak Reverse Voltage	V_{RSM}	24	36	48	V
RMS Reverse Voltage	$V_{R(RMS)}$	14	21	28	V
Average Rectified Forward Current (2) ($V_{R(equiv)} \leq 0.2\ V_R(dc)$, $T_L = 90°C$, $R_{\theta JA} = 80°C/W$, P.C. Board Mounting, see Note 2, $T_A = 55°C$)	I_O		1.0		A
Ambient Temperature (Rated $V_R(dc)$, $P_{F(AV)} = 0$, $R_{\theta JA} = 80°C/W$)	T_A	85	80	75	°C
Non–Repetitive Peak Surge Current (Surge applied at rated load conditions, half–wave, single phase 60 Hz, $T_L = 70°C$)	I_{FSM}		25 (for one cycle)		A
Operating and Storage Junction Temperature Range (Reverse Voltage applied)	T_J, T_{stg}		–65 to +125		°C
Peak Operating Junction Temperature (Forward Current applied)	$T_{J(pk)}$		150		°C

THERMAL CHARACTERISTICS (2)

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	80	°C/W

ELECTRICAL CHARACTERISTICS ($T_L = 25°C$ unless otherwise noted) (2)

Characteristic	Symbol	1N5817	1N5818	1N5819	Unit
Maximum Instantaneous Forward Voltage (1) ($i_F = 0.1$ A) ($i_F = 1.0$ A) ($i_F = 3.0$ A)	v_F	0.32 0.45 0.75	0.33 0.55 0.875	0.34 0.6 0.9	V
Maximum Instantaneous Reverse Current @ Rated dc Voltage (1) ($T_L = 25°C$) ($T_L = 100°C$)	I_R	1.0 10	1.0 10	1.0 10	mA

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%.
(2) Lead Temperature reference is cathode lead 1/32″ from case.

Preferred devices are Motorola recommended choices for future use and best overall value.

Rev 3

MOTOROLA

1N5817 1N5818 1N5819

NOTE 1 — DETERMINING MAXIMUM RATINGS

Reverse power dissipation and the possibility of thermal runaway must be considered when operating this rectifier at reverse voltages above 0.1 V_{RWM}. Proper derating may be accomplished by use of equation (1).

$$T_{A(max)} = T_{J(max)} - R_{\theta JA}P_{F(AV)} - R_{\theta JA}P_{R(AV)} \quad (1)$$

where $T_{A(max)}$ = Maximum allowable ambient temperature
$T_{J(max)}$ = Maximum allowable junction temperature (125°C or the temperature at which thermal runaway occurs, whichever is lowest)
$P_{F(AV)}$ = Average forward power dissipation
$P_{R(AV)}$ = Average reverse power dissipation
$R_{\theta JA}$ = Junction–to–ambient thermal resistance

Figures 1, 2, and 3 permit easier use of equation (1) by taking reverse power dissipation and thermal runaway into consideration. The figures solve for a reference temperature as determined by equation (2).

$$T_R = T_{J(max)} - R_{\theta JA}P_{R(AV)} \quad (2)$$

Substituting equation (2) into equation (1) yields:

$$T_{A(max)} = T_R - R_{\theta JA}P_{F(AV)} \quad (3)$$

Inspection of equations (2) and (3) reveals that T_R is the ambient temperature at which thermal runaway occurs or where T_J = 125°C, when forward power is zero. The transition from one boundary condition to the other is evident on the curves of Figures 1, 2, and 3 as a difference in the rate of change of the slope in the vicinity of 115°C. The data of Figures 1, 2, and 3 are based upon dc conditions. For use in common rectifier circuits, Table 1 indicates suggested factors for an equivalent dc voltage to use for conservative design, that is:

$$V_{R(equiv)} = V_{in(PK)} \times F \quad (4)$$

The factor F is derived by considering the properties of the various rectifier circuits and the reverse characteristics of Schottky diodes.

EXAMPLE: Find $T_{A(max)}$ for 1N5818 operated in a 12–volt dc supply using a bridge circuit with capacitive filter such that I_{DC} = 0.4 A ($I_{F(AV)}$ = 0.5 A), $I_{(FM)}/I_{(AV)}$ = 10, Input Voltage = 10 $V_{(rms)}$, $R_{\theta JA}$ = 80°C/W.

Step 1. Find $V_{R(equiv)}$. Read F = 0.65 from Table 1,
$\therefore V_{R(equiv)}$ = (1.41)(10)(0.65) = 9.2 V.
Step 2. Find T_R from Figure 2. Read T_R = 109°C
@ V_R = 9.2 V and $R_{\theta JA}$ = 80°C/W.
Step 3. Find $P_{F(AV)}$ from Figure 4. **Read $P_{F(AV)}$ = 0.5 W

$$@\ \frac{I_{(FM)}}{I_{(AV)}} = 10 \text{ and } I_{F(AV)} = 0.5\text{ A}.$$

Step 4. Find $T_{A(max)}$ from equation (3).
$T_{A(max)}$ = 109 – (80) (0.5) = 69°C.

**Values given are for the 1N5818. Power is slightly lower for the 1N5817 because of its lower forward voltage, and higher for the 1N5819.

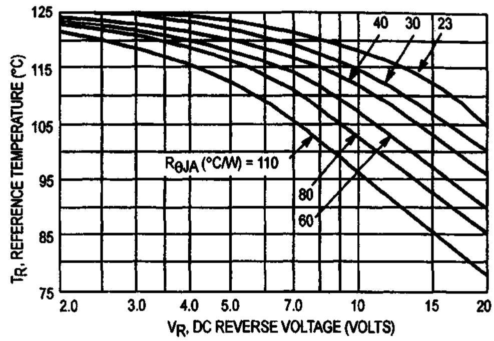


Figure 1. Maximum Reference Temperature 1N5817

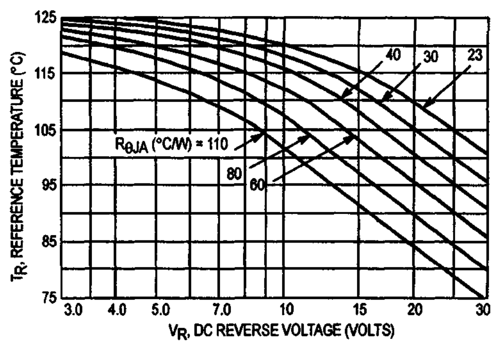


Figure 2. Maximum Reference Temperature 1N5818

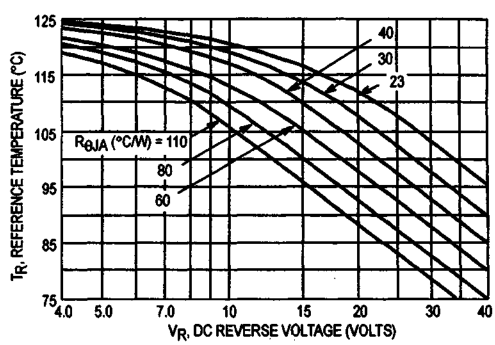


Figure 3. Maximum Reference Temperature 1N5819

Table 1. Values for Factor F

Circuit	Half Wave		Full Wave, Bridge		Full Wave, Center Tapped*†	
Load	Resistive	Capacitive*	Resistive	Capacitive	Resistive	Capacitive
Sine Wave	0.5	1.3	0.5	0.65	1.0	1.3
Square Wave	0.75	1.5	0.75	0.75	1.5	1.5

*Note that $V_{R(PK)} \approx 2.0\ V_{in(PK)}$. †Use line to center tap voltage for V_{in}.

1N5817 1N5818 1N5819

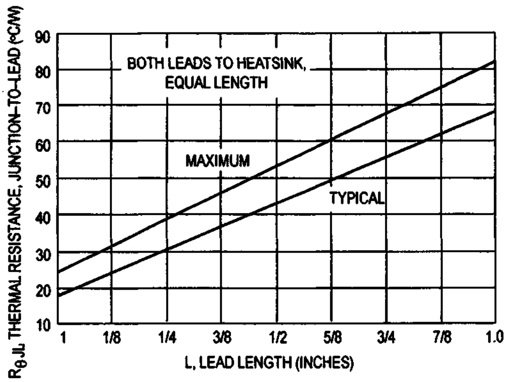


Figure 4. Steady–State Thermal Resistance

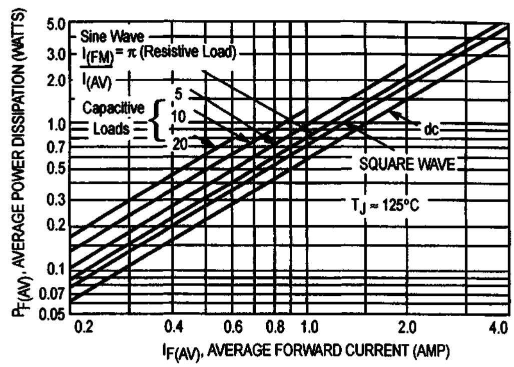


Figure 5. Forward Power Dissipation 1N5817–19

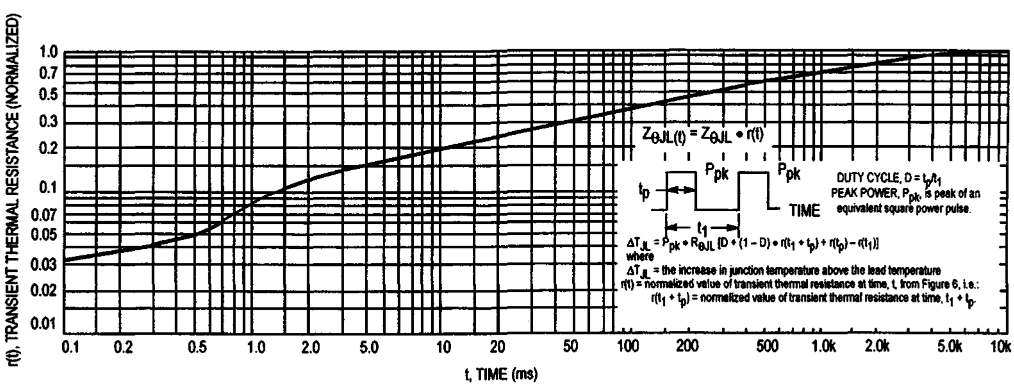


Figure 6. Thermal Response

NOTE 2 — MOUNTING DATA

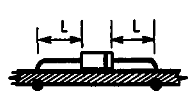
Data shown for thermal resistance junction–to–ambient ($R_{\theta JA}$) for the mountings shown are to be used as typical guideline values for preliminary engineering, or in case the tie point temperature cannot be measured.

TYPICAL VALUES FOR $R_{\theta JA}$ IN STILL AIR

Mounting Method	Lead Length, L (in)				$R_{\theta JA}$
	1/8	1/4	1/2	3/4	
1	52	65	72	85	°C/W
2	67	80	87	100	°C/W
3	50				°C/W

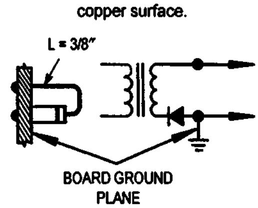
Mounting Method 1

P.C. Board with 1–1/2″ x 1–1/2″ copper surface.

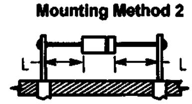


Mounting Method 3

P.C. Board with 1–1/2″ x 1–1/2″ copper surface.



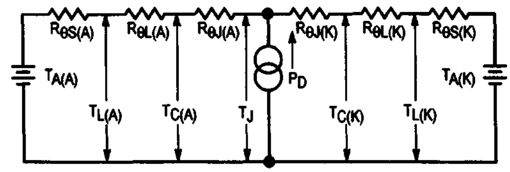
Mounting Method 2



VECTOR PIN MOUNTING

1N5817 1N5818 1N5819

NOTE 3 — THERMAL CIRCUIT MODEL
(For heat conduction through the leads)



Use of the above model permits junction to lead thermal resistance for any mounting configuration to be found. For a given total lead length, lowest values occur when one side of the rectifier is brought as close as possible to the heatsink. Terms in the model signify:

T_A = Ambient Temperature T_C = Case Temperature
T_L = Lead Temperature T_J = Junction Temperature
$R_{\theta S}$ = Thermal Resistance, Heatsink to Ambient
$R_{\theta L}$ = Thermal Resistance, Lead to Heatsink
$R_{\theta J}$ = Thermal Resistance, Junction to Case
P_D = Power Dissipation

(Subscripts A and K refer to anode and cathode sides, respectively.)
Values for thermal resistance components are:
$R_{\theta L}$ = 100°C/W/in typically and 120°C/W/in maximum
$R_{\theta J}$ = 36°C/W typically and 46°C/W maximum.

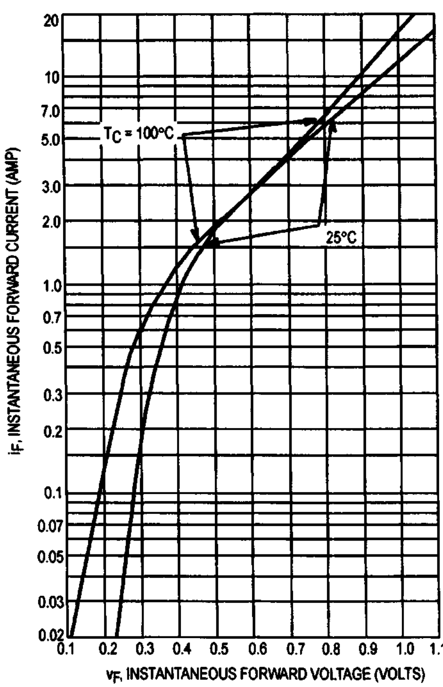


Figure 7. Typical Forward Voltage

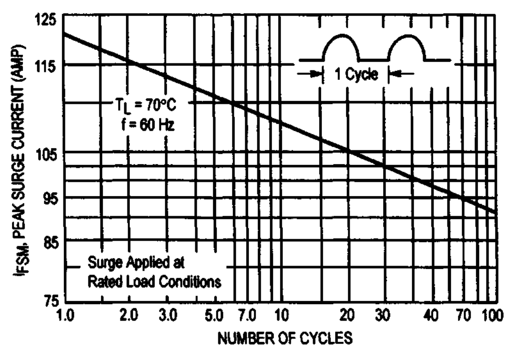


Figure 8. Maximum Nonrepetitive Surge Current

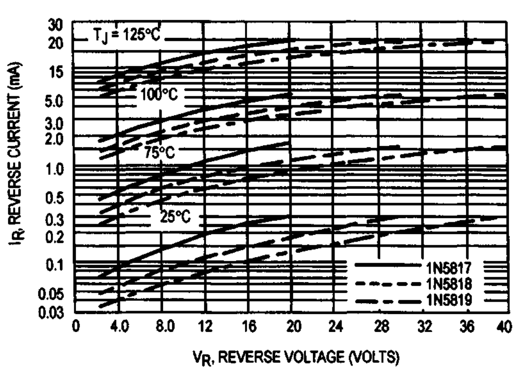


Figure 9. Typical Reverse Current

1N5817 1N5818 1N5819

NOTE 4 — HIGH FREQUENCY OPERATION

Since current flow in a Schottky rectifier is the result of majority carrier conduction, it is not subject to junction diode forward and reverse recovery transients due to minority carrier injection and stored charge. Satisfactory circuit analysis work may be performed by using a model consisting of an ideal diode in parallel with a variable capacitance. (See Figure 10.)

Rectification efficiency measurements show that operation will be satisfactory up to several megahertz. For example, relative waveform rectification efficiency is approximately 70 percent at 2.0 MHz, e.g., the ratio of dc power to RMS power in the load is 0.28 at this frequency, whereas perfect rectification would yield 0.406 for sine wave inputs. However, in contrast to ordinary junction diodes, the loss in waveform efficiency is not indicative of power loss: it is simply a result of reverse current flow through the diode capacitance, which lowers the dc output voltage.

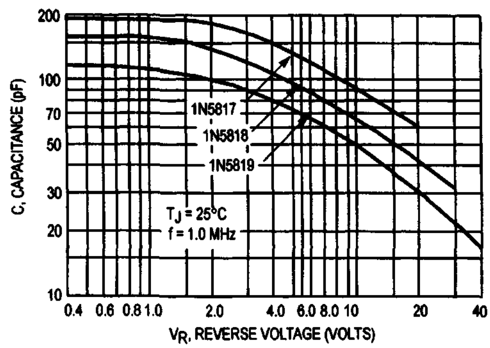
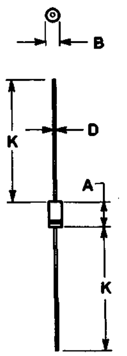


Figure 10. Typical Capacitance

1N5817 1N5818 1N5819

PACKAGE DIMENSIONS



NOTES:
1. ALL RULES AND NOTES ASSOCIATED WITH JEDEC DO–41 OUTLINE SHALL APPLY.
2. POLARITY DENOTED BY CATHODE BAND.
3. LEAD DIAMETER NOT CONTROLLED WITHIN F DIMENSION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	5.97	6.60	0.235	0.260
B	2.79	3.05	0.110	0.120
D	0.76	0.86	0.030	0.034
K	27.94	—	1.100	—

CASE 59–04
ISSUE M

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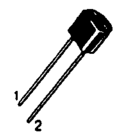
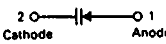
MOTOROLA

MVAM108★
MVAM109★
MVAM115★
MVAM125★

CASE 182-02, STYLE 1
(TO-226AC)





TUNING DIODES WITH VERY HIGH CAPACITANCE RATIO

★These are Motorola designated preferred devices.

SILICON TUNING DIODES

. . . designed for electronic tuning of AM receivers and high capacitance, high tuning ratio applications.

- High Capacitance Ratio — C_R = 15 (Min), MVAM108, 115, 125
- Guaranteed Diode Capacitance — C_t = 440 pF (Min) — 560 pF (Max) @ V_R = 1.0 VDc, f = 1.0 MHz, MVAM108, MVAM115, MVAM125
- Guaranteed Figure of Merit — Q = 150 (Min) @ V_R = 1.0 Vdc, f = 1.0 MHz

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Reverse Voltage	MVAM108 MVAM109 MVAM115 MVAM125	V_R	12 15 18 28	Volts
Forward Current		I_F	50	mA
Power Dissipation @ T_A = 25°C Derate above 25°C		P_D	280 2.8	mW mW/°C
Operating and Storage Junction Temperature Range		T_J, T_{stg}	−55 to +125	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted, Each Device)

Characteristic		Symbol	Min	Typ	Max	Unit
Breakdown Voltage (I_R = 10 μAdc)	 MVAM108 MVAM109 MVAM115 MVAM125	$V_{(BR)R}$	 12 15 18 28	 — — — —	 — — — —	Vdc
Reverse Current (V_R = 8.0 V) (V_R = 9.0 V) (V_R = 15 V) (V_R = 25 V)	 MVAM108 MVAM109 MVAM115 MVAM125	I_R	 — — — —	 — — — —	 100 100 100 100	nAdc
Diode Capacitance Temperatujre Coefficient (1) (V_R = 1.0 Vdc, f = 1.0 MHz, T_A = −40°C to +85°C)		TC_C	—	435	—	ppm/°C
Case Capacitance (f = 1.0 MHz, Lead Length 1/16")		C_C	—	0.18	—	pF
Diode Capacitance (2) (V_R = 1.0 Vdc, f = 1.0 MHz)	 MVAM108, 115, 125 MVAM109	C_t	 440 400	 500 460	 560 520	pF
Figure of Merit (f = 1.0 MHz, Lead Length 1/16", V_R = 1.0 Vdc)		Q	150	—	—	—
Capacitance Ratio (f = 1.0 MHz)	 MVAM108 MVAM109 MVAM115 MVAM125	 C1/C8 C1/C9 C1/C15 C1/C25	 15 12 15 15	 — — — —	 — — — —	—

NOTES:
1. The effect of increasing temperature 1.0°C, at any operating point, is equivalent to lowering the effective tuning voltage 1.25 mV. The percent change of capacitance per °C is nearly constant from −40°C to +100°C.
2. Upon request, diodes are available in matched sets. All diodes in a set can be matched for capacitance to 3% or 2.0 pF (whichever is greater) at all points along the specified tuning range.

MVAM108, MVAM109, MVAM115, MVAM125

FIGURE 1 — TYPICAL AM RADIO APPLICATION

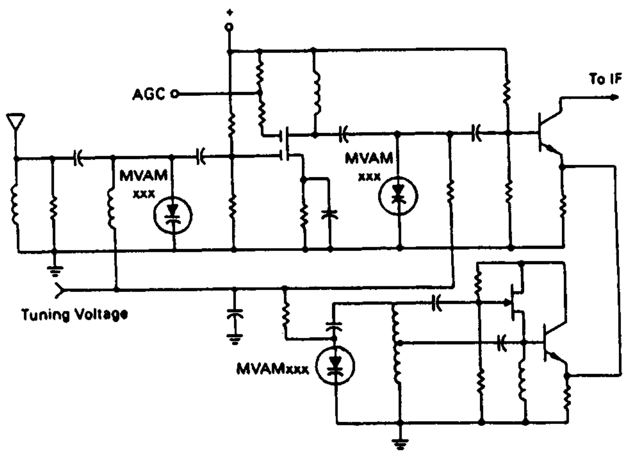


FIGURE 2 — CAPACITANCE versus REVERSE VOLTAGE

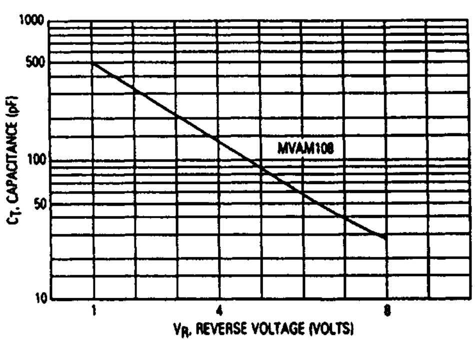


FIGURE 3 — CAPACITANCE versus REVERSE VOLTAGE

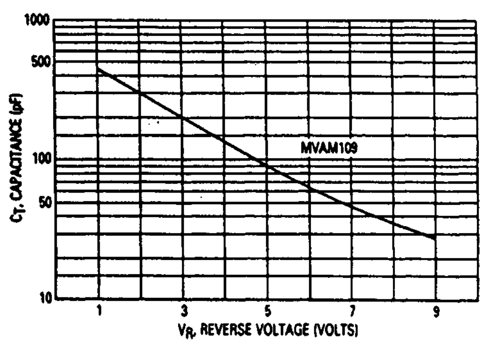


FIGURE 4 — CAPACITANCE versus REVERSE VOLTAGE

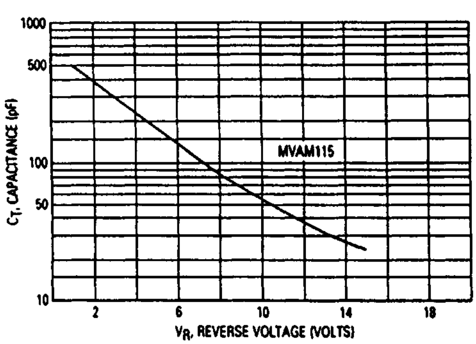
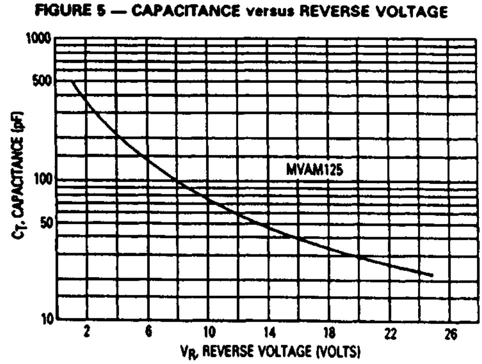


FIGURE 5 — CAPACITANCE versus REVERSE VOLTAGE



MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

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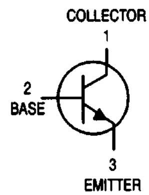
Amplifier Transistors
NPN Silicon

P2N2222A



CASE 29–04, STYLE 17
TO–92 (TO–226AA)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	40	Vdc
Collector–Base Voltage	V_{CBO}	75	Vdc
Emitter–Base Voltage	V_{EBO}	6.0	Vdc
Collector Current — Continuous	I_C	600	mAdc
Total Device Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	625 5.0	mW mW/°C
Total Device Dissipation @ $T_C = 25°C$ Derate above 25°C	P_D	1.5 12	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	83.3	°C/W

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Breakdown Voltage ($I_C = 10$ mAdc, $I_B = 0$)	$V_{(BR)CEO}$	40	—	Vdc
Collector–Base Breakdown Voltage ($I_C = 10$ μAdc, $I_E = 0$)	$V_{(BR)CBO}$	75	—	Vdc
Emitter–Base Breakdown Voltage ($I_E = 10$ μAdc, $I_C = 0$)	$V_{(BR)EBO}$	6.0	—	Vdc
Collector Cutoff Current ($V_{CE} = 60$ Vdc, $V_{EB(off)} = 3.0$ Vdc)	I_{CEX}	—	10	nAdc
Collector Cutoff Current ($V_{CB} = 60$ Vdc, $I_E = 0$) ($V_{CB} = 60$ Vdc, $I_E = 0$, $T_A = 150°C$)	I_{CBO}	 — —	 0.01 10	μAdc
Emitter Cutoff Current ($V_{EB} = 3.0$ Vdc, $I_C = 0$)	I_{EBO}	—	10	nAdc
Collector Cutoff Current ($V_{CE} = 10$ V)	I_{CEO}	—	10	nAdc
Base Cutoff Current ($V_{CE} = 60$ Vdc, $V_{EB(off)} = 3.0$ Vdc)	I_{BEX}	—	20	nAdc

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P2N2222A

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) (Continued)

Characteristic	Symbol	Min	Max	Unit
ON CHARACTERISTICS				
DC Current Gain	h_{FE}			—
(I_C = 0.1 mAdc, V_{CE} = 10 Vdc)		35	—	
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc)		50	—	
(I_C = 10 mAdc, V_{CE} = 10 Vdc)		75	—	
(I_C = 10 mAdc, V_{CE} = 10 Vdc, T_A = −55°C)		35	—	
(I_C = 150 mAdc, V_{CE} = 10 Vdc)(1)		100	300	
(I_C = 150 mAdc, V_{CE} = 1.0 Vdc)(1)		50	—	
(I_C = 500 mAdc, V_{CE} = 10 Vdc)(1)		40	—	
Collector–Emitter Saturation Voltage(1)	$V_{CE(sat)}$			Vdc
(I_C = 150 mAdc, I_B = 15 mAdc)		—	0.3	
(I_C = 500 mAdc, I_B = 50 mAdc)		—	1.0	
Base–Emitter Saturation Voltage(1)	$V_{BE(sat)}$			Vdc
(I_C = 150 mAdc, I_B = 15 mAdc)		0.6	1.2	
(I_C = 500 mAdc, I_B = 50 mAdc)		—	2.0	
SMALL–SIGNAL CHARACTERISTICS				
Current–Gain — Bandwidth Product(2) (I_C = 20 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)	f_T	300	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{obo}	—	8.0	pF
Input Capacitance (V_{EB} = 0.5 Vdc, I_C = 0, f = 1.0 MHz)	C_{ibo}	—	25	pF
Input Impedance	h_{ie}			kΩ
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		2.0	8.0	
(I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		0.25	1.25	
Voltage Feedback Ratio	h_{re}			$X\ 10^{-4}$
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		—	8.0	
(I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		—	4.0	
Small–Signal Current Gain	h_{fe}			—
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		50	300	
(I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		75	375	
Output Admittance	h_{oe}			μmhos
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		5.0	35	
(I_C = 10 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)		25	200	
Collector Base Time Constant (I_E = 20 mAdc, V_{CB} = 20 Vdc, f = 31.8 MHz)	$r_b'C_c$	—	150	ps
Noise Figure (I_C = 100 μAdc, V_{CE} = 10 Vdc, R_S = 1.0 kΩ, f = 1.0 kHz)	N_F	—	4.0	dB

SWITCHING CHARACTERISTICS

Characteristic	Conditions	Symbol	Min	Max	Unit
Delay Time	(V_{CC} = 30 Vdc, $V_{BE(off)}$ = −2.0 Vdc, I_C = 150 mAdc, I_{B1} = 15 mAdc) (Figure 1)	t_d	—	10	ns
Rise Time		t_r	—	25	ns
Storage Time	(V_{CC} = 30 Vdc, I_C = 150 mAdc, I_{B1} = I_{B2} = 15 mAdc) (Figure 2)	t_s	—	225	ns
Fall Time		t_f	—	60	ns

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
2. f_T is defined as the frequency at which $|h_{fe}|$ extrapolates to unity.

P2N2222A

SWITCHING TIME EQUIVALENT TEST CIRCUITS

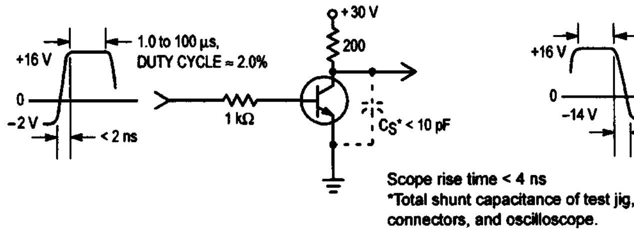


Figure 1. Turn–On Time

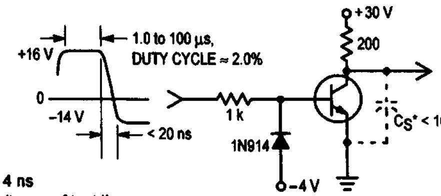


Figure 2. Turn–Off Time

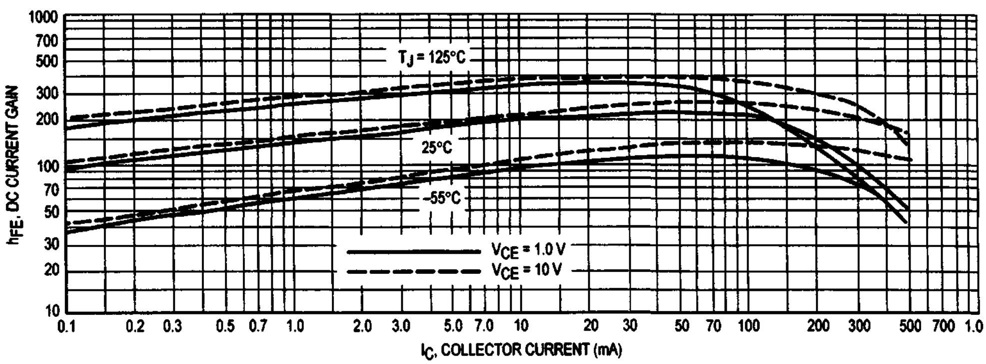


Figure 3. DC Current Gain

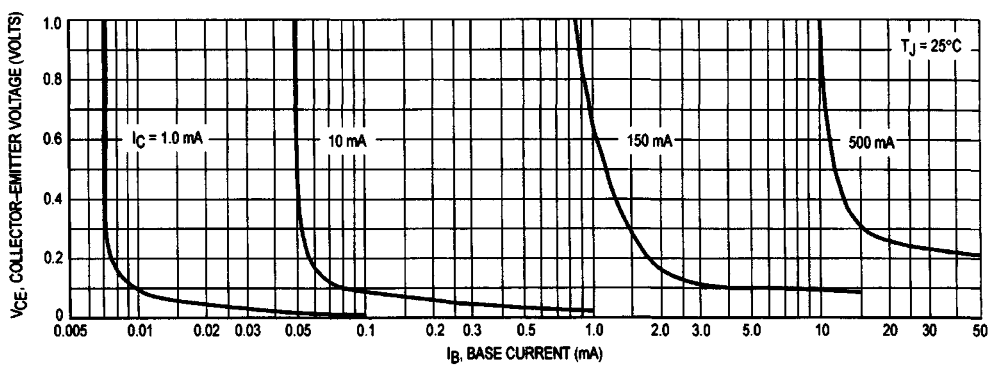


Figure 4. Collector Saturation Region

P2N2222A

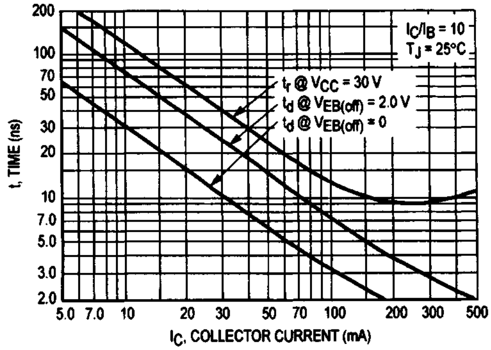


Figure 5. Turn–On Time

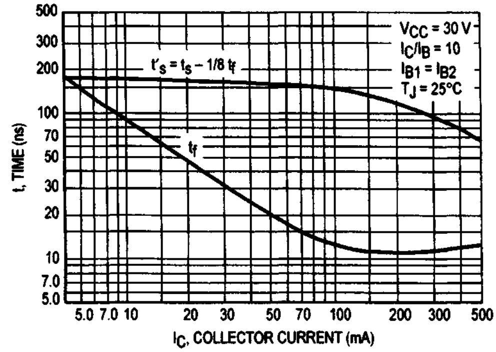


Figure 6. Turn–Off Time

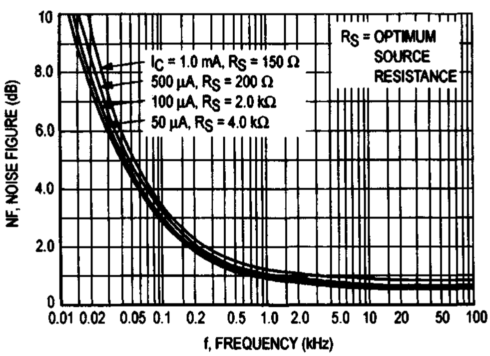


Figure 7. Frequency Effects

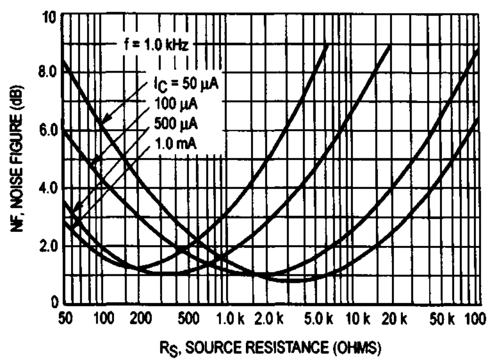


Figure 8. Source Resistance Effects

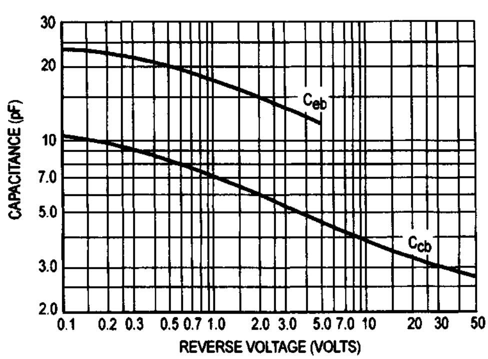


Figure 9. Capacitances

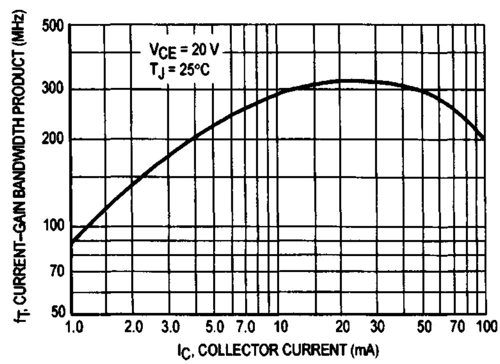


Figure 10. Current–Gain Bandwidth Product

P2N2222A

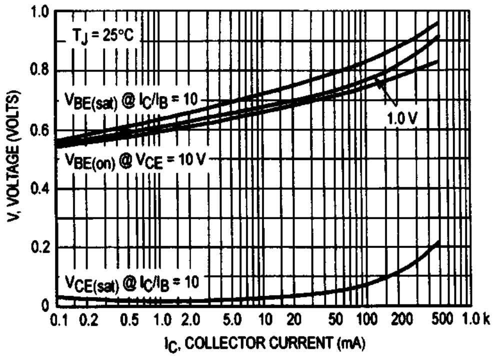


Figure 11. "On" Voltages

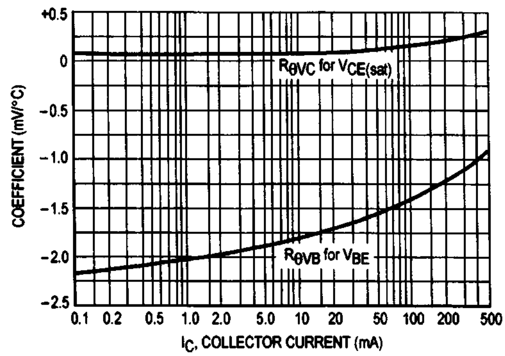
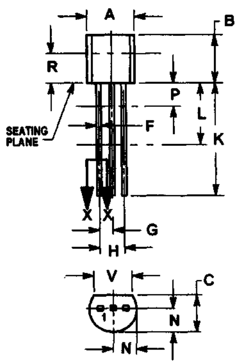
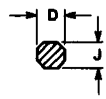


Figure 12. Temperature Coefficients

P2N2222A

PACKAGE DIMENSIONS





SECTION X–X

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. DIMENSION F APPLIES BETWEEN P AND L. DIMENSION D AND J APPLY BETWEEN L AND K MINIMUM. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.022	0.41	0.55
F	0.016	0.019	0.41	0.48
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	—	12.70	—
L	0.250	—	6.35	—
N	0.080	0.105	2.04	2.66
P	—	0.100	—	2.54
R	0.115	—	2.93	—
V	0.135	—	3.43	—

CASE 029–04
(TO–226AA)
ISSUE AD

STYLE 17:
PIN 1. COLLECTOR
2. BASE
3. EMITTER

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MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

2N3553

The RF Line

NPN SILICON HIGH-FREQUENCY TRANSISTOR

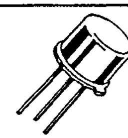
. . . designed for amplifier and oscillator applications in military and industrial equipment. Suitable for use as output, driver or pre-driver stages in VHF equipment.

- Specified 175 MHz, 28 Vdc Characteristics —
  Output Power = 2.5 Watts
  Minimum Gain = 10 dB
  Efficiency = 50%

2.5 W — 175 MHz

HIGH FREQUENCY TRANSISTOR

NPN SILICON

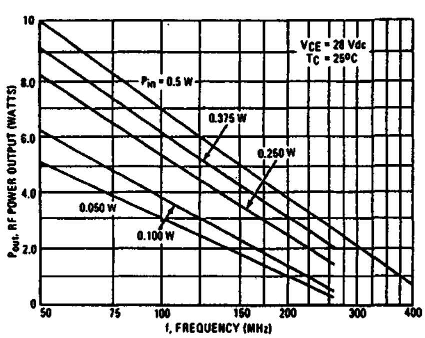


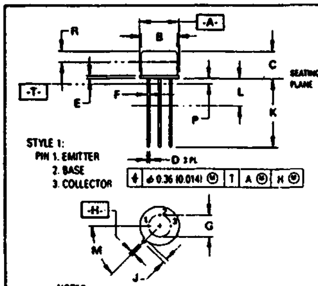
***MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	40	Vdc
Collector-Base Voltage	V_{CB}	65	Vdc
Emitter-Base Voltage	V_{EB}	4.0	Vdc
Collector Current	I_C	1.0	Adc
Total Device Dissipation @ $T_C = 25^\circ C$ Derate above $25^\circ C$	P_D	7.0 40	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +200	°C

*Indicates JEDEC Registered Data.

FIGURE 1 — OUTPUT POWER versus FREQUENCY





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION J MEASURED FROM DIMENSION A MAXIMUM.
4. DIMENSION B SHALL NOT VARY MORE THAN 0.25 (0.010) IN ZONE R. THIS ZONE CONTROLLED FOR AUTOMATIC HANDLING.
5. DIMENSION F APPLIES BETWEEN DIMENSION P AND L. DIMENSION D APPLIES BETWEEN DIMENSION L AND K MINIMUM. LEAD DIAMETER IS UNCONTROLLED IN DIMENSION P AND BEYOND DIMENSION K MINIMUM.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	8.51	9.39	0.335	0.370
B	7.75	8.50	0.305	0.335
C	6.10	6.60	0.240	0.260
D	0.41	0.53	0.016	0.021
E	0.23	1.04	0.009	0.041
F	0.41	0.48	0.016	0.019
G	5.08 BSC		0.200 BSC	
H	0.72	0.86	0.028	0.034
J	0.74	1.14	0.029	0.045
K	12.70	19.05	0.500	0.750
L	6.35	—	0.250	—
M	45° BSC		45° BSC	
P	—	1.27	—	0.050
R	2.54	—	0.100	—

CASE 79-04
TO-205AD
(TO-39)

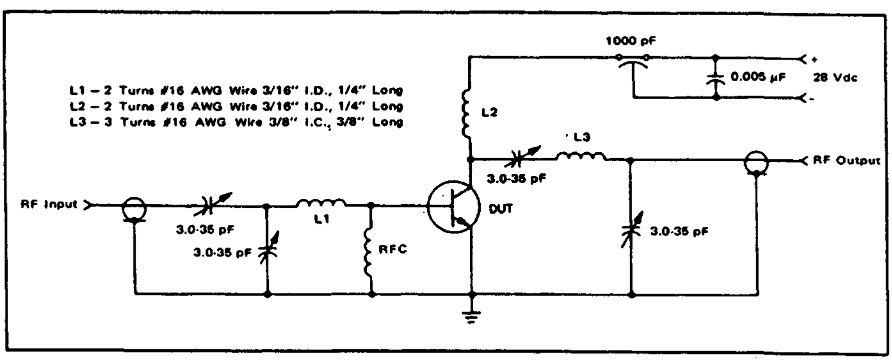
2N3553

*ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector-Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	40	–	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 0.1 mAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	–	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0)	I_{CEO}	–	–	0.1	mAdc
Collector Cutoff Current (V_{CE} = 30 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 200°C) (V_{CE} = 65 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEX}	– –	– –	5.0 1.0	mAdc
Emitter Cutoff Current (V_{BE} = 4.0 Vdc, I_C = 0)	I_{EBO}	–	–	0.1	mAdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 250 mAdc, V_{CE} = 5.0 Vdc)	h_{FE}	10	–	–	–
Collector-Emitter Saturation Voltage (I_C = 250 mAdc, I_B = 50 mAdc)	$V_{CE(sat)}$	–	–	1.0	Vdc
DYNAMIC CHARACTERISTICS					
Current-Gain—Bandwidth Product (I_C = 100 mAdc, V_{CE} = 28 Vdc, f = 100 MHz)	f_T	–	500	–	MHz
Output Capacitance (V_{CB} = 30 Vdc, I_E = 0, f = 100 kHz)	C_{ob}	–	8.0	10	pF
FUNCTIONAL TESTS					
Power Input (V_{CE} = 28 Vdc, P_{out} = 2.5 Watts, f = 175 MHz)	P_{in}	–	–	0.25	Watt
Common-Emitter Amplifier Power Gain (V_{CE} = 28 Vdc, P_{out} = 2.5 Watts, f = 175 MHz)	G_{pe}	10	–	–	dB
Collector Efficiency (V_{CE} = 28 Vdc, P_{out} = 2.5 Watts, f = 175 MHz)	η	50	–	–	%

*Indicates JEDEC Registered Data
(1) Pulsed thru a 25 mH inductor.

FIGURE 2 – 175 MHz TEST CIRCUIT SCHEMATIC



MOTOROLA
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General Purpose Transistors

PNP Silicon

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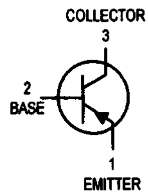
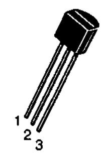
*Motorola Preferred Device





CASE 29–04, STYLE 1
TO–92 (TO–226AA)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	40	Vdc
Collector–Base Voltage	V_{CBO}	40	Vdc
Emitter–Base Voltage	V_{EBO}	5.0	Vdc
Collector Current — Continuous	I_C	200	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	625 5.0	mW mW/°C
Total Power Dissipation @ T_A = 60°C	P_D	250	mW
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	1.5 12	Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–55 to +150	°C

THERMAL CHARACTERISTICS(1)

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	83.3	°C/W

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Breakdown Voltage (2) (I_C = 1.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	40	—	Vdc
Collector–Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0)	$V_{(BR)CBO}$	40	—	Vdc
Emitter–Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	$V_{(BR)EBO}$	5.0	—	Vdc
Base Cutoff Current (V_{CE} = 30 Vdc, V_{EB} = 3.0 Vdc)	I_{BL}	—	50	nAdc
Collector Cutoff Current (V_{CE} = 30 Vdc, V_{EB} = 3.0 Vdc)	I_{CEX}	—	50	nAdc

1. Indicates Data in addition to JEDEC Requirements.
2. Pulse Test: Pulse Width ≤ 300 μs; Duty Cycle ≤ 2.0%.

Preferred devices are Motorola recommended choices for future use and best overall value.

REV 2

MOTOROLA

2N3905 2N3906

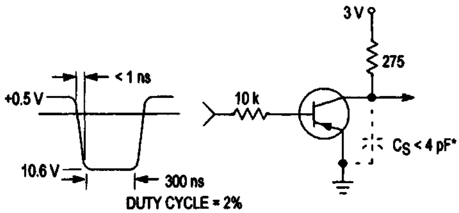
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) (Continued)

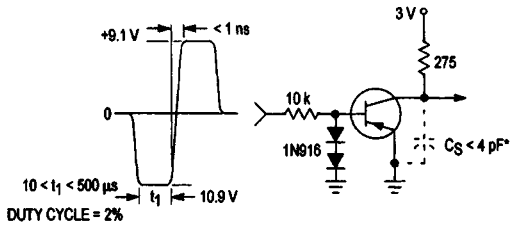
Characteristic		Symbol	Min	Max	Unit
ON CHARACTERISTICS[1]					
DC Current Gain		h_{FE}			—
(I_C = 0.1 mAdc, V_{CE} = 1.0 Vdc)	2N3905		30	—	
	2N3906		60	—	
(I_C = 1.0 mAdc, V_{CE} = 1.0 Vdc)	2N3905		40	—	
	2N3906		80	—	
(I_C = 10 mAdc, V_{CE} = 1.0 Vdc)	2N3905		50	150	
	2N3906		100	300	
(I_C = 50 mAdc, V_{CE} = 1.0 Vdc)	2N3905		30	—	
	2N3906		60	—	
(I_C = 100 mAdc, V_{CE} = 1.0 Vdc)	2N3905		15	—	
	2N3906		30	—	
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 10 mAdc, I_B = 1.0 mAdc)			—	0.25	
(I_C = 50 mAdc, I_B = 5.0 mAdc			—	0.4	
Base–Emitter Saturation Voltage		$V_{BE(sat)}$			Vdc
(I_C = 10 mAdc, I_B = 1.0 mAdc)			0.65	0.85	
(I_C = 50 mAdc, I_B = 5.0 mAdc)			—	0.95	
SMALL–SIGNAL CHARACTERISTICS					
Current–Gain — Bandwidth Product		f_T			MHz
(I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)	2N3905		200	—	
	2N3906		250	—	
Output Capacitance (V_{CB} = 5.0 Vdc, I_E = 0, f = 1.0 MHz)		C_{obo}	—	4.5	pF
Input Capacitance (V_{EB} = 0.5 Vdc, I_C = 0, f = 1.0 MHz)		C_{ibo}	—	10.0	pF
Input Impedance		h_{ie}			kΩ
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N3905		0.5	8.0	
	2N3906		2.0	12	
Voltage Feedback Ratio		h_{re}			X 10^{-4}
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N3905		0.1	5.0	
	2N3906		0.1	10	
Small–Signal Current Gain		h_{fe}			—
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N3905		50	200	
	2N3906		100	400	
Output Admittance		h_{oe}			µmhos
(I_C = 1.0 mAdc, V_{CE} = 10 Vdc, f = 1.0 kHz)	2N3905		1.0	40	
	2N3906		3.0	60	
Noise Figure		NF			dB
(I_C = 100 µAdc, V_{CE} = 5.0 Vdc, R_S = 1.0 k Ω, f = 1.0 kHz)	2N3905		—	5.0	
	2N3906		—	4.0	

SWITCHING CHARACTERISTICS

Characteristic	Conditions		Symbol	Min	Max	Unit
Delay Time	(V_{CC} = 3.0 Vdc, V_{BE} = 0.5 Vdc, I_C = 10 mAdc, I_{B1} = 1.0 mAdc)		t_d	—	35	ns
Rise Time			t_r	—	35	ns
Storage Time	(V_{CC} = 3.0 Vdc, I_C = 10 mAdc, I_{B1} = I_{B2} = 1.0 mAd	2N3905	t_s	—	200	ns
		2N3906		—	225	
Fall Time		2N3905	t_f	—	60	ns
		2N3906		—	75	

1. Pulse Test: Pulse Width ≤ 300 µs; Duty Cycle ≤ 2.0%.





* Total shunt capacitance of test jig and connectors

Figure 1. Delay and Rise Time Equivalent Test Circuit

Figure 2. Storage and Fall Time Equivalent Test Circuit

TYPICAL TRANSIENT CHARACTERISTICS

T_J = 25°C
T_J = 125°C

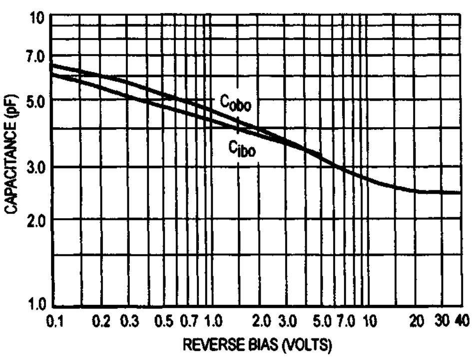


Figure 3. Capacitance

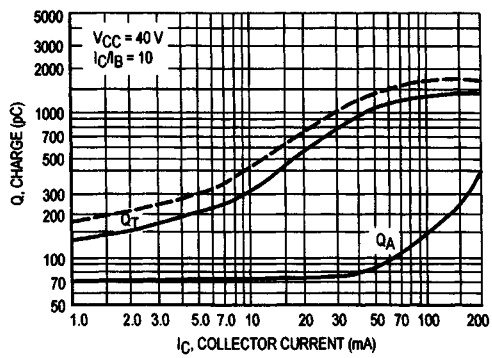


Figure 4. Charge Data

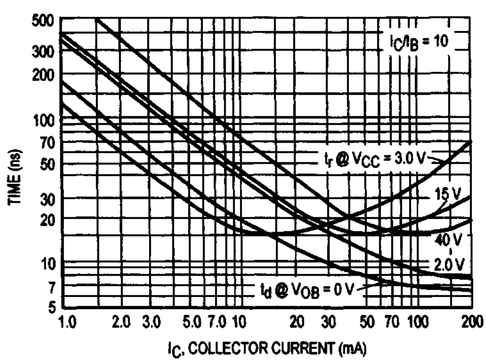


Figure 5. Turn–On Time

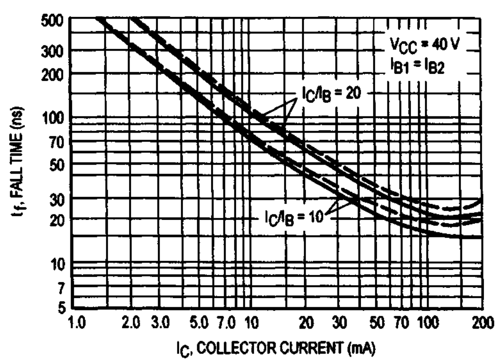


Figure 6. Fall Time

2N3905 2N3906

TYPICAL AUDIO SMALL–SIGNAL CHARACTERISTICS
NOISE FIGURE VARIATIONS

(V_{CE} = –5.0 Vdc, T_A = 25°C, Bandwidth = 1.0 Hz)

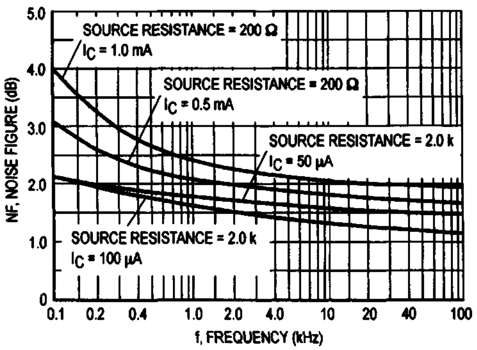


Figure 7.

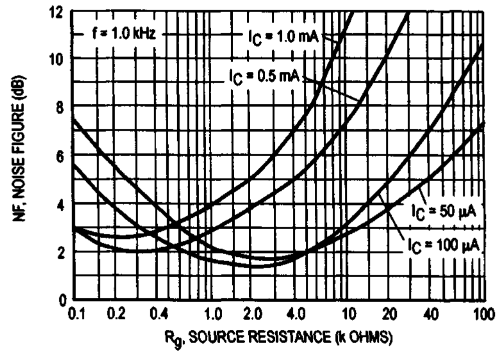


Figure 8.

h PARAMETERS

(V_{CE} = –10 Vdc, f = 1.0 kHz, T_A = 25°C)

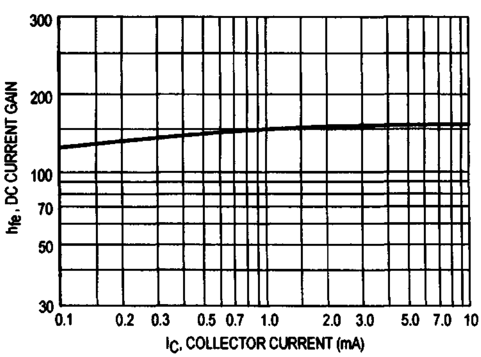


Figure 9. Current Gain

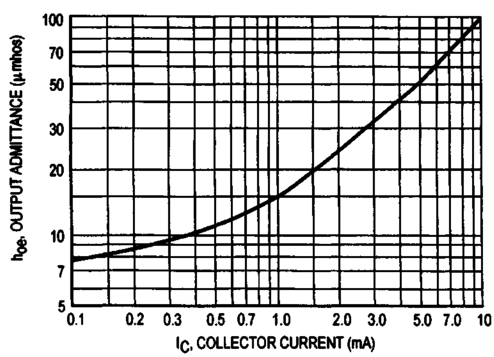


Figure 10. Output Admittance

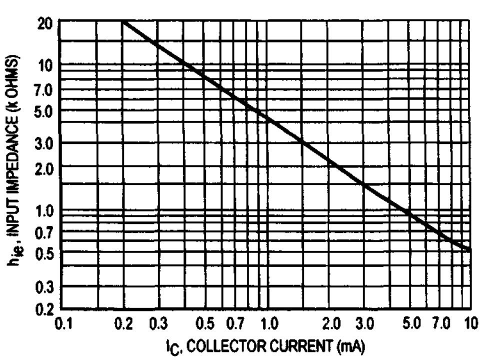


Figure 11. Input Impedance

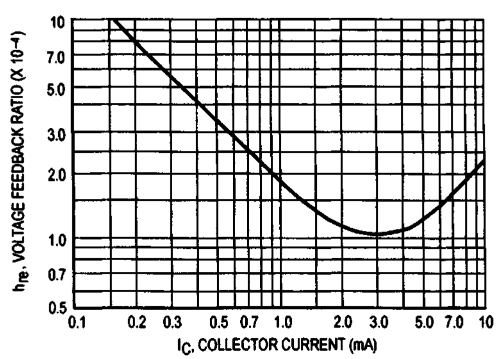


Figure 12. Voltage Feedback Ratio

2N3905 2N3906

TYPICAL STATIC CHARACTERISTICS

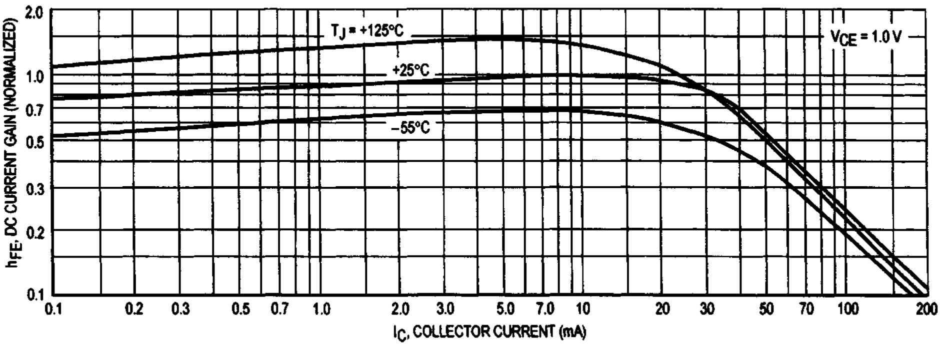


Figure 13. DC Current Gain

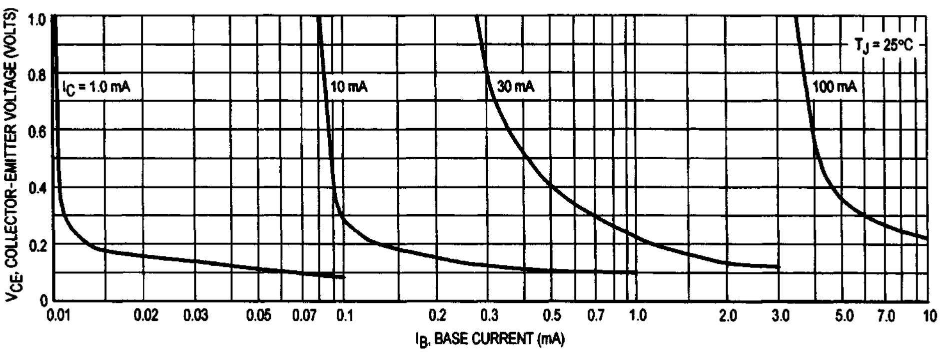


Figure 14. Collector Saturation Region

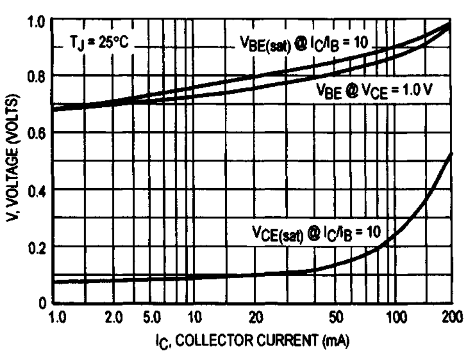


Figure 15. "ON" Voltages

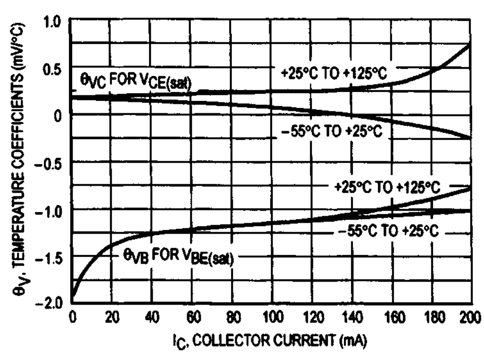
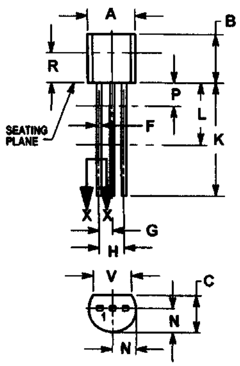
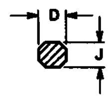


Figure 16. Temperature Coefficients

2N3905 2N3906

PACKAGE DIMENSIONS





SECTION X–X

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. DIMENSION F APPLIES BETWEEN P AND L. DIMENSION D AND J APPLY BETWEEN L AND K MINIMUM. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.022	0.41	0.55
F	0.016	0.019	0.41	0.48
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	—	12.70	—
L	0.250	—	6.35	—
N	0.080	0.105	2.04	2.66
P	—	0.100	—	2.54
R	0.115	—	2.93	—
V	0.135	—	3.43	—

CASE 029–04
(TO–226AA)
ISSUE AD

STYLE 1:
PIN 1. EMITTER
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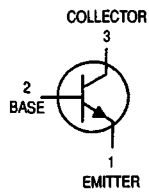
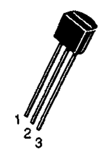




CASE 29–04, STYLE 1
TO–92 (TO–226AA)

MAXIMUM RATINGS

Rating	Symbol	2N4123	2N4124	Unit
Collector–Emitter Voltage	V_{CEO}	30	25	Vdc
Collector–Base Voltage	V_{CBO}	40	30	Vdc
Emitter–Base Voltage	V_{EBO}	5.0		Vdc
Collector Current — Continuous	I_C	200		mAdc
Total Device Dissipation @ $T_A = 25°C$ Derate above 25°C	P_D	625 5.0		mW mW/°C
Total Device Dissipation @ $T_C = 25°C$ Derate above 25°C	P_D	1.5 12		Watts mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−55 to +150		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	200	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	83.3	°C/W

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage[1] ($I_C = 1.0$ mAdc, $I_E = 0$)	 2N4123 2N4124	$V_{(BR)CEO}$	 30 25	 — —	Vdc
Collector–Base Breakdown Voltage ($I_C = 10$ μAdc, $I_E = 0$)	 2N4123 2N4124	$V_{(BR)CBO}$	 40 30	 — —	Vdc
Emitter–Base Breakdown Voltage ($I_E = 10$ μAdc, $I_C = 0$)		$V_{(BR)EBO}$	5.0	—	Vdc
Collector Cutoff Current ($V_{CB} = 20$ Vdc, $I_E = 0$)		I_{CBO}	—	50	nAdc
Emitter Cutoff Current ($V_{EB} = 3.0$ Vdc, $I_C = 0$)		I_{EBO}	—	50	nAdc

1. Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%.

MOTOROLA

2N4123 2N4124

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) (Continued)

Characteristic		Symbol	Min	Max	Unit
ON CHARACTERISTICS					
DC Current Gain(1)		h_{FE}			—
(I_C = 2.0 mAdc, V_{CE} = 1.0 Vdc)	2N4123		50	150	
	2N4124		120	360	
(I_C = 50 mAdc, V_{CE} = 1.0 Vdc)	2N4123		25	—	
	2N4124		60	—	
Collector–Emitter Saturation Voltage(1) (I_C = 50 mAdc, I_B = 5.0 mAdc)		$V_{CE(sat)}$	—	0.3	Vdc
Base–Emitter Saturation Voltage(1) (I_C = 50 mAdc, I_B = 5.0 mAdc)		$V_{BE(sat)}$	—	0.95	Vdc
SMALL–SIGNAL CHARACTERISTICS					
Current–Gain — Bandwidth Product		f_T			MHz
(I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)	2N4123		250	—	
	2N4124		300	—	
Input Capacitance (V_{EB} = 0.5 Vdc, I_C = 0, f = 1.0 MHz)		C_{ibo}	—	8.0	pF
Collector–Base Capacitance (I_E = 0, V_{CB} = 5.0 V, f = 1.0 MHz)		C_{cb}	—	4.0	pF
Small–Signal Current Gain		h_{fe}			—
(I_C = 2.0 mAdc, V_{CE} = 10 Vdc, R_S = 10 k ohm, f = 1.0 kHz)	2N4123		50	200	
	2N4124		120	480	
Current Gain — High Frequency		$\|h_{fe}\|$			—
(I_C = 10 mAdc, V_{CE} = 20 Vdc, f = 100 MHz)	2N4123		2.5	—	
	2N4124		3.0	—	
(I_C = 2.0 mAdc, V_{CE} = 10 V, f = 1.0 kHz)	2N4123		50	200	
(I_C = 2.0 mAdc, V_{CE} = 10 V, f = 1.0 kHz)	2N4124		120	480	
Noise Figure		NF			dB
(I_C = 100 μAdc, V_{CE} = 5.0 Vdc, R_S = 1.0 k ohm,	2N4123		—	6.0	
f = 1.0 kHz)	2N4124		—	5.0	

1. Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%.

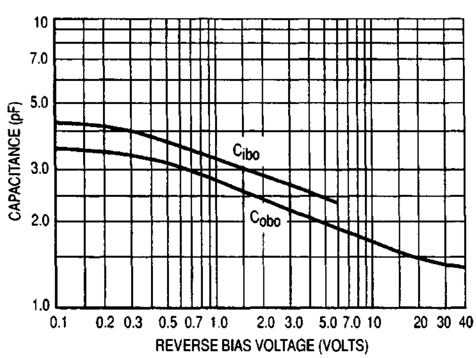


Figure 1. Capacitance

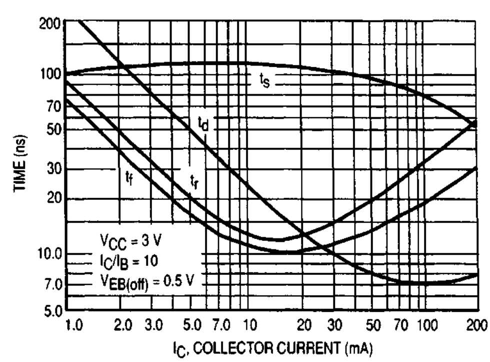


Figure 2. Switching Times

2N4123 2N4124

AUDIO SMALL–SIGNAL CHARACTERISTICS

NOISE FIGURE

(V_{CE} = 5 Vdc, T_A = 25°C)
Bandwidth = 1.0 Hz

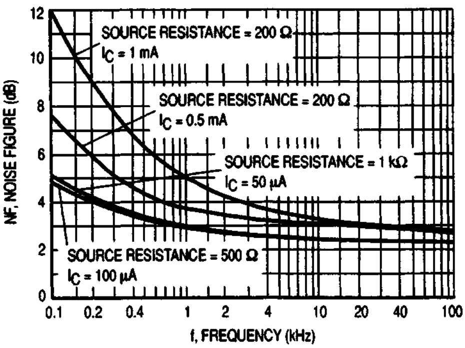


Figure 3. Frequency Variations

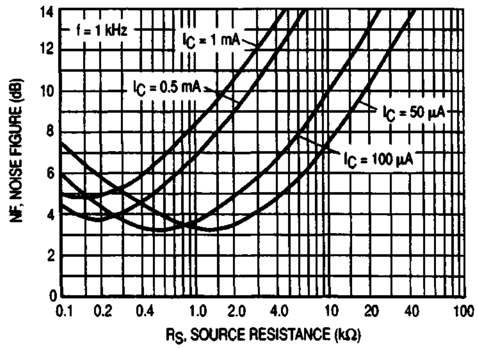


Figure 4. Source Resistance

h PARAMETERS

(V_{CE} = 10 V, f = 1 kHz, T_A = 25°C)

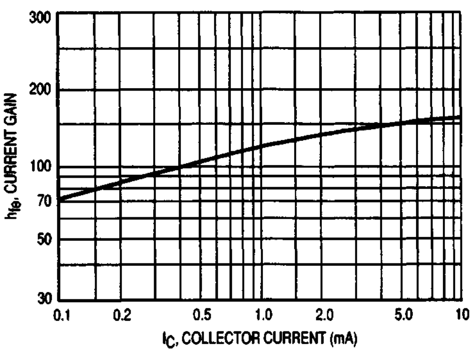


Figure 5. Current Gain

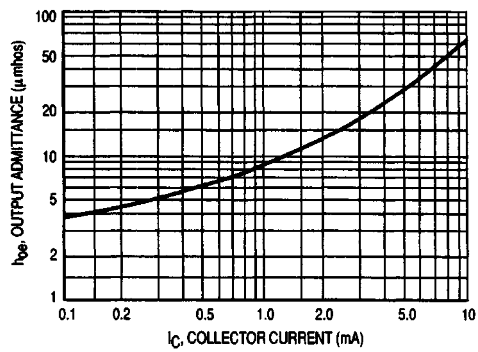


Figure 6. Output Admittance

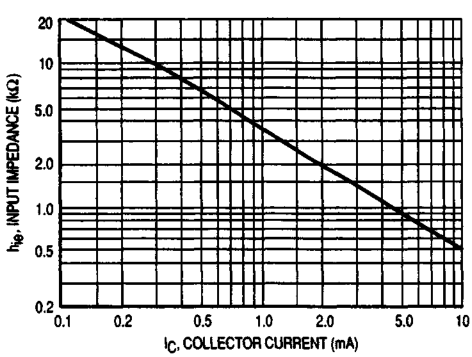


Figure 7. Input Impedance

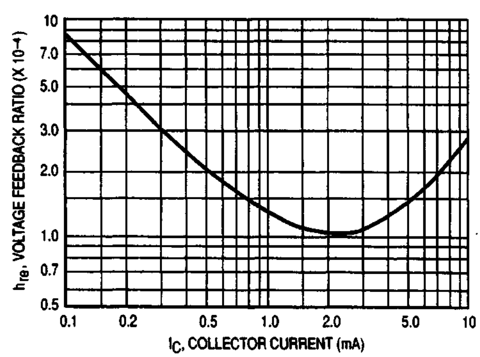


Figure 8. Voltage Feedback Ratio

2N4123 2N4124

STATIC CHARACTERISTICS

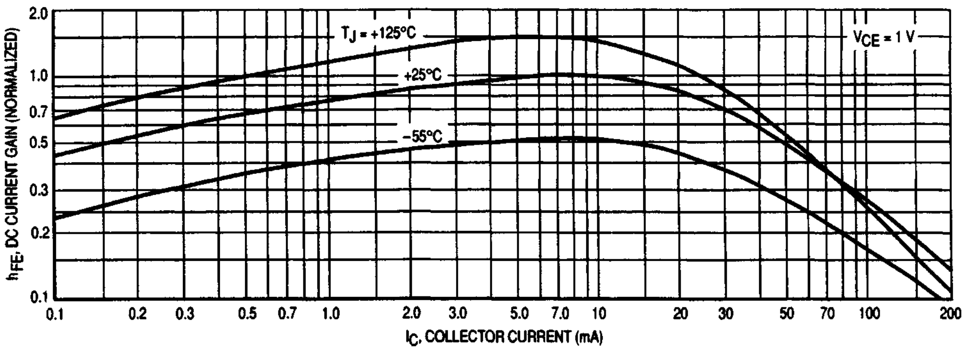


Figure 9. DC Current Gain

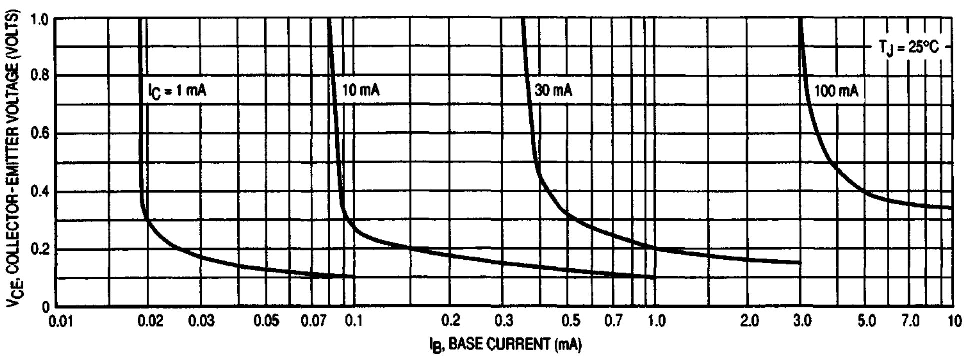


Figure 10. Collector Saturation Region

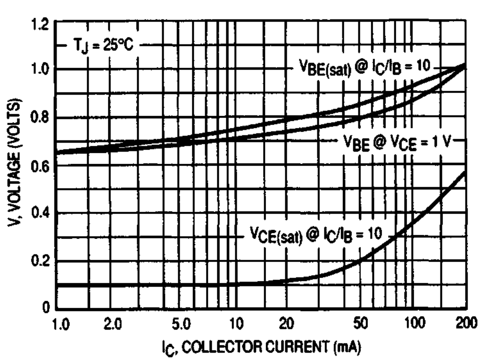


Figure 11. "On" Voltages

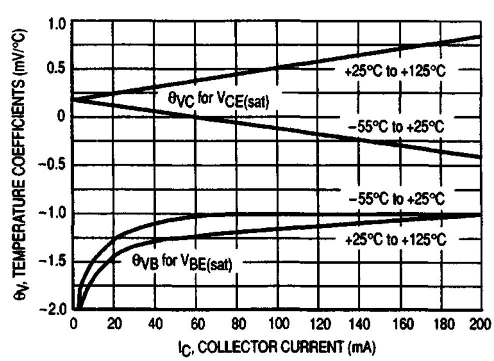
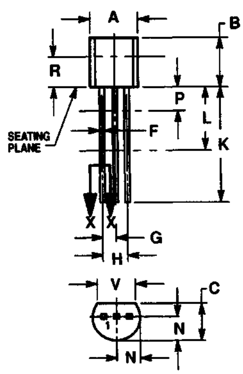
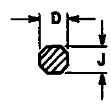


Figure 12. Temperature Coefficients

2N4123 2N4124

PACKAGE DIMENSIONS





SECTION X–X

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. DIMENSION F APPLIES BETWEEN P AND L. DIMENSION D AND J APPLY BETWEEN L AND K MINIMUM. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.022	0.41	0.55
F	0.016	0.019	0.41	0.48
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	—	12.70	—
L	0.250	—	6.35	—
N	0.080	0.105	2.04	2.66
P	—	0.100	—	2.54
R	0.115	—	2.93	—
V	0.135	—	3.43	—

CASE 029–04
(TO–226AA)
ISSUE AD

STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

2N4123 2N4124

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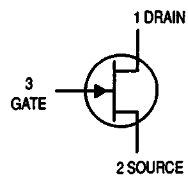
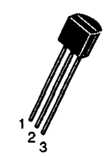


J308
J309
J310

Motorola Preferred Devices



CASE 29–04, STYLE 5
TO–92 (TO–226AA)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DS}	25	Vdc
Gate–Source Voltage	V_{GS}	25	Vdc
Forward Gate Current	I_{GF}	10	mAdc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D	350 2.8	mW mW/°C
Junction Temperature Range	T_J	–65 to +125	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Gate–Source Breakdown Voltage (I_G = –1.0 µAdc, V_{DS} = 0)		$V_{(BR)GSS}$	–25	—	—	Vdc
Gate Reverse Current (V_{GS} = –15 Vdc, V_{DS} = 0, T_A = 25°C) (V_{GS} = –15 Vdc, V_{DS} = 0, T_A = +125°C)		I_{GSS}	 — —	 — —	 –1.0 –1.0	 nAdc µAdc
Gate Source Cutoff Voltage (V_{DS} = 10 Vdc, I_D = 1.0 nAdc)	 J308 J309 J310	$V_{GS(off)}$	 –1.0 –1.0 –2.0	 — — —	 –6.5 –4.0 –6.5	Vdc
ON CHARACTERISTICS						
Zero–Gate–Voltage Drain Current(1) (V_{DS} = 10 Vdc, V_{GS} = 0)	 J308 J309 J310	I_{DSS}	 12 12 24	 — — —	 60 30 60	mAdc
Gate–Source Forward Voltage (V_{DS} = 0, I_G = 1.0 mAdc)		$V_{GS(f)}$	—	—	1.0	Vdc
SMALL–SIGNAL CHARACTERISTICS						
Common–Source Input Conductance (V_{DS} = 10 Vdc, I_D = 10 mAdc, f = 100 MHz)	 J308 J309 J310	$Re(y_{is})$	 — — —	 0.7 0.7 0.5	 — — —	mmhos
Common–Source Output Conductance (V_{DS} = 10 Vdc, I_D = 10 mAdc, f = 100 MHz)		$Re(y_{os})$	—	0.25	—	mmhos
Common–Gate Power Gain (V_{DS} = 10 Vdc, I_D = 10 mAdc, f = 100 MHz)		G_{pg}	—	16	—	dB

1. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 3.0%.

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J308 J309 J310

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) (Continued)

Characteristic		Symbol	Min	Typ	Max	Unit
SMALL–SIGNAL CHARACTERISTICS (continued)						
Common–Source Forward Transconductance (V_{DS} = 10 Vdc, I_D = 10 mAdc, f = 100 MHz)		$Re(y_{fs})$	—	12	—	mmhos
Common–Gate Input Conductance (V_{DS} = 10 Vdc, I_D = 10 mAdc, f = 100 MHz)		$Re(y_{ig})$	—	12	—	mmhos
Common–Source Forward Transconductance (V_{DS} = 10 Vdc, I_D = 10 mAdc, f = 1.0 kHz)	J308	g_{fs}	8000	—	20000	µmhos
	J309		10000	—	20000	
	J310		8000	—	18000	
Common–Source Output Conductance (V_{DS} = 10 Vdc, I_D = 10 mAdc, f = 1.0 kHz)		g_{os}	—	—	250	µmhos
Common–Gate Forward Transconductance (V_{DS} = 10 Vdc, I_D = 10 mAdc, f = 1.0 kHz)	J308	g_{fg}	—	13000	—	µmhos
	J309		—	13000	—	
	J310		—	12000	—	
Common–Gate Output Conductance (V_{DS} = 10 Vdc, I_D = 10 mAdc, f = 1.0 kHz)	J308	g_{og}	—	150	—	µmhos
	J309		—	100	—	
	J310		—	150	—	
Gate–Drain Capacitance (V_{DS} = 0, V_{GS} = −10 Vdc, f = 1.0 MHz)		C_{gd}	—	1.8	2.5	pF
Gate–Source Capacitance (V_{DS} = 0, V_{GS} = −10 Vdc, f = 1.0 MHz)		C_{gs}	—	4.3	5.0	pF
FUNCTIONAL CHARACTERISTICS						
Noise Figure (V_{DS} = 10 Vdc, I_D = 10 mAdc, f = 450 MHz)		NF	—	1.5	—	dB
Equivalent Short–Circuit Input Noise Voltage (V_{DS} = 10 Vdc, I_D = 10 mAdc, f = 100 Hz)		$\bar{e}_n$	—	10	—	$nV/\sqrt{Hz}$

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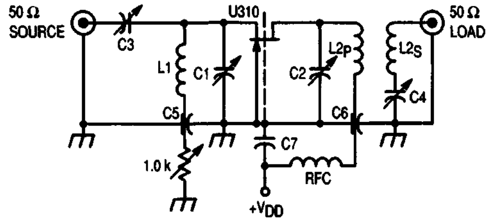

C1 = C2 = 0.8 – 10 pF, JFD #MVM010W.
C3 = C4 = 8.35 pF Erie #539–002D.
C5 = C6 = 5000 pF Erie (2443–000).
C7 = 1000 pF, Allen Bradley #FA5C.
RFC = 0.33 μH Miller #9230–30.
L1 = One Turn #16 Cu, 1/4″ I.D. (Air Core).
L2p = One Turn #16 Cu, 1/4″ I.D. (Air Core).
L2S = One Turn #16 Cu, 1/4″ I.D. (Air Core).

Figure 1. 450 MHz Common–Gate Amplifier Test Circuit

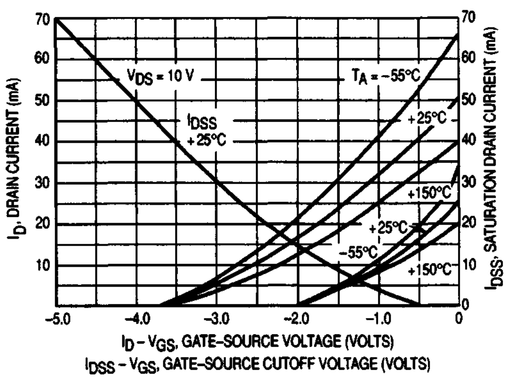

Figure 2. Drain Current and Transfer Characteristics versus Gate–Source Voltage

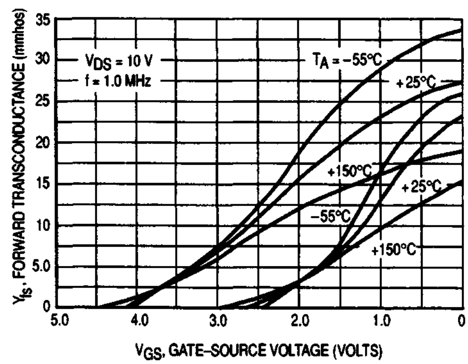

Figure 3. Forward Transconductance versus Gate–Source Voltage

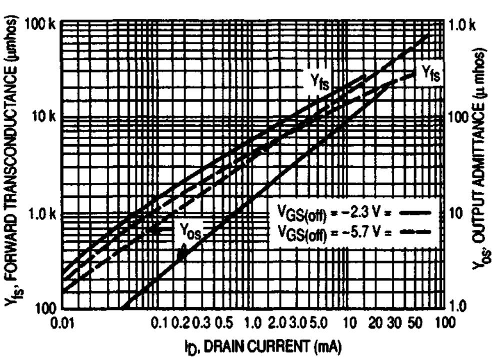

Figure 4. Common–Source Output Admittance and Forward Transconductance versus Drain Current

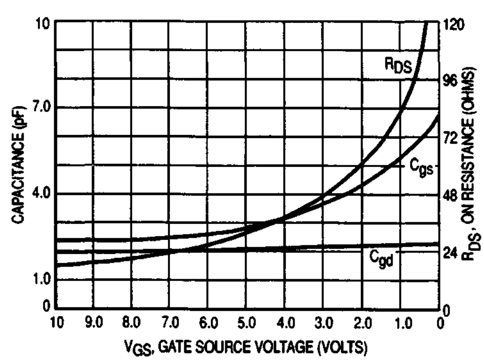

Figure 5. On Resistance and Junction Capacitance versus Gate–Source Voltage

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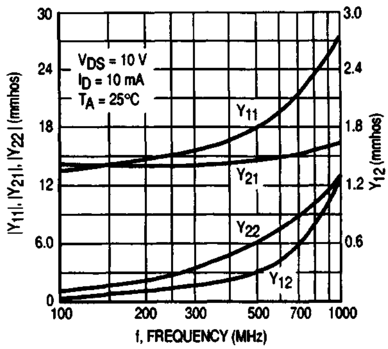


Figure 6. Common–Gate Y Parameter Magnitude versus Frequency

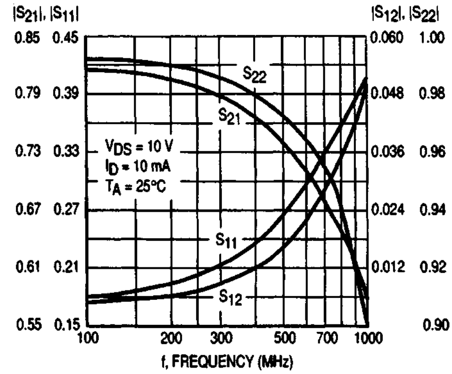


Figure 7. Common–Gate S Parameter Magnitude versus Frequency

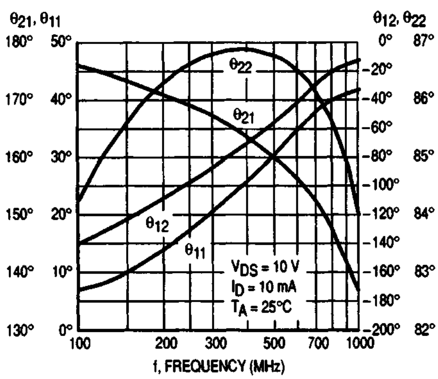


Figure 8. Common–Gate Y Parameter Phase–Angle versus Frequency

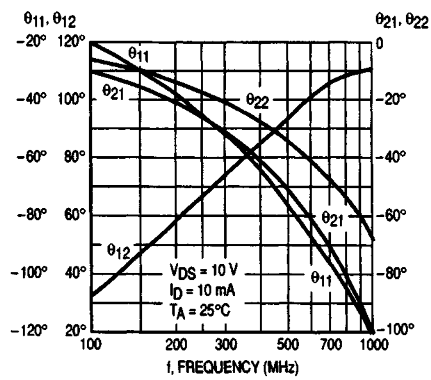


Figure 9. S Parameter Phase–Angle versus Frequency

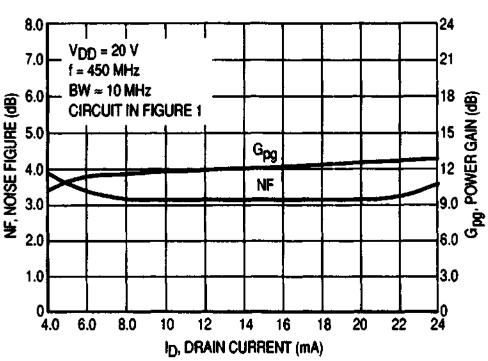


Figure 10. Noise Figure and Power Gain versus Drain Current

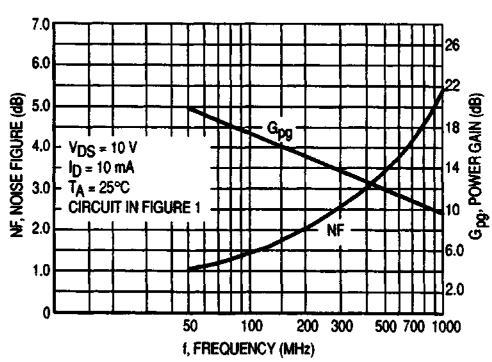
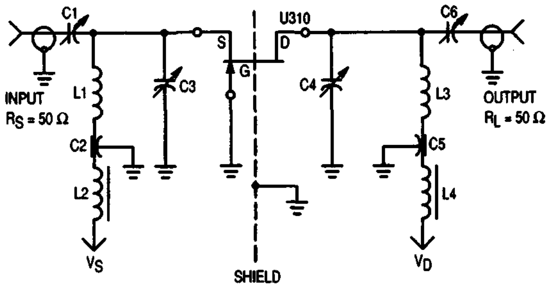


Figure 11. Noise Figure and Power Gain versus Frequency

J308 J309 J310



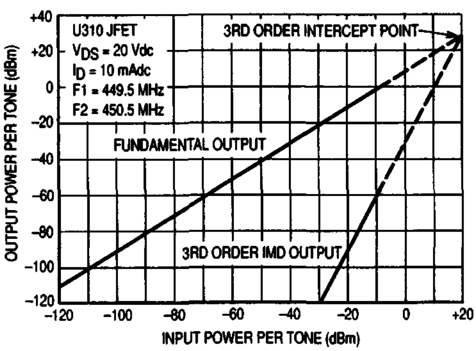
B_W (3 dB) – 36.5 MHz
I_D – 10 mAdc
V_{DS} – 20 Vdc
Device case grounded
IM test tones – f1 = 449.5 MHz, f2 = 450.5 MHz

C1 = 1–10 pF Johanson Air variable trimmer.
C2, C5 = 100 pF feed thru button capacitor.
C3, C4, C6 = 0.5–6 pF Johanson Air variable trimmer.

L1 = 1/8″ x 1/32″ x 1–5/8″ copper bar.
L2, L4 = Ferroxcube Vk200 choke.
L3 = 1/8″ x 1/32″ x 1–7/8″ copper bar.

Figure 12. 450 MHz IMD Evaluation Amplifier

Amplifier power gain and IMD products are a function of the load impedance. For the amplifier design shown above with C4 and C6 adjusted to reflect a load to the drain resulting in a nominal power gain of 9 dB, the 3rd order intercept point (IP) value is 29 dBm. Adjusting C4, C6 to provide larger load values will result in higher gain, smaller bandwidth and lower IP values. For example, a nominal gain of 13 dB can be achieved with an intercept point of 19 dBm.



Example of intercept point plot use:
Assume two in–band signals of –20 dBm at the amplifier input. They will result in a 3rd-order IMD signal at the output of –90 dBm. Also, each signal level at the output will be –11 dBm, showing an amplifier gain of 9.0 dB and an intermodulation ratio (IMR) capability of 79 dB. The gain and IMR values apply only for signal levels below comparison.

Figure 13. Two-Tone 3rd-Order Intercept Point

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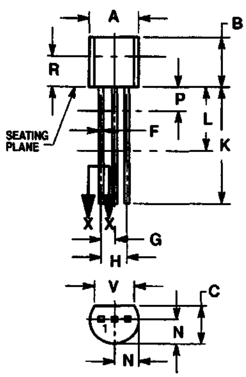
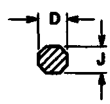
PACKAGE DIMENSIONS





SECTION X–X

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. DIMENSION F APPLIES BETWEEN P AND L. DIMENSION D AND J APPLY BETWEEN L AND K MINIMUM. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.022	0.41	0.55
F	0.016	0.019	0.41	0.48
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	—	12.70	—
L	0.250	—	6.35	—
N	0.080	0.105	2.04	2.66
P	—	0.100	—	2.54
R	0.115	—	2.93	—
V	0.135	—	3.43	—

CASE 029–04
(TO–226AA)
ISSUE AD

STYLE 5:
PIN 1. DRAIN
2. SOURCE
3. GATE

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MOTOROLA

MC78L00, A Series

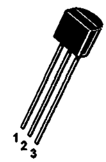
Three-Terminal Low Current Positive Voltage Regulators

The MC78L00, A Series of positive voltage regulators are inexpensive, easy–to–use devices suitable for a multitude of applications that require a regulated supply of up to 100 mA. Like their higher powered MC7800 and MC78M00 Series cousins, these regulators feature internal current limiting and thermal shutdown making them remarkably rugged. No external components are required with the MC78L00 devices in many applications.

These devices offer a substantial performance advantage over the traditional zener diode–resistor combination, as output impedance and quiescent current are substantially reduced.

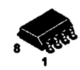
- Wide Range of Available, Fixed Output Voltages
- Low Cost
- Internal Short Circuit Current Limiting
- Internal Thermal Overload Protection
- No External Components Required
- Complementary Negative Regulators Offered (MC79L00 Series)
- Available in either ±5% (AC) or ±10% (C) Selections

P SUFFIX
CASE 29



Pin 1. Output
2. GND
3. Input

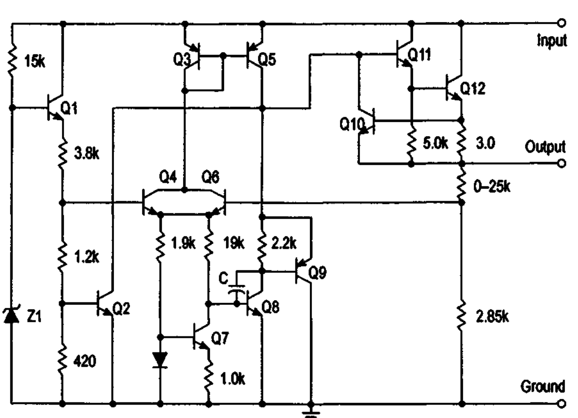
D SUFFIX
PLASTIC PACKAGE
CASE 751
(SOP–8)*



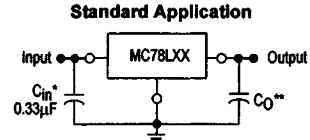
Pin		
1. V_{out}	5. NC
2. GND	6. GND
3. GND	7. GND
4. NC	8. V_{in}

* SOP–8 is an internally modified SO–8 package. Pins 2, 3, 6, and 7 are electrically common to the die attach flag. This internal lead frame modification decreases package thermal resistance and increases power dissipation capability when appropriately mounted on a printed circuit board. SOP–8 conforms to all external dimensions of the standard SO–8 package.

Representative Schematic Diagram



Standard Application



A common ground is required between the input and the output voltages. The input voltage must remain typically 2.0 V above the output voltage even during the low point on the input ripple voltage.

*C_{in} is required if regulator is located an appreciable distance from power supply filter.
**C_O is not needed for stability; however, it does improve transient response.

ORDERING INFORMATION

Device	Operating Temperature Range	Package
MC78LXXACD*	T_J = 0° to +125°C	SOP–8
MC78LXXACP		Plastic Power
MC78LXXCP		Plastic Power
MC78LXXABD*	T_J = –40° to +125°C	SOP–8
MC78LXXABP*		Plastic Power

XX indicates nominal voltage
*Available in 5, 8, 9, 12 and 15 V devices.

DEVICE TYPE/NOMINAL VOLTAGE

10%	5%	Voltage
MC78L05C	MC78L05AC	5.0
MC78L08C	MC78L08AC	8.0
MC78L09C	MC78L09AC	9.0
MC78L12C	MC78L12AC	12
MC78L15C	MC78L15AC	15
MC78L18C	MC78L18AC	18
MC78L24C	MC78L24AC	24

 Rev 3

MC78L00, A Series

MAXIMUM RATINGS (T_A = +125°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Input Voltage (2.6 V–8.0 V) (12 V–18 V) (24 V)	V_I	30 35 40	Vdc
Storage Temperature Range	T_{stg}	–65 to +150	°C
Operating Junction Temperature Range	T_J	0 to +150	°C

ELECTRICAL CHARACTERISTICS (V_I = 10 V, I_O = 40 mA, C_I = 0.33 µF, C_O = 0.1 µF, –40°C < T_J < +125°C (for MC78LXXAB), 0°C < T_J < +125°C (for MC78LXXAC), unless otherwise noted.)

Characteristics	Symbol	MC78L05AC, AB Min	MC78L05AC, AB Typ	MC78L05AC, AB Max	MC78L05C Min	MC78L05C Typ	MC78L05C Max	Unit
Output Voltage (T_J = +25°C)	V_O	4.8	5.0	5.2	4.6	5.0	5.4	Vdc
Line Regulation (T_J = +25°C, I_O = 40 mA) 7.0 Vdc ≤ V_I ≤ 20 Vdc 8.0 Vdc ≤ V_I ≤ 20 Vdc	Reg_{line}	– –	55 45	150 100	– –	55 45	200 150	mV
Load Regulation (T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA) (T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)	Reg_{load}	– –	11 5.0	60 30	– –	11 5.0	60 30	mV
Output Voltage (7.0 Vdc ≤ V_I ≤ 20 Vdc, 1.0 mA ≤ I_O ≤ 40 mA) (V_I = 10 V, 1.0 mA ≤ I_O ≤ 70 mA)	V_O	4.75 4.75	– –	5.25 5.25	4.5 4.5	– –	5.5 5.5	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	– –	3.8 –	6.0 5.5	– –	3.8 –	6.0 5.5	mA
Input Bias Current Change (8.0 Vdc ≤ V_I ≤ 20 Vdc) (1.0 mA ≤ I_O ≤ 40 mA)	ΔI_{IB}	– –	– –	1.5 0.1	– –	– –	1.5 0.2	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	40	–	–	40	–	µV
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 8.0 Vdc ≤ V_I ≤ 18 V, T_J = +25°C)	RR	41	49	–	40	49	–	dB
Dropout Voltage (T_J = +25°C)	$V_I - V_O$	–	1.7	–	–	1.7	–	Vdc

ELECTRICAL CHARACTERISTICS (V_I = 14 V, I_O = 40 mA, C_I = 0.33 µF, C_O = 0.1 µF, –40°C < T_J < +125°C (for MC78LXXAB), 0°C < T_J < +125°C (for MC78LXXAC), unless otherwise noted.)

Characteristics	Symbol	MC78L08AC, AB Min	MC78L08AC, AB Typ	MC78L08AC, AB Max	MC78L08C Min	MC78L08C Typ	MC78L08C Max	Unit
Output Voltage (T_J = +25°C)	V_O	7.7	8.0	8.3	7.36	8.0	8.64	Vdc
Line Regulation (T_J = +25°C, I_O = 40 mA) 10.5 Vdc ≤ V_I ≤ 23 Vdc 11 Vdc ≤ V_I ≤ 23 Vdc	Reg_{line}	– –	20 12	175 125	– –	20 12	200 150	mV
Load Regulation (T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA) (T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)	Reg_{load}	– –	15 8.0	80 40	– –	15 6.0	80 40	mV
Output Voltage (10.5 Vdc ≤ V_I ≤ 23 Vdc, 1.0 mA ≤ I_O ≤ 40 mA) (V_I = 14 V, 1.0 mA ≤ I_O ≤ 70 mA)	V_O	7.6 7.6	– –	8.4 8.4	7.2 7.2	– –	8.8 8.8	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	– –	3.0 –	6.0 5.5	– –	3.0 –	6.0 5.5	mA
Input Bias Current Change (11 Vdc ≤ V_I ≤ 23 Vdc) (1.0 mA ≤ I_O ≤ 40 mA)	ΔI_{IB}	– –	– –	1.5 0.1	– –	– –	1.5 0.2	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	60	–	–	52	–	µV
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 12 V ≤ V_I ≤ 23 V, T_J = +25°C)	RR	37	57	–	36	55	–	dB
Dropout Voltage (T_J = +25°C)	$V_I - V_O$	–	1.7	–	–	1.7	–	Vdc

MC78L00, A Series

ELECTRICAL CHARACTERISTICS (V_I = 15 V, I_O = 40 mA, C_I = 0.33 µF, C_O = 0.1 µF, –40°C < T_J < +125°C (for MC78LXXAB), 0°C < T_J < +125°C (for MC78LXXAC), unless otherwise noted.)

Characteristics	Symbol	MC78L09AC, AB			MC78L09C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	8.6	9.0	9.4	8.3	9.0	9.7	Vdc
Line Regulation (T_J = +25°C, I_O = 40 mA)	Reg_{line}							mV
11.5 Vdc ≤ V_I ≤ 24 Vdc		–	20	175	–	20	200	
12 Vdc ≤ V_I ≤ 24 Vdc		–	12	125	–	12	150	
Load Regulation	Reg_{load}							mV
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA)		–	15	90	–	15	90	
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)		–	8.0	40	–	6.0	40	
Output Voltage	V_O							Vdc
(11.5 Vdc ≤ V_I ≤ 24 Vdc, 1.0 mA ≤ I_O ≤ 40 mA)		8.5	–	9.5	8.1	–	9.9	
(V_I = 15 V, 1.0 mA ≤ I_O ≤ 70 mA)		8.5	–	9.5	8.1	–	9.9	
Input Bias Current	I_{IB}							mA
(T_J = +25°C)		–	3.0	6.0	–	3.0	6.0	
(T_J = +125°C)		–	–	5.5	–	–	5.5	
Input Bias Current Change	ΔI_{IB}							mA
(11 Vdc ≤ V_I ≤ 23 Vdc)		–	–	1.5	–	–	1.5	
(1.0 mA ≤ I_O ≤ 40 mA)		–	–	0.1	–	–	0.2	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	60	–	–	52	–	µV
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 13 V ≤ V_I ≤ 24 V, T_J = +25°C)	RR	37	57	–	36	55	–	dB
Dropout Voltage (T_J = +25°C)	$V_I - V_O$	–	1.7	–	–	1.7	–	Vdc

ELECTRICAL CHARACTERISTICS (V_I = 19 V, I_O = 40 mA, C_I = 0.33 µF, C_O = 0.1 µF, –40°C < T_J < +125°C (for MC78LXXAB), 0°C < T_J < +125°C (for MC78LXXAC), unless otherwise noted.)

Characteristics	Symbol	MC78L12AC, AB			MC78L12C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	11.5	12	12.5	11.1	12	12.9	Vdc
Line Regulation (T_J = +25°C, I_O = 40 mA)	Reg_{line}							mV
14.5 Vdc ≤ V_I ≤ 27 Vdc		–	120	250	–	120	250	
16 Vdc ≤ V_I ≤ 27 Vdc		–	100	200	–	100	200	
Load Regulation	Reg_{load}							mV
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA)		–	20	100	–	20	100	
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)		–	10	50	–	10	50	
Output Voltage	V_O							Vdc
(14.5 Vdc ≤ V_I ≤ 27 Vdc, 1.0 mA ≤ I_O ≤ 40 mA)		11.4	–	12.6	10.8	–	13.2	
(V_I = 19 V, 1.0 mA ≤ I_O ≤ 70 mA)		11.4	–	12.6	10.8	–	13.2	
Input Bias Current	I_{IB}							mA
(T_J = +25°C)		–	4.2	6.5	–	4.2	6.5	
(T_J = +125°C)		–	–	6.0	–	–	6.0	
Input Bias Current Change	ΔI_{IB}							mA
(16 Vdc ≤ V_I ≤ 27 Vdc)		–	–	1.5	–	–	1.5	
(1.0 mA ≤ I_O ≤ 40 mA)		–	–	0.1	–	–	0.2	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	80	–	–	80	–	µV
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 15 V ≤ V_I ≤ 25 V, T_J = +25°C)	RR	37	42	–	36	42	–	dB
Dropout Voltage (T_J = +25°C)	$V_I - V_O$	–	1.7	–	–	1.7	–	Vdc

MC78L00, A Series

ELECTRICAL CHARACTERISTICS (V_I = 23 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, –40°C < T_J < +125°C (for MC78LXXAB), 0°C < T_J < +125°C (for MC78LXXAC), unless otherwise noted.)

Characteristics	Symbol	MC78L15AC, AB			MC78L15C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	14.4	15	15.6	13.8	15	16.2	Vdc
Line Regulation (T_J = +25°C, I_O = 40 mA) 17.5 Vdc ≤ V_I ≤ 30 Vdc 20 Vdc ≤ V_I ≤ 30 Vdc	Reg_{line}	 – –	 130 110	 300 250	 – –	 130 110	 300 250	mV
Load Regulation (T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA) (T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)	Reg_{load}	 – –	 25 12	 150 75	 – –	 25 12	 150 75	mV
Output Voltage (17.5 Vdc ≤ V_I ≤ 30 Vdc, 1.0 mA ≤ I_O ≤ 40 mA) (V_I = 23 V, 1.0 mA ≤ I_O ≤ 70 mA)	V_O	 14.25 14.25	 – –	 15.75 15.75	 13.5 13.5	 – –	 16.5 16.5	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 – –	 4.4 –	 6.5 6.0	 – –	 4.4 –	 6.5 6.0	mA
Input Bias Current Change (20 Vdc ≤ V_I ≤ 30 Vdc) (1.0 mA ≤ I_O ≤ 40 mA)	ΔI_{IB}	 – –	 – –	 1.5 0.1	 – –	 – –	 1.5 0.2	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	90	–	–	90	–	μV
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 18.5 V ≤ V_I ≤ 28.5 V, T_J = +25°C)	RR	34	39	–	33	39	–	dB
Dropout Voltage (T_J = +25°C)	$V_I - V_O$	–	1.7	–	–	1.7	–	Vdc

ELECTRICAL CHARACTERISTICS (V_I = 27 V, I_O = 40 mA, C_I = 0.33 μF, C_O = 0.1 μF, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristics	Symbol	MC78L18AC			MC78L18C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	17.3	18	18.7	16.6	18	19.4	Vdc
Line Regulation (T_J = +25°C, I_O = 40 mA) 21.4 Vdc ≤ V_I ≤ 33 Vdc 20.7 Vdc ≤ V_I ≤ 33 Vdc 22 Vdc ≤ V_I ≤ 33 Vdc 21 Vdc ≤ V_I ≤ 33 Vdc	Reg_{line}	 – –	 45 35	 325 275	 – – 	 32 27 	 325 275 	mV
Load Regulation (T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA) (T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)	Reg_{load}	 – –	 30 15	 170 85	 – –	 30 15	 170 85	mV
Output Voltage (21.4 Vdc ≤ V_I ≤ 33 Vdc, 1.0 mA ≤ I_O ≤ 40 mA) (20.7 Vdc ≤ V_I ≤ 33 Vdc, 1.0 mA ≤ I_O ≤ 40 mA) (V_I = 27 V, 1.0 mA ≤ I_O ≤ 70 mA) (V_I = 27 V, 1.0 mA ≤ I_O ≤ 70 mA)	V_O	 17.1 17.1	 – –	 18.9 18.9	 16.2 16.2 	 – – 	 19.8 19.8 	Vdc
Input Bias Current (T_J = +25°C) (T_J = +125°C)	I_{IB}	 – –	 3.1 –	 6.5 6.0	 – –	 3.1 –	 6.5 6.0	mA
Input Bias Current Change (22 Vdc ≤ V_I ≤ 33 Vdc) (21 Vdc ≤ V_I ≤ 33 Vdc) (1.0 mA ≤ I_O ≤ 40 mA)	ΔI_{IB}	 – –	 – –	 1.5 0.1	 – –	 – –	 1.5 0.2	mA
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	150	–	–	150	–	μV
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 23 V ≤ V_I ≤ 33 V, T_J = +25°C)	RR	33	48	–	32	46	–	dB
Dropout Voltage (T_J = +25°C)	$V_I - V_O$	–	1.7	–	–	1.7	–	Vdc

MC78L00, A Series

ELECTRICAL CHARACTERISTICS (V_I = 33 V, I_O = 40 mA, C_I = 0.33 µF, C_O = 0.1 µF, 0°C < T_J < +125°C, unless otherwise noted.)

Characteristics	Symbol	MC78L24AC			MC78L24C			Unit
		Min	Typ	Max	Min	Typ	Max	
Output Voltage (T_J = +25°C)	V_O	23	24	25	22.1	24	25.9	Vdc
Line Regulation	Reg_{line}							mV
(T_J = +25°C, I_O = 40 mA)								
27.5 Vdc ≤ V_I ≤ 38 Vdc		–	–	–	–	35	350	
28 Vdc ≤ V_I ≤ 80 Vdc		–	50	300	–	30	300	
27 Vdc ≤ V_I ≤ 38 Vdc		–	60	350	–	–	–	
Load Regulation	Reg_{load}							mV
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 100 mA)		–	40	200	–	40	200	
(T_J = +25°C, 1.0 mA ≤ I_O ≤ 40 mA)		–	20	100	–	20	100	
Output Voltage	V_O							Vdc
(28 Vdc ≤ V_I ≤ 38 Vdc, 1.0 mA ≤ I_O ≤ 40 mA)					21.6	–	26.4	
(27 Vdc ≤ V_I ≤ 38 Vdc, 1.0 mA ≤ I_O ≤ 40 mA)		22.8	–	25.2				
(28 Vdc ≤ V_I = 33 Vdc, 1.0 mA ≤ I_O ≤ 70 mA)					21.6	–	26.4	
(27 Vdc ≤ V_I ≤ 33 Vdc, 1.0 mA ≤ I_O ≤ 70 mA)		22.8	–	25.2				
Input Bias Current	I_{IB}							mA
(T_J = +25°C)		–	3.1	6.5	–	3.1	6.5	
(T_J = +125°C)		–	–	6.0	–	–	6.0	
Input Bias Current Change	ΔI_{IB}							mA
(28 Vdc ≤ V_I ≤ 38 Vdc)		–	–	1.5	–	–	1.5	
(1.0 mA ≤ I_O ≤ 40 mA)		–	–	0.1	–	–	0.2	
Output Noise Voltage (T_A = +25°C, 10 Hz ≤ f ≤ 100 kHz)	V_n	–	200	–	–	200	–	µV
Ripple Rejection (I_O = 40 mA, f = 120 Hz, 29 V ≤ V_I ≤ 35 V, T_J = +25°C)	RR	31	45	–	30	43	–	dB
Dropout Voltage (T_J = +25°C)	$V_I - V_O$	–	1.7	–	–	1.7	–	Vdc

MC78L00, A Series

Figure 1. Dropout Characteristics

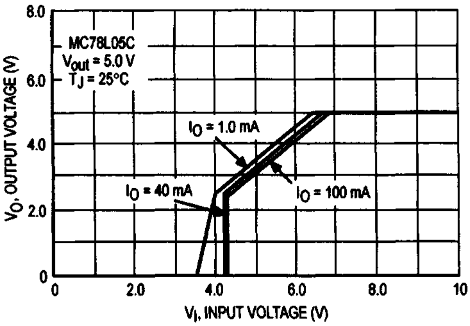


Figure 2. Dropout Voltage versus Junction Temperature

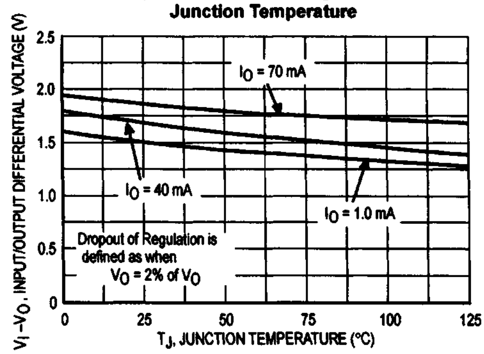


Figure 3. Input Bias Current versus Ambient Temperature

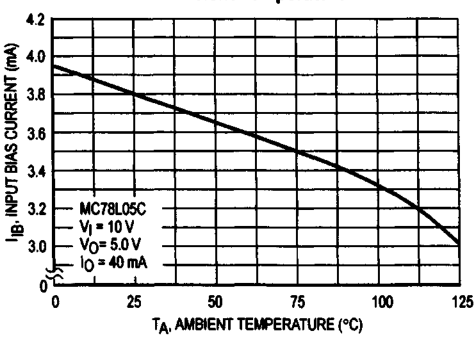


Figure 4. Input Bias Current versus Input Voltage

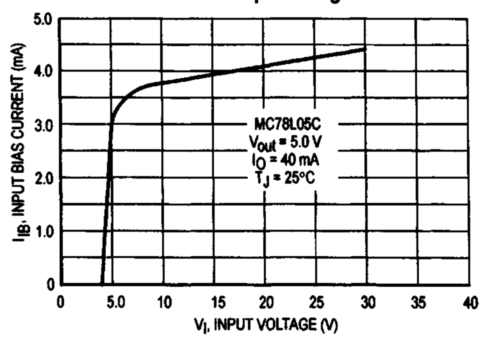


Figure 5. Maximum Average Power Dissipation versus Ambient Temperature – TO–92 Type Package

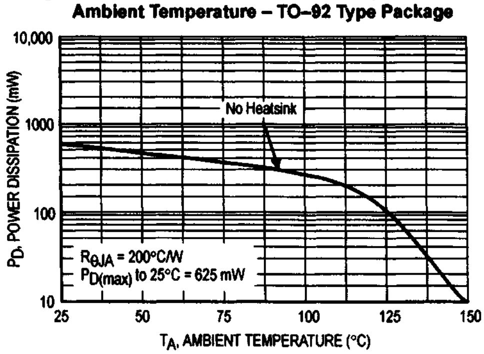
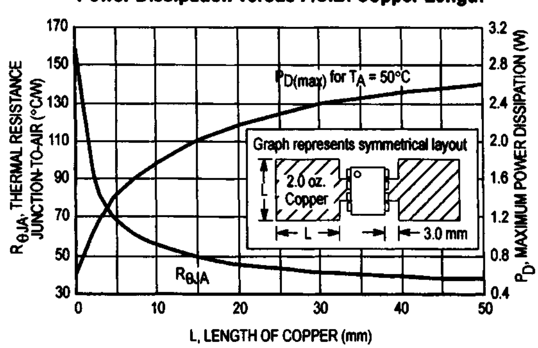


Figure 6. SOP–8 Thermal Resistance and Maximum Power Dissipation versus P.C.B. Copper Length



MC78L00, A Series

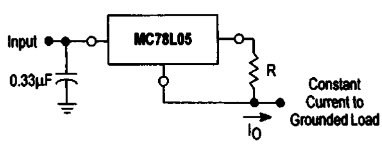
APPLICATIONS INFORMATION

Design Considerations

The MC78L00 Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition. Internal Short Circuit Protection limits the maximum current the circuit will pass.

In many low-current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. The input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33 µF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen.The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead. Bypassing the output is also recommended.

Figure 7. Current Regulator



The MC78L00 regulators can also be used as a current source when connected as above. In order to minimize dissipation the MC78L05C is chosen in this application. Resistor R determines the current as follows:

$$I_O = \frac{5.0\ V}{R} + I_B$$

I_{IB} = 3.8 mA over line and load changes

For example, a 100 mA current source would require R to be a 50 Ω, 1/2 W resistor and the output voltage compliance would be the input voltage less 7 V.

Figure 8. ± 15 V Tracking Voltage Regulator

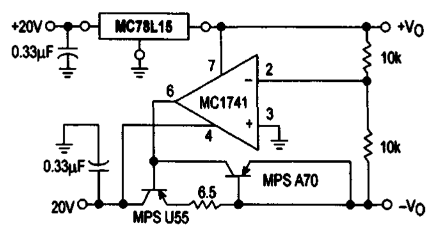
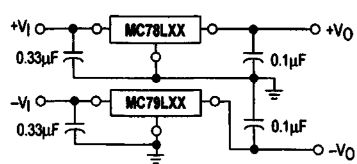


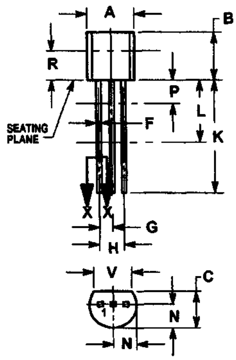
Figure 9. Positive and Negative Regulator

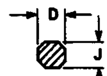


MC78L00, A Series

OUTLINE DIMENSIONS

P SUFFIX
PLASTIC PACKAGE
CASE 29–04
ISSUE AD



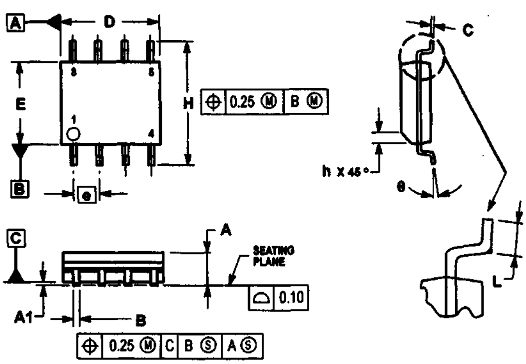


SECTION X–X

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. DIMENSION F APPLIES BETWEEN P AND L. DIMENSION D AND J APPLY BETWEEN L AND K MINIMUM. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.022	0.41	0.55
F	0.016	0.019	0.41	0.48
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	—	12.70	—
L	0.250	—	6.35	—
N	0.080	0.105	2.04	2.66
P	—	0.100	—	2.54
R	0.115	—	2.93	—
V	0.135	—	3.43	—

D SUFFIX
PLASTIC PACKAGE
CASE 751–05
(SOP–8)
ISSUE R



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°

How to reach us:
USA / EUROPE / Locations Not Listed: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036. 1–800–441–2447 or 602–303–5454

MFAX: RMFAX0@email.sps.mot.com – TOUCHTONE 602–244–6609
INTERNET: http://Design–NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, 6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–81–3521–8315

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298

MOTOROLA

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MC78L00/D

National Semiconductor

September 1997

LM386
Low Voltage Audio Power Amplifier

General Description

The LM386 is a power amplifier designed for use in low voltage consumer applications. The gain is internally set to 20 to keep external part count low, but the addition of an external resistor and capacitor between pins 1 and 8 will increase the gain to any value up to 200.

The inputs are ground referenced while the output is automatically biased to one half the supply voltage. The quiescent power drain is only 24 milliwatts when operating from a 6 volt supply, making the LM386 ideal for battery operation.

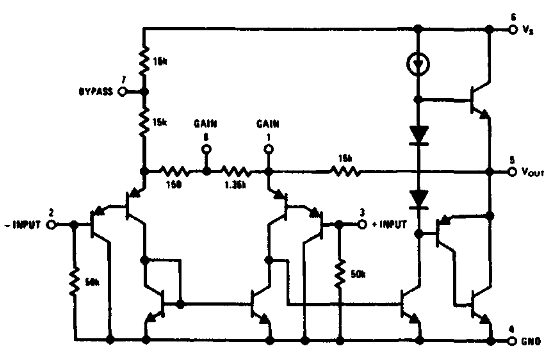
Features

- Battery operation
- Minimum external parts
- Wide supply voltage range: 4V–12V or 5V–18V
- Low quiescent current drain: 4 mA
- Voltage gains from 20 to 200
- Ground referenced input
- Self-centering output quiescent voltage
- Low distortion
- Available in 8 pin MSOP package

Applications

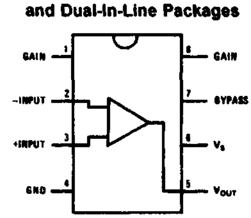
- AM-FM radio amplifiers
- Portable tape player amplifiers
- Intercoms
- TV sound systems
- Line drivers
- Ultrasonic drivers
- Small servo drivers
- Power converters

Equivalent Schematic and Connection Diagrams



DS006976-1

Small Outline, Molded Mini Small Outline, and Dual-In-Line Packages



DS006976-2

Top View
Order Number LM386M-1, LM386MM-1, LM386N-1, LM386N-3 or LM386N-4
See NS Package Number M08A, MUA08A or N08E

 www.national.com

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	
(LM386N-1, -3, LM386M-1)	15V
Supply Voltage (LM386N-4)	22V
Package Dissipation (Note 3)	
(LM386N)	1.25W
(LM386M)	0.73W
(LM386MM-1)	0.595W
Input Voltage	±0.4V
Storage Temperature	65 C to +150 C
Operating Temperature	0 C to +70 C
Junction Temperature	+150 C
Soldering Information	
Dual-In-Line Package	
Soldering (10 sec)	+260 C
Small Outline Package	
(SOIC and MSOP)	
Vapor Phase (60 sec)	+215 C
Infrared (15 sec)	+220 C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Thermal Resistance	
θ_{JC} (DIP)	37 C/W
θ_{JA} (DIP)	107 C/W
θ_{JC} (SO Package)	35 C/W
θ_{JA} (SO Package)	172 C/W
θ_{JA} (MSOP)	210 C/W
θ_{JC} (MSOP)	56 C/W

Electrical Characteristics(Notes 1, 2)

T_A = 25 C

Parameter	Conditions	Min	Typ	Max	Units
Operating Supply Voltage (V_S)					
LM386N-1, -3, LM386M-1, LM386MM-1		4		12	V
LM386N-4		5		18	V
Quiescent Current (I_Q)	V_S = 6V, V_{IN} = 0		4	8	mA
Output Power (P_{OUT})					
LM386N-1, LM386M-1, LM386MM-1	V_S = 6V, R_L = 8Ω, THD = 10%	250	325		mW
LM386N-3	V_S = 9V, R_L = 8Ω, THD = 10%	500	700		mW
LM386N-4	V_S = 16V, R_L = 32Ω, THD = 10%	700	1000		mW
Voltage Gain (A_V)	V_S = 6V, f = 1 kHz		26		dB
	10 µF from Pin 1 to 8		46		dB
Bandwidth (BW)	V_S = 6V, Pins 1 and 8 Open		300		kHz
Total Harmonic Distortion (THD)	V_S = 6V, R_L = 8Ω, P_{OUT} = 125 mW f = 1 kHz, Pins 1 and 8 Open		0.2		%
Power Supply Rejection Ratio (PSRR)	V_S = 6V, f = 1 kHz, C_{BYPASS} = 10 µF Pins 1 and 8 Open, Referred to Output		50		dB
Input Resistance (R_{IN})			50		kΩ
Input Bias Current (I_{BIAS})	V_S = 6V, Pins 2 and 3 Open		250		nA

Note 1: All voltages are measured with respect to the ground pin, unless otherwise specified.

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: For operation in ambient temperatures above 25 C, the device must be derated based on a 150 C maximum junction temperature and 1) a thermal resistance of 80 C/W junction to ambient for the dual-in-line package and 2) a thermal resistance of 170 C/W for the small outline package.

Application Hints

GAIN CONTROL

To make the LM386 a more versatile amplifier, two pins (1 and 8) are provided for gain control. With pins 1 and 8 open the 1.35 kΩ resistor sets the gain at 20 (26 dB). If a capacitor is put from pin 1 to 8, bypassing the 1.35 kΩ resistor, the gain will go up to 200 (46 dB). If a resistor is placed in series with the capacitor, the gain can be set to any value from 20 to 200. Gain control can also be done by capacitively coupling a resistor (or FET) from pin 1 to ground.

Additional external components can be placed in parallel with the internal feedback resistors to tailor the gain and frequency response for individual applications. For example, we can compensate poor speaker bass response by frequency shaping the feedback path. This is done with a series RC from pin 1 to 5 (paralleling the internal 15 kΩ resistor). For 6 dB effective bass boost: R ≅ 15 kΩ, the lowest value for good stable operation is R = 10 kΩ if pin 8 is open. If pins 1 and 8 are bypassed then R as low as 2 kΩ can be used. This restriction is because the amplifier is only compensated for closed-loop gains greater than 9.

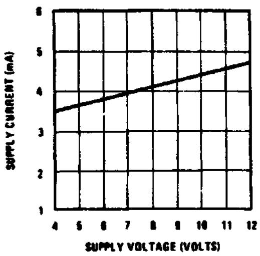
INPUT BIASING

The schematic shows that both inputs are biased to ground with a 50 kΩ resistor. The base current of the input transistors is about 250 nA, so the inputs are at about 12.5 mV when left open. If the dc source resistance driving the LM386 is higher than 250 kΩ it will contribute very little additional offset (about 2.5 mV at the input, 50 mV at the output). If the dc source resistance is less than 10 kΩ, then shorting the unused input to ground will keep the offset low (about 2.5 mV at the input, 50 mV at the output). For dc source resistances between these values we can eliminate excess offset by putting a resistor from the unused input to ground, equal in value to the dc source resistance. Of course all offset problems are eliminated if the input is capacitively coupled.

When using the LM386 with higher gains (bypassing the 1.35 kΩ resistor between pins 1 and 8) it is necessary to bypass the unused input, preventing degradation of gain and possible instabilities. This is done with a 0.1 μF capacitor or a short to ground depending on the dc source resistance on the driven input.

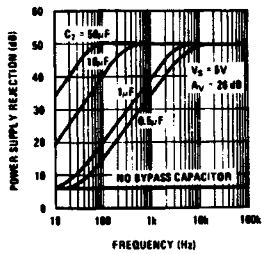
Typical Performance Characteristics

Quiescent Supply Current vs Supply Voltage



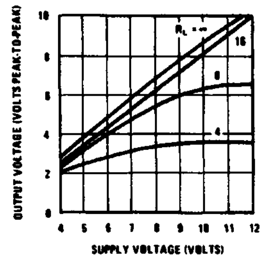
DS006976-5

Power Supply Rejection Ratio (Referred to the Output) vs Frequency



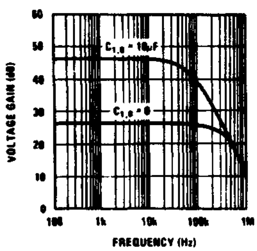
DS006976-12

Peak-to-Peak Output Voltage Swing vs Supply Voltage



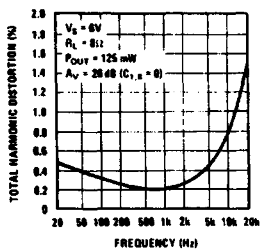
DS006976-13

Voltage Gain vs Frequency



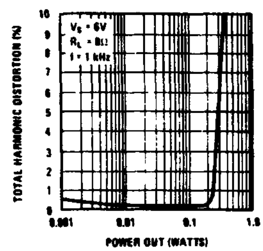
DS006976-14

Distortion vs Frequency



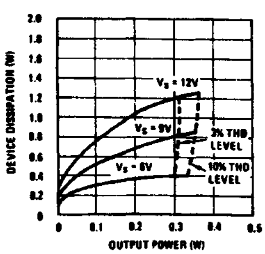
DS006976-15

Distortion vs Output Power



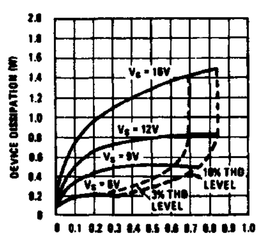
DS006976-16

Device Dissipation vs Output Power—4Ω Load



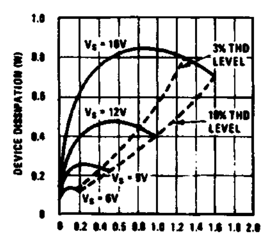
DS006976-17

Device Dissipation vs Output Power—8Ω Load



DS006976-18

Device Dissipation vs Output Power—16Ω Load



DS006976-19

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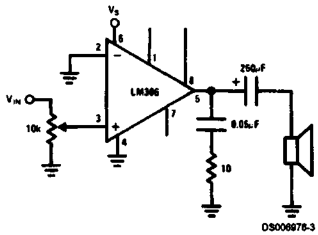
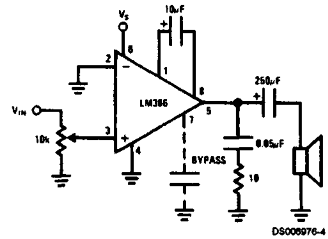
Typical Applications

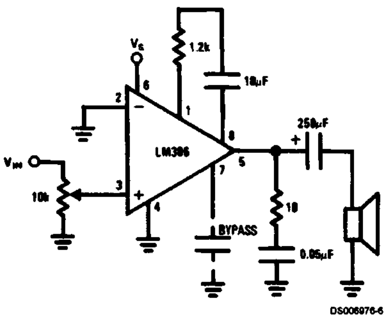
Amplifier with Gain = 20
Minimum Parts



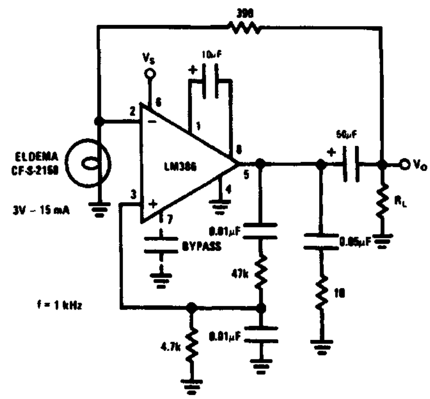
Amplifier with Gain = 200



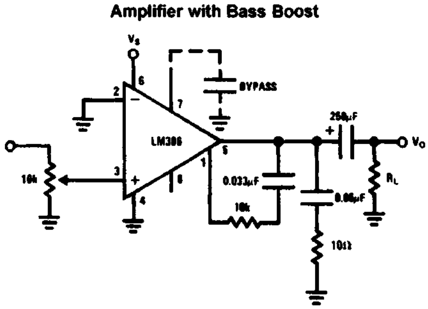
Amplifier with Gain = 50



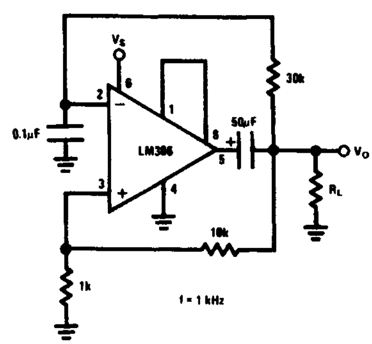
Low-Distortion Power Wienbridge Oscillator



Amplifier with Bass Boost

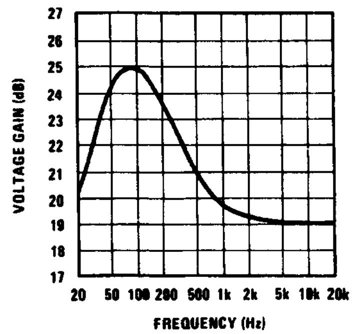


Square Wave Oscillator



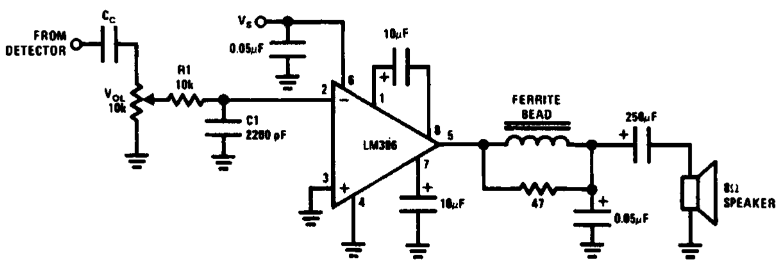
Typical Applications (Continued)

Frequency Response with Bass Boost



DS006976-10

AM Radio Power Amplifier



DS006976-11

Note 4: Twist Supply lead and supply ground very tightly.

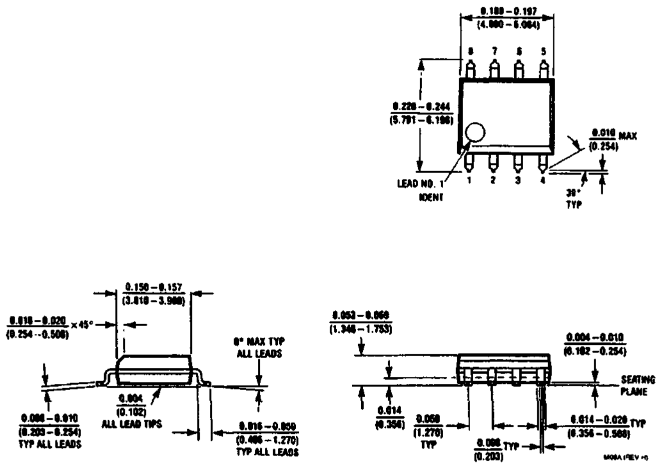
Note 5: Twist speaker lead and ground very tightly.

Note 6: Ferrite bead in Ferroxcube K5-001-001/3B with 3 turns of wire.

Note 7: R1C1 band limits input signals.

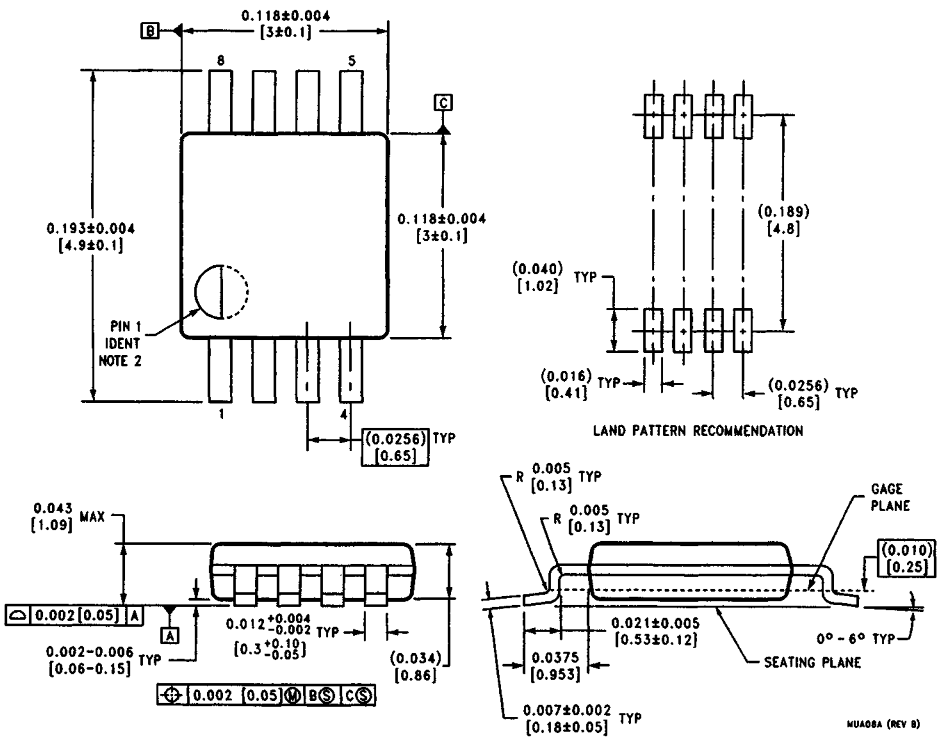
Note 8: All components must be spaced very closely to IC.

Physical Dimensions inches (millimeters) unless otherwise noted



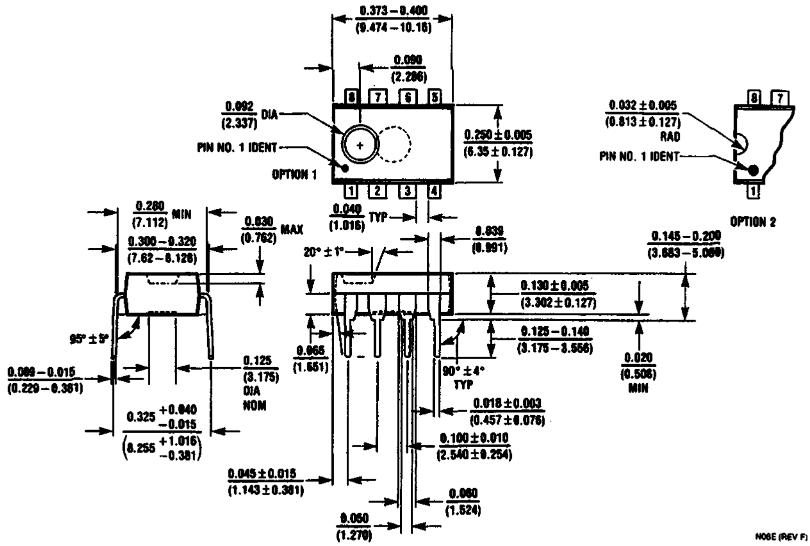
SO Package (M)
Order Number LM386M-1
NS Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



8-Lead (0.118" Wide) Molded Mini Small Outline Package
Order Number LM386MM-1
NS Package Number MUA08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



Dual-In-Line Package (N)
Order Number LM386N-1, LM386N-3 or LM386N-4
NS Package Number N08E

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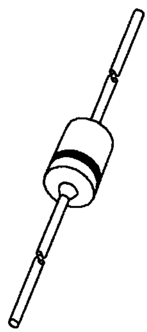
DISCRETE SEMICONDUCTORS

DATA SHEET



1N4148; 1N4446; 1N4448
High-speed diodes

Product specification
1996 Sep 03
Supersedes data of April 1996
File under Discrete Semiconductors, SC01

Philips Semiconductors

PHILIPS

High-speed diodes 1N4148; 1N4446; 1N4448

FEATURES

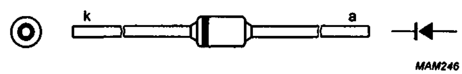
- Hermetically sealed leaded glass SOD27 (DO-35) package
- High switching speed: max. 4 ns
- General application
- Continuous reverse voltage: max. 75 V
- Repetitive peak reverse voltage: max. 75 V
- Repetitive peak forward current: max. 450 mA.

APPLICATIONS

- High-speed switching.

DESCRIPTION

The 1N4148, 1N4446, 1N4448 are high-speed switching diodes fabricated in planar technology, and encapsulated in hermetically sealed leaded glass SOD27 (DO-35) packages.



The diodes are type branded.

Fig.1 Simplified outline (SOD27; DO-35) and symbol.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{RRM}	repetitive peak reverse voltage		–	75	V
V_R	continuous reverse voltage		–	75	V
I_F	continuous forward current	see Fig.2; note 1	–	200	mA
I_{FRM}	repetitive peak forward current		–	450	mA
I_{FSM}	nonrepetitive peak forward current	square wave; T_j = 25 °C prior to surge; see Fig.4			
		t = 1 μs	–	4	A
		t = 1 ms	–	1	A
		t = 1 s	–	0.5	A
P_{tot}	total power dissipation	T_{amb} = 25 °C; note 1	–	500	mW
T_{stg}	storage temperature		−65	+200	°C
T_j	junction temperature		–	200	°C

Note

1. Device mounted on an FR4 printed circuit-board; lead length 10 mm.

High-speed diodes 1N4148; 1N4446; 1N4448

ELECTRICAL CHARACTERISTICS

T_j = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_F	forward voltage	see Fig.3			
	1N4148	I_F = 10 mA	–	1.0	V
	1N4446	I_F = 20 mA	–	1.0	V
	1N4448	I_F = 5 mA	0.62	0.72	V
		I_F = 100 mA	–	1.0	V
I_R	reverse current	V_R = 20 V; see Fig.5		25	nA
		V_R = 20 V; T_j = 150 °C; see Fig.5	–	50	μA
I_R	reverse current; 1N4448	V_R = 20 V; T_j = 100 °C; see Fig.5	–	3	μA
C_d	diode capacitance	f = 1 MHz; V_R = 0; see Fig.6		4	pF
t_{rr}	reverse recovery time	when switched from I_F = 10 mA to I_R = 60 mA; R_L = 100 Ω; measured at I_R = 1 mA; see Fig.7		4	ns
V_{fr}	forward recovery voltage	when switched from I_F = 50 mA; t_r = 20 ns; see Fig.8	–	2.5	V

THERMAL CHARACTERISTICS

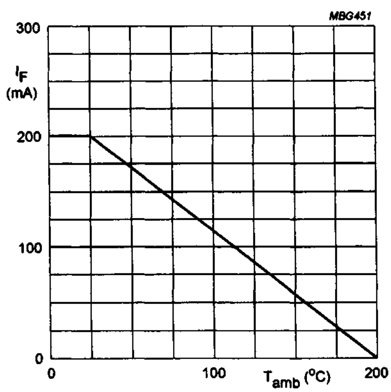
SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}tp}$	thermal resistance from junction to tie-point	lead length 10 mm	240	K/W
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	lead length 10 mm; note 1	350	K/W

Note

1. Device mounted on a printed circuit-board without metallization pad.

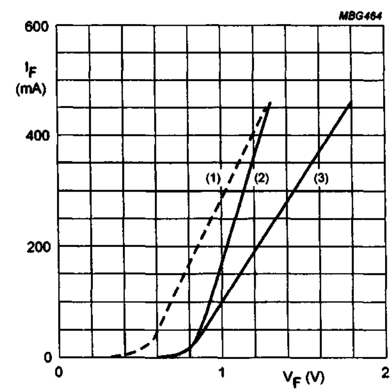
High-speed diodes 1N4148; 1N4446; 1N4448

GRAPHICAL DATA



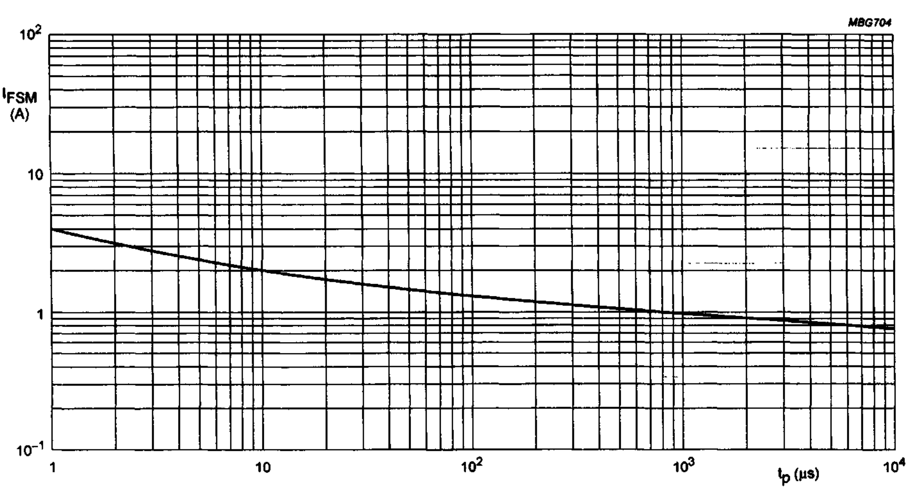
Device mounted on an FR4 printed-circuit board; lead length 10 mm.

Fig.2 Maximum permissible continuous forward current as a function of ambient temperature.



(1) T_j = 175 °C; typical values.
(2) T_j = 25 °C; typical values.
(3) T_j = 25 °C; maximum values.

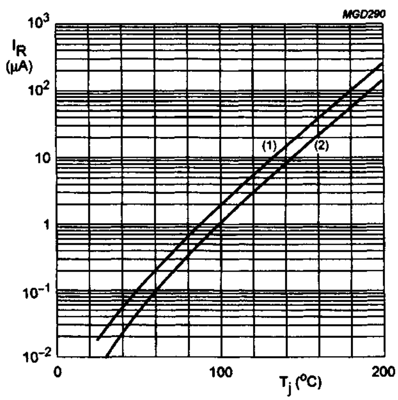
Fig.3 Forward current as a function of forward voltage.



Based on square wave currents.
T_j = 25 °C prior to surge.

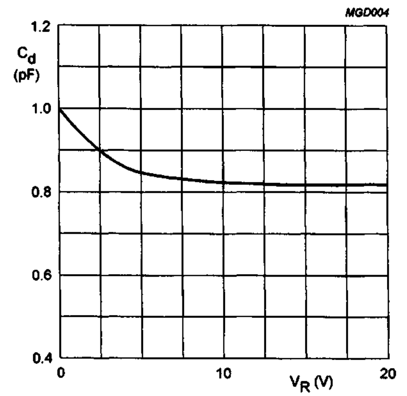
Fig.4 Maximum permissible nonrepetitive peak forward current as a function of pulse duration.

High-speed diodes 1N4148; 1N4446; 1N4448



(1) V_R = 75 V; typical values.
(2) V_R = 20 V; typical values.

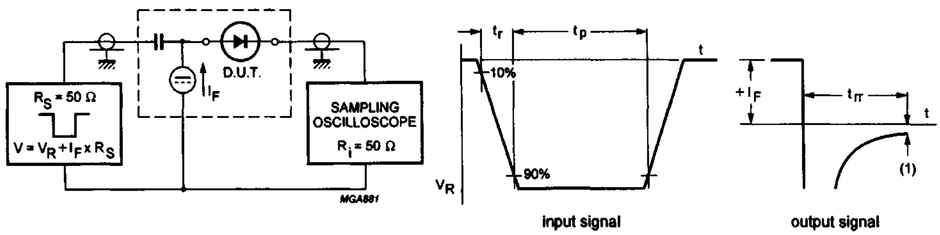
Fig.5 Reverse current as a function of junction temperature.



f = 1 MHz; T_j = 25 °C.

Fig.6 Diode capacitance as a function of reverse voltage; typical values.

High-speed diodes 1N4148; 1N4446; 1N4448



(1) I_R = 1 mA.

Fig.7 Reverse recovery voltage test circuit and waveforms.

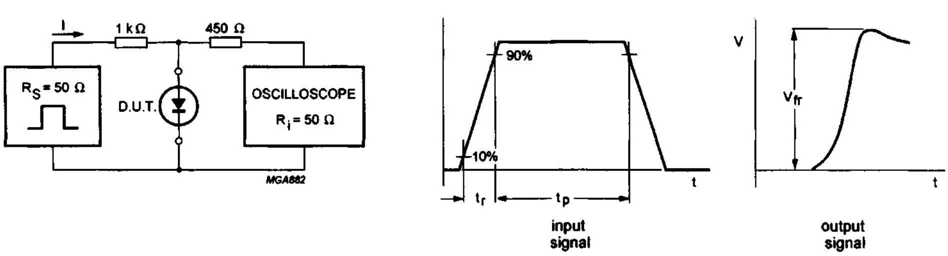
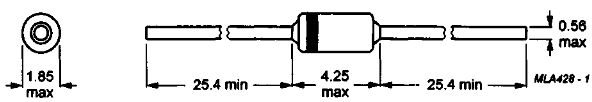


Fig.8 Forward recovery voltage test circuit and waveforms.

High-speed diodes 1N4148; 1N4446; 1N4448

PACKAGE OUTLINE



Dimensions in mm.

Fig.9 SOD27 (DO-35).

DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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RF COMMUNICATIONS PRODUCTS

DATA SHEET

SA602A
Double-balanced mixer and oscillator

Product specification
Replaces datasheet of April 17, 1990
IC17 Data Handbook

1997 Nov 07

Philips Semiconductors

PHILIPS

Double-balanced mixer and oscillator SA602A

DESCRIPTION

The SA602A is a low-power VHF monolithic double-balanced mixer with input amplifier, on-board oscillator, and voltage regulator. It is intended for high performance, low-power communication systems. The guaranteed parameters of the SA602A make this device particularly well suited for cellular radio applications. The mixer is a "Gilbert cell" multiplier configuration which typically provides 18dB of gain at 45MHz. The oscillator will operate to 200MHz. It can be configured as a crystal oscillator, a tuned tank oscillator, or a buffer for an external LO. For higher frequencies the LO input may be externally driven. The noise figure at 45MHz is typically less than 5dB. The gain, intercept performance, low-power and noise characteristics make the SA602A a superior choice for high-performance battery operated equipment. It is available in an 8-lead dual in-line plastic package and an 8-lead SO (surface-mount miniature package).

FEATURES

- Low current consumption: 2.4mA typical
- Excellent noise figure: <4.7dB typical at 45MHz
- High operating frequency
- Excellent gain, intercept and sensitivity
- Low external parts count; suitable for crystal/ceramic filters
- SA602A meets cellular radio specifications

PIN CONFIGURATION

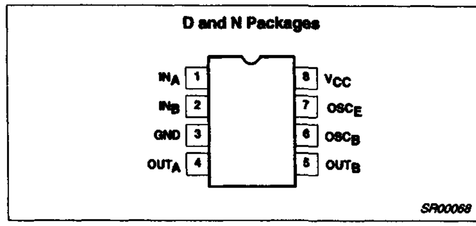


Figure 1. Pin Configuration

APPLICATIONS

- Cellular radio mixer/oscillator
- Portable radio
- VHF transceivers
- RF data links
- HF/VHF frequency conversion
- Instrumentation frequency conversion
- Broadband LANs

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Dual In-Line Plastic (DIP)	-40 to +85°C	SA602AN	SOT97-1
8-Pin Plastic Small Outline (SO) package (Surface-mount)	-40 to +85°C	SA602AD	SOT96-1

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Maximum operating voltage	9	V
T_{STG}	Storage temperature range	-65 to +150	°C
T_A	Operating ambient temperature range SA602A	-40 to +85	°C
θ_{JA}	Thermal impedance D package	90	°C/W
	N package	75	°C/W

Double-balanced mixer and oscillator SA602A

BLOCK DIAGRAM

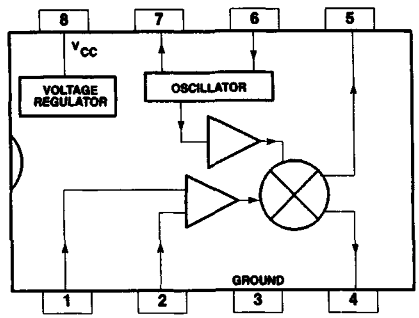


Figure 2. Block Diagram

AC/DC ELECTRICAL CHARACTERISTICS

V_{CC} = +6V, T_A = 25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			SA602A			
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		4.5		8.0	V
	DC current drain			2.4	2.8	mA
f_{IN}	Input signal frequency			500		MHz
f_{OSC}	Oscillator frequency			200		MHz
	Noise figure at 45MHz			5.0	5.5	dB
	Third-order intercept point	RF_{IN} = -45dBm: f_1 = 45.0MHz f_2 = 45.06MHz		-13	-15	dBm
	Conversion gain at 45MHz		14	17		dB
R_{IN}	RF input resistance		1.5			kΩ
C_{IN}	RF input capacitance			3	3.5	pF
	Mixer output resistance	(Pin 4 or 5)		1.5		kΩ

DESCRIPTION OF OPERATION

The SA602A is a Gilbert cell, an oscillator/buffer, and a temperature compensated bias network as shown in the equivalent circuit. The Gilbert cell is a differential amplifier (Pins 1 and 2) which drives a balanced switching cell. The differential input stage provides gain and determines the noise figure and signal handling performance of the system.

The SA602A is designed for optimum low-power performance. When used with the SA604 as a 45MHz cellular radio second IF and demodulator, the SA602A is capable of receiving -119dBm signals with a 12dB S/N ratio. Third-order intercept is typically -13dBm (that is approximately +5dBm output intercept because of the RF gain). The system designer must be cognizant of this large signal limitation. When designing LANs or other closed systems where transmission levels are high, and small-signal or signal-to-noise issues are not critical, the input to the SA602A should be appropriately scaled.

Besides excellent low-power performance well into VHF, the SA602A is designed to be flexible. The input, RF mixer output and oscillator ports can support a variety of configurations provided the designer understands certain constraints, which will be explained here.

The RF inputs (Pins 1 and 2) are biased internally. They are symmetrical. The equivalent AC input impedance is approximately 1.5k || 3pF through 50MHz. Pins 1 and 2 can be used interchangeably, but they should not be DC biased externally. Figure 5 shows three typical input configurations.

The mixer outputs (Pins 4 and 5) are also internally biased. Each output is connected to the internal positive supply by a 1.5kΩ resistor. This permits direct output termination yet allows for balanced output as well. Figure 6 shows three single-ended output configurations and a balanced output.

Double-balanced mixer and oscillator SA602A

The oscillator is capable of sustaining oscillation beyond 200MHz in crystal or tuned tank configurations. The upper limit of operation is determined by tank "Q" and required drive levels. The higher the "Q" of the tank or the smaller the required drive, the higher the permissible oscillation frequency. If the required LO is beyond oscillation limits, or the system calls for an external LO, the external signal can be injected at Pin 6 through a DC blocking capacitor. External LO should be at least $200mV_{P-P}$.

Figure 7 shows several proven oscillator circuits. Figure 7a is appropriate for cellular radio. As shown, an overtone mode of operation is utilized. Capacitor C3 and inductor L1 suppress oscillation at the crystal fundamental frequency. In the fundamental mode, the suppression network is omitted.

Figure 8 shows a Colpitts varactor tuned tank oscillator suitable for synthesizer-controlled applications. It is important to buffer the output of this circuit to assure that switching spikes from the first counter or prescaler do not end up in the oscillator spectrum. The dual-gate MOSFET provides optimum isolation with low current. The FET offers good isolation, simplicity, and low current, while the bipolar transistors provide the simple solution for noncritical applications. The resistive divider in the emitter-follower circuit should be chosen to provide the minimum input signal which will assure correct system operation.

When operated above 100MHz, the oscillator may not start if the Q of the tank is too low. A 22kΩ resistor from Pin 7 to ground will increase the DC bias current of the oscillator transistor. This improves the AC operating characteristic of the transistor and should help the oscillator to start. A 22kΩ resistor will not upset the other DC biasing internal to the device, but smaller resistance values should be avoided.

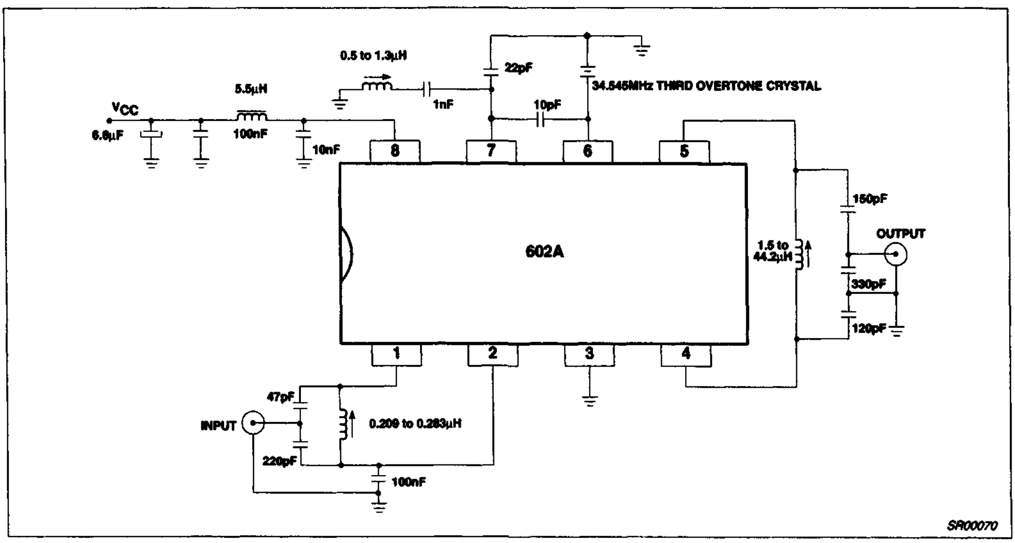


Figure 3. Test Configuration

Double-balanced mixer and oscillator SA602A

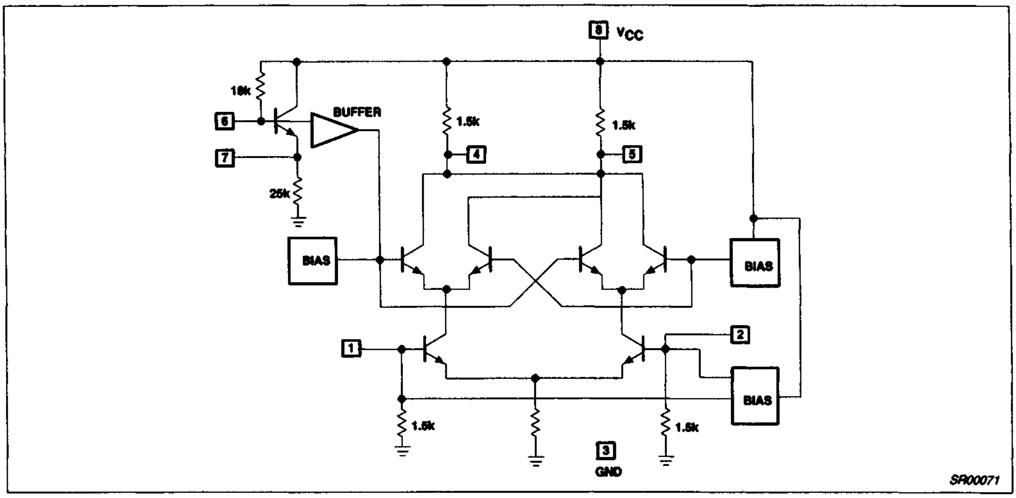


Figure 4. Equivalent Circuit

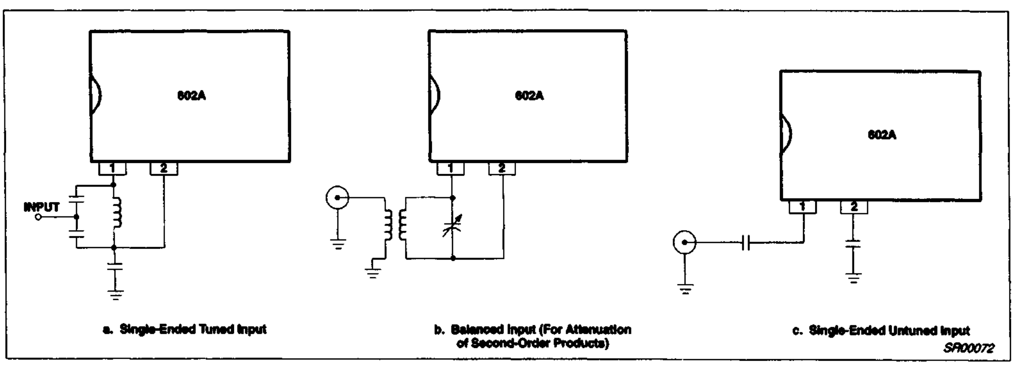
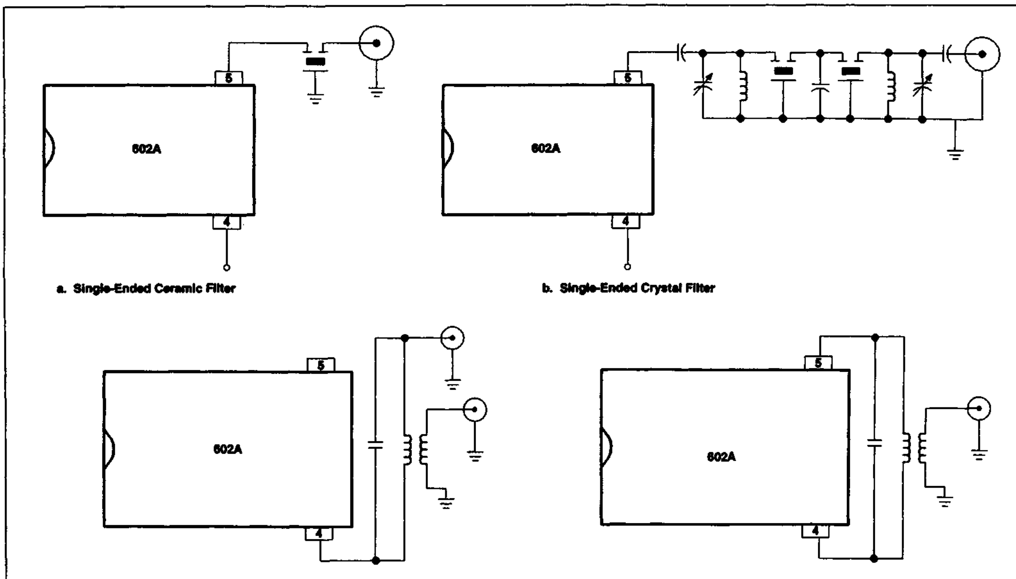


Figure 5. Input Configuration

Double-balanced mixer and oscillator SA602A



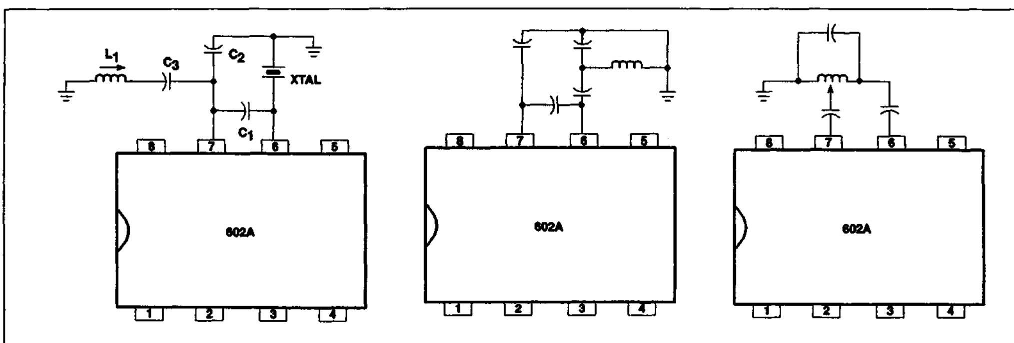
a. Single-Ended Ceramic Filter

b. Single-Ended Crystal Filter

c. Single-Ended IFT

d.. Balanced Output

Figure 6. Output Configuration



a. Colpitts Crystal Oscillator (Overtone Mode)

b. Colpitts L/C Tank Oscillator

c. Hartley L/C Tank Oscillator

Figure 7. Oscillator Circuits

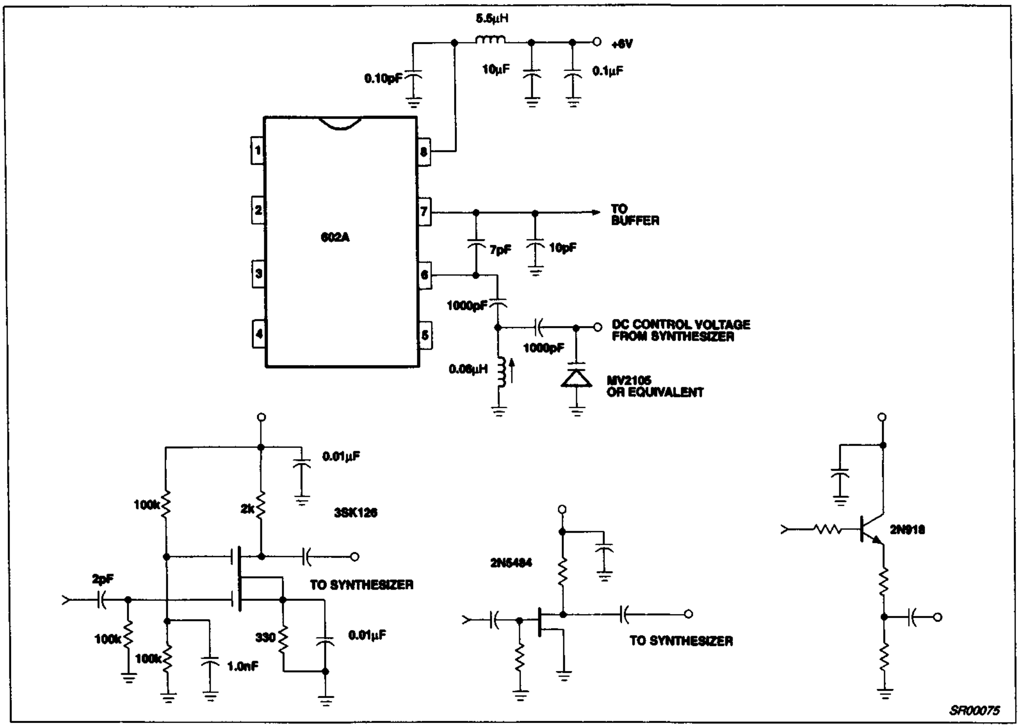


Figure 8. Colpitts Oscillator Suitable for Synthesizer Applications and Typical Buffers

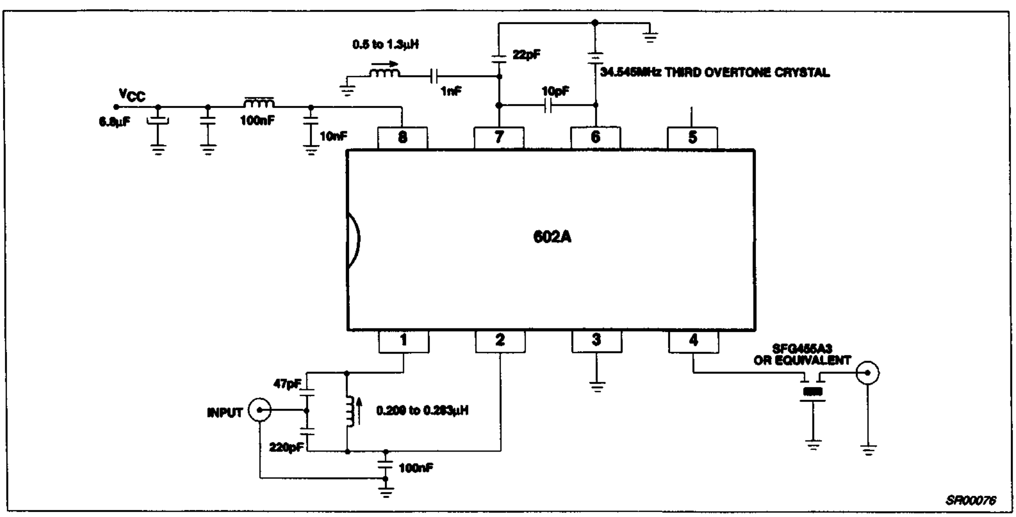


Figure 9. Typical Application for Cellular Radio

Philips Semiconductors | Product specification

Double-balanced mixer and oscillator — SA602A

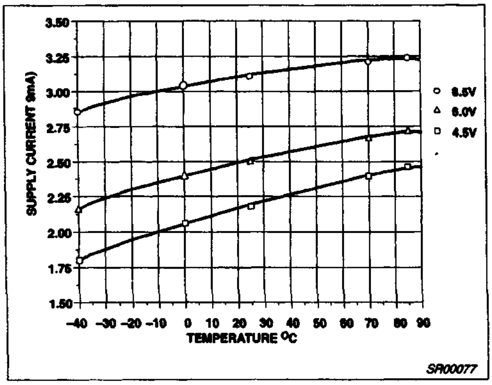


Figure 10. I_{CC} vs Supply Voltage

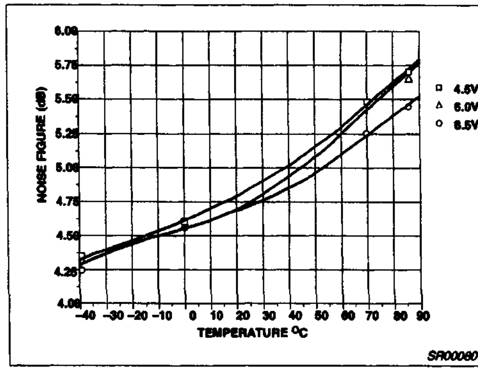


Figure 13. Noise Figure

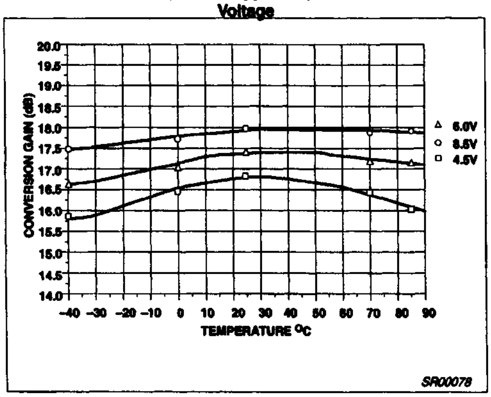


Figure 11. Conversion Gain vs Supply Voltage

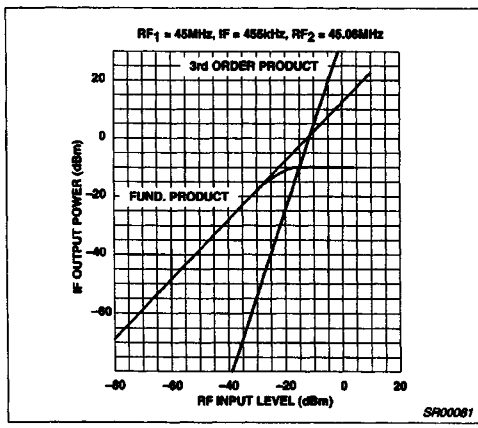


Figure 14. Third-Order Intercept and Compression

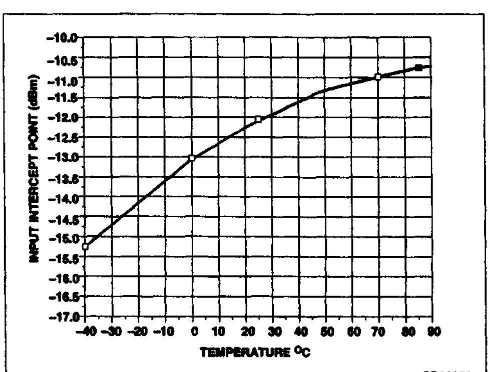


Figure 12. Third-Order Intercept Point

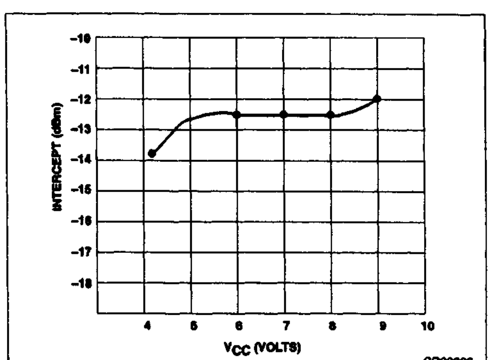
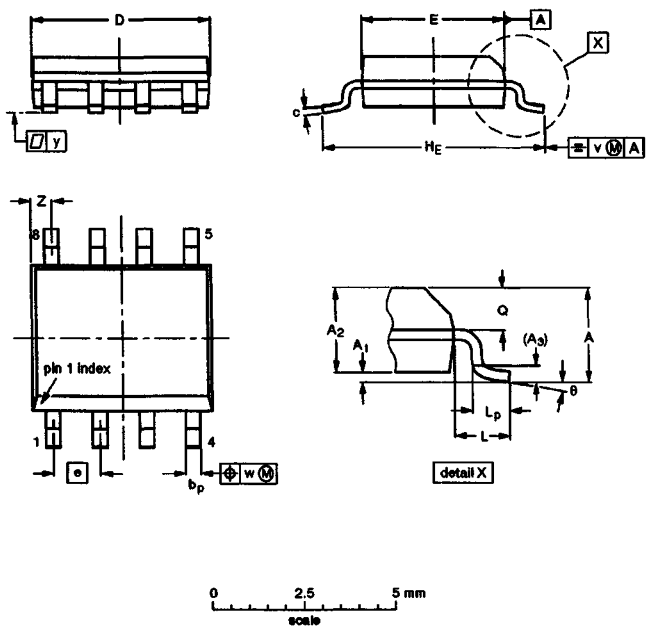


Figure 15. Input Third-Order Intermod Point vs V_{CC}

Double-balanced mixer and oscillator | SA602A

SO8: plastic small outline package; 8 leads; body width 3.9mm | **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(2)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.20 0.19	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

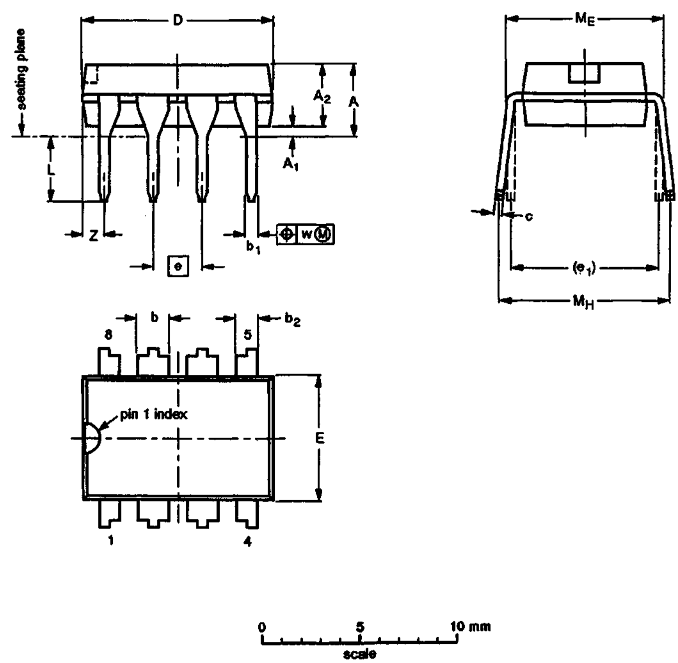
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03S	MS-012AA				~~92-11-17~~ 95-02-04

Double-balanced mixer and oscillator SA602A

DIP8: plastic dual in-line package; 8 leads (300 mil) **SOT97-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.14	0.53 0.38	1.07 0.89	0.36 0.23	9.8 9.2	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	1.15
inches	0.17	0.020	0.13	0.068 0.045	0.021 0.015	0.042 0.035	0.014 0.009	0.39 0.36	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.045

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT97-1	050G01	MO-001AN				~~92-11-17~~ 95-02-04

Double-balanced mixer and oscillator SA602A

DEFINITIONS

Data Sheet Identification	Product Status	Definition
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Product Specification	Full Production	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

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