11

Oscillators

It is common in public-address systems to hear a loud tone when someone moves the microphone too close to a speaker. People call this *feedback*, and it is caused by sound from the speaker getting back into the microphone. When this happens, the sound is amplified again and again until the amplifier overloads. It is perhaps surprising that we hear a single tone rather than a broad range of frequencies, and it suggests that we can use feedback to make a sine-wave oscillator. We can distinguish between two kinds of feedback. The public-address oscillations are an example of *positive feedback*, where the output adds to the signal. In *negative feedback*, the output cancels part of the input, reducing the gain. We have had two examples of negative feedback so far, in the emitter resistor of the Driver Amplifier and in the source resistor of the Buffer Amplifier. In both cases, the output generates a voltage across a resistor that cancels part of the input. We will see two more examples of negative feedback when we consider the Automatic Gain Control and the Audio Amplifier. Positive feedback increases the gain of an amplifier. This was used in early radios in a circuit called a *regenerative* receiver, where positive feedback brought the receiver to the brink of oscillation. This gave a large gain and allowed a receiver to operate with only a single stage of amplification. However, regenerative receivers were difficult to adjust, and they tended to break into oscillation. Eventually they were superseded by the more stable superheterodyne receiver. Today we use positive feedback for oscillators.

11.1 Criteria for Oscillation

We start by establishing general criteria for oscillation. In Figure 11.1a, we show an amplifier with gain and a linear feedback network. We will call the input to the amplifier x and the output y. We characterize the amplifier by a gain G that is the ratio of the output to the input. In the NorCal 40A oscillators, the amplifier is a transistor with an output current and input voltage, and so the gain is a transconductance. For the feedback network, the roles of x and y reverse, so that y is the input and x is the output. We characterize the feedback network by a loss L, which is the ratio of input to output. We can write the following equations:

$$y = Gx, \tag{11.1}$$

$$y = Lx, \tag{11.2}$$

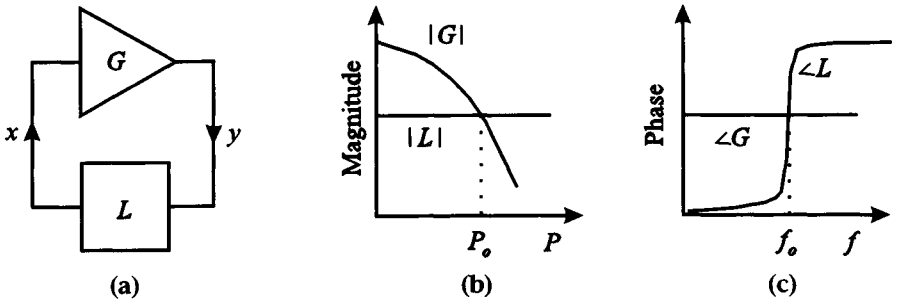


Figure 11.1. Oscillator network consisting of an amplifier with a gain G, and a feedback network with a loss L (a), satisfying the magnitude (b) and phase (c) criteria.

where all the quantities are complex numbers. If $G \neq L$, x and y must be zero, and there is no oscillation. However, if $G = L$, then we can have an output. Since G and L are complex numbers, this is actually two conditions, one for magnitudes and one for phases. We can write the oscillation criteria as

$$|G| = |L|, \tag{11.3}$$

$$\angle G = \angle L. \tag{11.4}$$

Physically, the gain of the amplifier must compensate for the loss of the feedback network, and the phase shift of the feedback network must offset the phase shift of the amplifier.

The key to satisfying the magnitude criterion is to recognize that the gain of practical amplifiers falls at high power levels. This can be from overload, or from a gain-limiting circuit. This is shown in Figure 11.1b, where the gain and loss are plotted as a function of the output power P. The loss $|L|$ is shown as a flat line, because the feedback network is linear. We meet the magnitude criterion at the intersection of these two curves:

$$|G(P_o)| = |L|, \tag{11.5}$$

where P_o is the oscillator output power. For the phase criterion, we consider the frequency variation in the feedback network. In public-address system feedback, this is provided by the acoustic delay between the speaker and the microphone. In our oscillators, it is provided by a resonant circuit that gives a rapidly varying phase near the resonant frequency. This is shown in Figure 11.1c, which gives the phase as a function of the frequency f. The amplifier phase $\angle G$ usually varies much more slowly than the phase of the resonator. We meet the phase criterion at the intersection:

$$\angle L(f_o) = \angle G. \tag{11.6}$$

This determines the oscillation frequency f_o. In our oscillator models, there is no phase shift in the amplifier; therefore, the phase criterion is satisfied at the resonant frequency of the feedback network, where there is no phase shift. In

summary, the power characteristics of the amplifier determine the output power, and the frequency characteristics of the feedback network determine the frequency. In general, high-Q networks have a fast phase variation that gives precise control of the oscillation frequency. This means that crystal oscillators are more stable than LC oscillators.

These formulas determine the power and frequency of an oscillation, but we also have to think about how the oscillation starts. This is actually a more serious mathematical problem than we can explore here, and we will give criteria that are sufficient for starting but do not cover all cases. Physically, oscillations either build up from noise or start from an external signal. If

$$|G| > |L| \tag{11.7}$$

at low powers, noise at a frequency that meets the phase criterion is repeatedly amplified until it reaches the output level that satisfies the magnitude criterion. This gives us *starting* criteria:

$$|g| > |L|, \tag{11.8}$$

$$\angle L(f_o) = \angle g, \tag{11.9}$$

where g is the small-signal gain. Some systems that oscillate well at high power levels will not start by themselves. For example, consider using a Class-C amplifier in an oscillator. Class-C amplifiers have a threshold that gives them low gain at low power levels. This is shown in Figure 11.2. I have drawn a line to indicate the response of the feedback network (L). For power levels below the starting power P_s, signals are not amplified, and there will be no oscillation. Ordinarily this is a good thing, and it means that Class-C amplifiers will not oscillate on their own. To make one oscillate, we need an external signal that is larger than P_s for a kick start. After the oscillation is started, we can remove the external signal. This is the basis of operation of the *super-regenerative receiver*, which is used in garage-door openers and inexpensive walkie-talkies. In these circuits, the received signal triggers an oscillation. The oscillators in the NorCal 40A begin in Class A; thus they are self starting. However, as the oscillation builds up, operation shifts to Class C.

The figure raises another question. There are actually two powers that meet the magnitude criterion – P_s and P_o. At which level will the oscillator settle? It

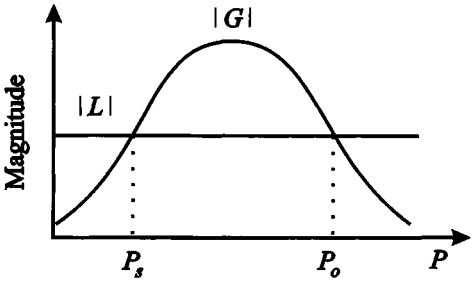


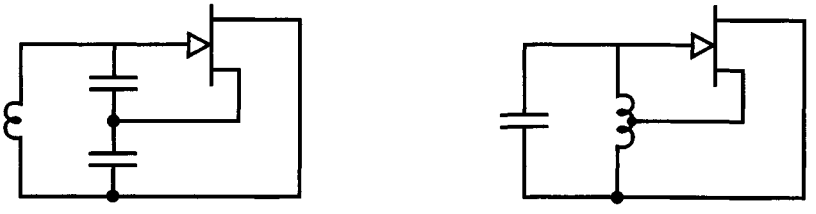
Figure 11.2. Starting problem for an oscillator with a Class-C amplifier.

turns out that P_s is not a stable operating point. If we drop slightly below P_s, then $|G| < |L|$, and the signal will die out. However, above P_s, $|G| > |L|$, and the signal increases until the output power reaches the stable operating point P_o.

11.2 Clapp Oscillator

Many, many different oscillators have been invented, and by tradition they carry the inventor's name. You may run across Hartley, Colpitts, Clapp, Pierce, Gouriet, Hansen, Harris, Butler, Lampkin, Seiler, Miller, Meissner, Vackar, Gunn, and Wien. This can be quite confusing, because some of the designs are improvements on a previous circuit. One can, however, think in terms of families of oscillators and variations within a family. One oscillator may be called by more than one name, depending on whether one is referring to the family or to a variation within a family. Each type usually has both field-effect and bipolar versions. It is often difficult to say that one design is better than another, because much depends on how well the components for the oscillator are chosen and how well the oscillator is isolated from the other circuits in the receiver. In general, each oscillator has a resonator to determine the frequency and a divider network to feed back part of the output to the input. We can classify oscillators in two major families depending on whether the inductor or the capacitor in the resonant circuit is used for the divider. The Colpitts oscillator uses a capacitive divider (Figure 11.3a), and the Hartley oscillator uses the inductor as the divider (Figure 11.3b).

The oscillators in the NorCal 40A are Clapp oscillators. The Clapp oscillator is in the Colpitts family, with a capacitor divider for feedback. Consequently, you may also hear them referred to correctly as Colpitts oscillators. In the Clapp oscillator, the inductor is replaced by a resonant circuit. This allows us to have large voltages in the resonator elements, which helps in keeping the frequency stable, without overloading the transistor. We use this circuit with an LC resonator in the variable-frequency oscillator, or VFO (Figure 11.4). The VFO uses a JFET source follower



(a) (b)

Figure 11.3. Colpitts oscillator, with a capacitive-divider feedback network (a), and Hartley oscillator, with inductor feedback (b). The inductor network is usually made by a connection part way down the coil called a *tap*. The amount of feedback is controlled by the position of the tap. In both figures, the bias and load networks are omitted for simplicity.

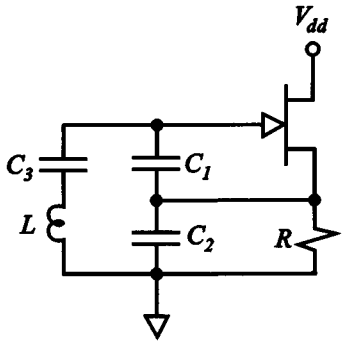


Figure 11.4. Clapp oscillator circuit that is used for the variable-frequency oscillator (VFO) in the NorCal 40A. C_1 and C_2 form the divider network, and R is the load. The gate and source bias networks and the tuning are complicated, and we omit them for now.

for the amplifier. The BFO and Transmit Oscillators use a crystal resonator with a BJT emitter follower.

We start with a small-signal model for the JFET VFO. This will give us the phase condition for starting and for oscillation and the magnitude condition for starting. The final oscillations are large voltages, and we will need a large-signal analysis for the oscillation condition for magnitudes. We replace the JFET in Figure 11.4 with the model in Figure 9.17a, and we substitute a ground connection for the supply voltage V_{dd}. We can write the small-signal equivalent circuit shown in Figure 11.5.

In this analysis, the gate-source voltage v_{gs} corresponds to the input x in Equation 11.1, and the drain current i_d is the output y. For the JFET, we write

$$i_d = g_m v_{gs}. \tag{11.10}$$

We can therefore write the small-signal gain g as

$$g = g_m. \tag{11.11}$$

There is no phase shift, and so we meet this phase condition at the resonant frequency ω_0 for the network. To see this, consider that in resonance, the reactances of the two arms of the feedback network must cancel, and

$$-\frac{1}{j\omega_0 C_2} = j\omega_0 L + \frac{1}{j\omega_0 C_3} + \frac{1}{j\omega_0 C_1}. \tag{11.12}$$

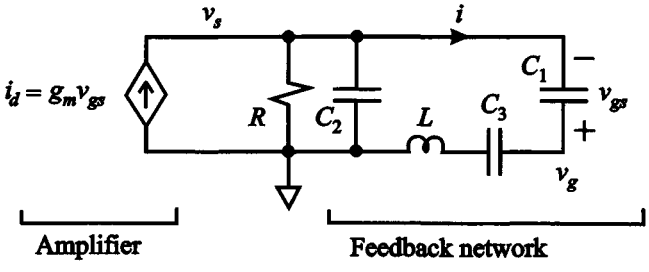


Figure 11.5. Small-signal equivalent circuit for the Clapp VFO. It takes quite a bit of rearrangement to turn Figure 11.4 into this circuit; so you should go through it carefully.

We can rewrite this as

$$\omega_0 = \frac{1}{\sqrt{LC}}, \tag{11.13}$$

where C is the series combination of the three capacitors, given by

$$C = \frac{1}{1/C_1 + 1/C_2 + 1/C_3}. \tag{11.14}$$

At resonance, the currents in the arms of the feedback network cancel, and we can write

$$i = -j\omega_0 C_2 v_s \tag{11.15}$$

and thus

$$v_{gs} = -\frac{i}{j\omega_0 C_1} = \frac{v_s C_2}{C_1}. \tag{11.16}$$

At resonance, we can write the source voltage v_s as

$$v_s = Ri_d, \tag{11.17}$$

so that we can rewrite v_{gs} as

$$v_{gs} = i_d RC_2/C_1. \tag{11.18}$$

This means that the loss L is given by

$$L = \frac{i_d}{v_{gs}} = \frac{C_1}{RC_2}. \tag{11.19}$$

Because both g and L have zero phase shift, we meet the phase criterion (Equation 11.9). The starting condition becomes

$$g_m > \frac{C_1}{RC_2}. \tag{11.20}$$

In measurements, it is convenient to measure the gate voltage v_g and the source voltage v_s. We can write

$$v_g = v_{gs} + v_s = v_s(1 + C_2/C_1). \tag{11.21}$$

This formula only depends on the feedback network, which is linear, and so it is valid for AC quantities large and small. In the NorCal 40A VFO, $C_1 = C_2$, and the circuit voltages are related by

$$v_{gs} = v_s \tag{11.22}$$

and

$$v_g = 2v_s. \tag{11.23}$$

Equation 11.19 becomes

$$L = 1/R \tag{11.24}$$

so that the starting condition (Equation 11.8) becomes

$$g_m > 1/R. \tag{11.25}$$

The oscillation starts if the transconductance is larger than the inverse of the load resistance. In practice, the required transconductance will be higher than this because of the output resistance of the JFET and losses in the resonator. In a circuit, g_m is determined by the bias voltage. In the VFO, we begin with a bias voltage near zero, so that g_m is large and the oscillation starts easily.

11.3 Variable-Frequency Oscillator

The VFO is a key component in a transceiver, because it sets the operating frequency. The VFO is shared between the transmitter and receiver, so that they track in frequency. The challenge in a VFO is that we would like to be able to adjust the frequency easily, but once we set the frequency, we would like it to stay put. If the frequency drifts, it forces the other operator to retune, and there is the danger of interfering with others on nearby frequencies. The frequency shift that can be tolerated is different for each radio service, but for the NorCal 40A, a reasonable limit is 100 Hz.

There are two basic approaches to making variable oscillators. One can start with a crystal oscillator, and use dividing and multiplying circuits to create sine waves at other frequencies. This is called a *synthesized* oscillator, and it gives good stability over a wide range of frequencies. However, the circuits are complex. The other approach is to build an LC oscillator and to minimize the frequency drift. Our VFO is an LC oscillator. There are several things that can be done to stabilize the VFO. We work at as low a frequency as possible, because frequency drifts are usually proportional to frequency. In our transceiver, the VFO is at 2.1 MHz, well below the operating frequency, 7 MHz. To vary the frequency, we use a varactor, which is a reverse-biased diode that acts as a variable capacitor. A major factor that causes drift is temperature change from heat produced by circuit components, particularly the Power Amplifier, and by changes in the outside temperature. The VFO is isolated to some extent from the Power Amplifier because it is at the other end of the board, but we also need to select the capacitors and inductors to minimize the frequency shift.

We can predict the temperature stability of the oscillator from the temperature coefficients of the components. Mathematically we write a temperature coefficient α of a quantity x in the form

$$\alpha = \frac{1}{x} \cdot \frac{dx}{dT}, \tag{11.26}$$

where T is the temperature. Usually we multiply α by a million to state it as parts per million. We can rewrite this formula in terms of logarithms as

$$\alpha = \frac{d \ln(x)}{dT}. \tag{11.27}$$

Now consider a resonant frequency given by

$$f = \frac{1}{2\pi\sqrt{LC}}. \tag{11.28}$$

We can write the logarithm of the frequency as

$$\ln(f) = -\ln(2\pi) - \frac{\ln(L)}{2} - \frac{\ln(C)}{2}. \tag{11.29}$$

We can write the frequency temperature coefficient α_f as

$$\alpha_f = \frac{d\ln(f)}{dT} = -\frac{\alpha_l + \alpha_c}{2}, \tag{11.30}$$

where α_l and α_c are the inductor and capacitor temperature coefficients. This formula shows that for good temperature stability, we must either choose stable components or find components whose temperature coefficients cancel. Appendix D gives the temperature coefficients for the resistors, capacitors, and inductors in the transceiver. The capacitors in the VFO are made of polystyrene, which has a small negative temperature coefficient. The inductor is made of a carbonyl iron powder with a small positive temperature coefficient to cancel the capacitive shift. In addition, instead of a ceramic trimmer capacitor, we set the VFO with an air-variable capacitor, which is quite stable.

11.4 Gain Limiting

The JFET in the VFO does not actually overload. Instead, the gain is limited by a detector diode, which keeps the output well below the supply voltage, giving a clean sine wave. Figure 11.6 shows the circuit. The starting resistor ensures that initially the gate voltage begins at ground, giving a large initial g_m so that the oscillation starts easily. The detector diode conducts on positive peaks of the gate

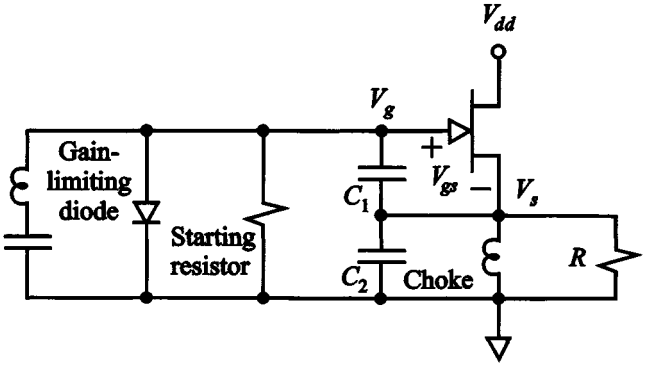


Figure 11.6. The VFO circuit in the NorCal 40A. The choke sets the DC source voltage to zero. The diode limits g_m to give a clean sine wave.

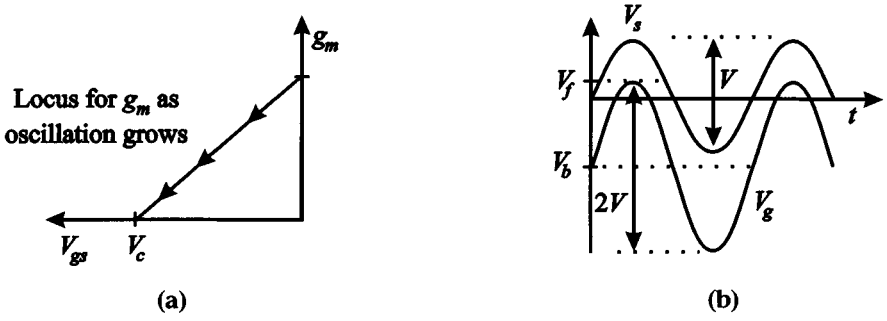


Figure 11.7. Effect of the gain-limiting diode on g_m as the oscillation builds up (a). V_g and V_s waveforms (b).

voltage. When the diode conducts, it pulls charge through the capacitors, and this gives the gate a negative bias, reducing g_m. As long as g_m is greater than $1/R$, the value required by the oscillation condition, the oscillation grows. This causes more current through the diode, and the bias voltage drops further, taking g_m with it (Figure 11.7a). Eventually an equilibrium is reached where the oscillation condition is satisfied, and the oscillation does not grow any more.

Figure 11.7b shows the final gate and source voltage waveforms V_g and V_s. They are both sinusoidal. We let V be the peak-to-peak value of the output voltage V_s. For our VFO, $C_1 = C_2$, and Equation 11.23 tells us that the peak-to-peak value of V_g is twice that of V_s. In addition, V_g and V_s have different DC values. V_s has no DC offset because of the choke. However, the peak voltage of V_g is limited to V_f, the forward voltage of the gain-limiting diode. This gives V_g a large negative DC offset V_b. From Figure 11.7b we can write

$$V_b = V_f - V. \tag{11.31}$$

To find the gate-source voltage V_{gs}, we subtract V_s from V_g. This is shown in Figure 11.8a. The peak-to-peak value of V_{gs} is V. V_{gs} is always negative, and the DC bias is V_b. The maximum value of the gate-source voltage V_m is given by

$$V_m = V_b + V/2. \tag{11.32}$$

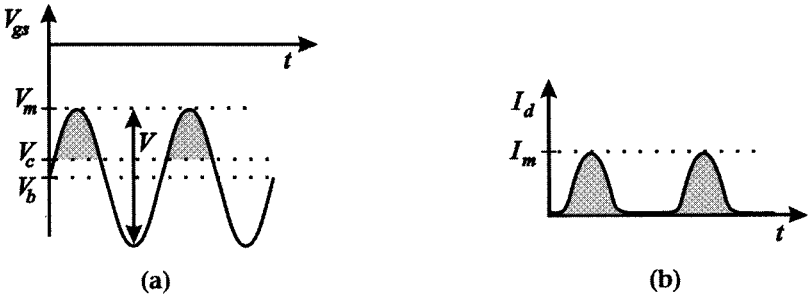


Figure 11.8. VFO gate-source voltage V_{gs} (a), and drain current I_d (b).

We can substitute for V_b from Equation 11.31 to get

$$V_m = V_f - V/2. \tag{11.33}$$

In practice, the bias voltage V_b is below the cut-off voltage V_c. This means that the JFET is active for less than half a cycle and that it is operating in Class C. Power is added to the oscillator in current pulses, rather than continuously (Figure 11.8b). One might liken this to a person pushing a child in a swing. We calculated the start oscillation condition in terms of g_m, which only applies when the JFET is active and the signals are small. Now we have large signals and a JFET that is off more than half the cycle. We define a *large-signal transconductance* G_m given by

$$G_m = I/V, \tag{11.34}$$

where I and V are the peak-to-peak values of the fundamental components of the drain current and gate-source voltage. G_m is also called a *describing function*. In the VFO, it is the amplifier gain; thus we can combine Equations 11.5 and 11.24 to get the oscillation condition:

$$G_m = 1/R. \tag{11.35}$$

G_m can be calculated approximately from JFET characteristics. We start with Equation 9.74 for the drain current:

$$I_d = I_{dss}(1 - V_{gs}/V_c)^2. \tag{11.36}$$

As an approximation, we assume that the current is on for nearly half a cycle, and this gives the current a cosine-squared shape. Therefore the average value of the current over the half cycle will be half its peak value, and the average current over the entire cycle will be a quarter of its peak value. We can write the DC drain current I_o approximately as

$$I_o = I_m/4, \tag{11.37}$$

where I_m is the maximum drain current. The fact that the current is proportional to the cosine squared gives the current a narrow pulse shape. In Section B.4, the Fourier series for a pulse train is derived, and it is shown that the peak-to-peak value of the fundamental component is four times the DC component. This means we can write

$$I \approx I_m. \tag{11.38}$$

Now we can divide by V to get

$$G_m = I_m/V. \tag{11.39}$$

Figure 11.9 is a plot of G_m versus V, calculated using this formula and Equation 11.33 and Figure 9.15. The oscillation condition is $G_m = 1/R$, and I have added

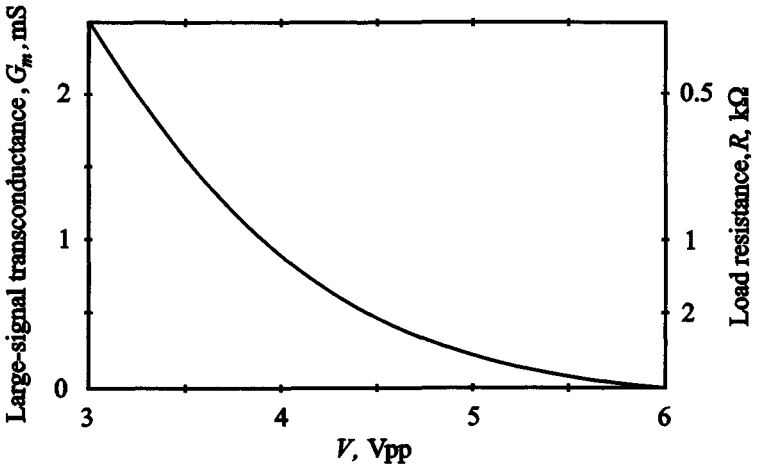


Figure 11.9. Large-signal transconductance G_m of the J309 JFET in a Clapp oscillator with $C_1 = C_2$. V is the peak-to-peak value of both the gate-source voltage and the output voltage. The right axis gives the load resistance R on an inverted scale to allow prediction of the output voltage.

an inverted scale for R to show this relation. The plot also allows us to predict the output voltage because V is equal to the output voltage.

11.5 Crystal Oscillators

The crystal oscillators in the NorCal 40A are also Clapp oscillators (Figure 11.10). These circuits are included in the SA602AN mixer ICs. The amplifier is an emitter

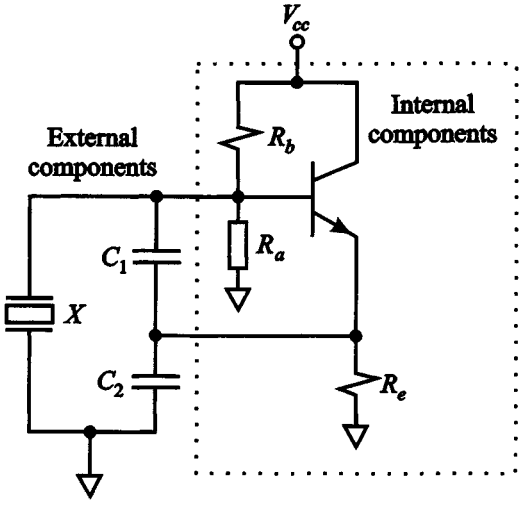


Figure 11.10. Clapp crystal oscillator in the SA602AN integrated circuit that is used for the Transmit Oscillator and the Beat Frequency Oscillator.

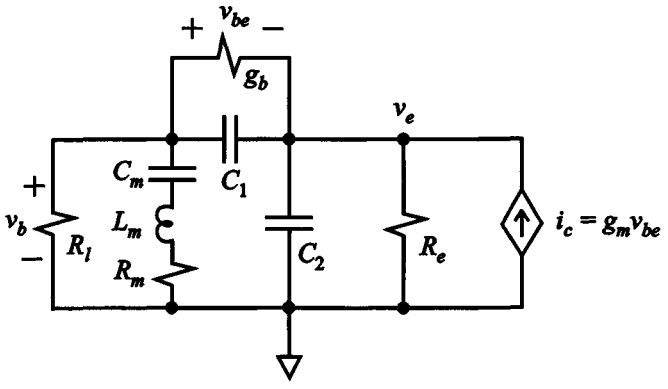


Figure 11.11. Equivalent circuit for the Clapp crystal oscillators.

follower, and R_b (18 kΩ) and R_e (25 kΩ) are internal bias resistors. R_a represents the internal load, which is a buffer amplifier that drives the mixer. We neglect the reactance of the internal load. C_1 and C_2 are external capacitors that form the divider network. X is an external crystal resonator.

The analysis can be simplified if we use a small-signal BJT model with a transconductance that is like that for the JFET. The circuit shown in Figure 11.11. The collector current i_c is given by

$$i_c = g_m v_{be}. \tag{11.40}$$

In the oscillator analysis, we consider v_{be} as the amplifier input and i_c as the output, so that we can write the small-signal gain g as

$$g = g_m, \tag{11.41}$$

The crystal is represented by its motional inductance L_m and capacitance C_m. Provided the Q is large, we meet the phase condition again at the resonant frequency ω_0 given by

$$-\frac{1}{j\omega_0 C_1} - \frac{1}{j\omega_0 C_2} = j\omega_0 L_m + \frac{1}{j\omega_0 C_m}. \tag{11.42}$$

We can rewrite this in terms of the resonant frequency as

$$\omega_0 = \frac{1}{\sqrt{L_m C}}, \tag{11.43}$$

where C is the series combination of the three capacitances, given by

$$C = \frac{1}{1/C_1 + 1/C_2 + 1/C_m}. \tag{11.44}$$

Finding the starting condition is complicated by the fact that there are many sources of loss in the oscillator that may be important. In Figure 11.11, we include the effect of the load as R_l, the crystal resistance as R_m, the base–emitter diode as a conductance g_b, and the emitter bias resistor as R_e. R_l itself represents the parallel

combination of the base bias resistor R_b and the buffer amplifier impedance R_a. The crystal resistance R_m varies considerably from crystal to crystal.

For the base–emitter conductance we use Equation 9.23,

$$g_b = I_b / V_t, \tag{11.45}$$

where I_b is the DC base-bias current and V_t is the thermal voltage, 25 mV at room temperature. We have to be careful in using this formula, because it is a small-signal formula, and the base current varies greatly during a cycle. We can think of it as the average of the conductance over a cycle.

We transform all the resistances to an equivalent resistance R parallel to the current source, assuming the Q is high in each case. There are successive transformations from parallel to series and then series to parallel. We skip the details and write

$$\frac{1}{R} = \frac{(C_1 + C_2)^2}{R_l C_1^2} + R_m(\omega_0 C_2)^2 + g_b\left(\frac{C_2}{C_1}\right)^2 + \frac{1}{R_e}. \tag{11.46}$$

Now we can use Equation 11.20 that we developed for the JFET VFO, provided we identify "base" with "gate" and "source" with "emitter." The starting condition becomes

$$g_m > \frac{C_1}{RC_2} = \frac{(C_1 + C_2)^2}{C_1 C_2 R_l} + (\omega_0 C_1)(\omega_0 C_2)R_m + \frac{C_2}{C_1}\frac{I_b}{V_t} + \frac{C_1}{C_2 R_e}. \tag{11.47}$$

Previously we found that g_m is proportional to the collector bias current I_c (Equation 9.26). If the oscillation does not start, it may be possible to start it by adding an external resistor in parallel to R_e to increase the bias. Also, it should be noticed that although each resistance pushes up the required value of g_m, making it harder to start, the effect of the divider capacitors depends on where the loss in the circuit comes from.

For a large-signal analysis, we need to consider that the emitter current comes in narrow pulses. This is because the relationship between the base voltage and collector current is exponential, and small changes in voltage cause large spikes in current. This is shown for a Clapp crystal oscillator in Figure 11.12. The fact that the emitter current comes in narrow pulses allows us an easy way to predict the output voltage, because we know that the peak-to-peak value of the fundamental component is four times the DC current (Appendix B, Section 4). We write

$$I = 4I_o, \tag{11.48}$$

where I is the peak-to-peak value of the emitter current and I_o is its DC value. Equation 11.21 lets us write the peak-to-peak value of the output voltage V across the load R_l as

$$V = IR\frac{C_1 + C_2}{C_1}. \tag{11.49}$$

It is hard to say much about this formula because R is itself a function of the various

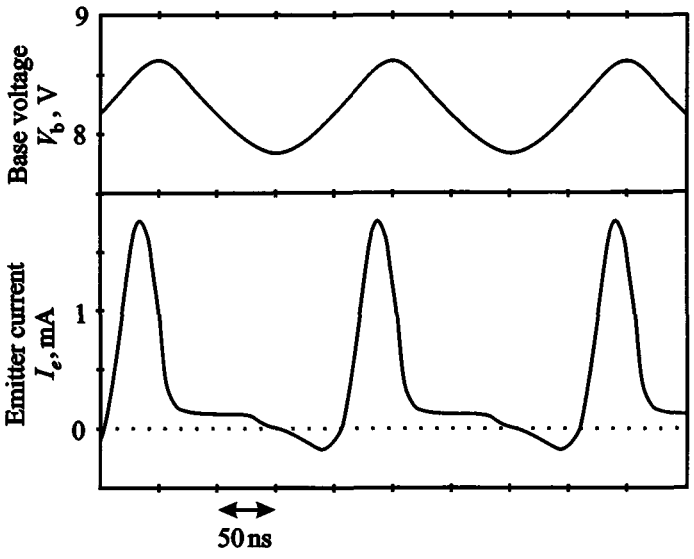


Figure 11.12. Measured emitter current I_e and base voltage V_b for a breadboard Clapp crystal oscillator. The component values are the same as those used in SA602AN and in the NorCal 40A. A 2N4124 transistor like the one in the Receiver Switch is used in place of the internal transistor in the SA602AN to make it easy to measure the emitter current through a 100-Ω series resistor.

resistances and capacitances. However, if the load resistance R_l is dominant, we can use Equation 11.46 to write

$$V = \frac{4I_o R_l C_1}{C_1 + C_2}. \tag{11.50}$$

This formula predicts that the output voltage increases as C_1 increases. In the NorCal 40A, C_1 is a trimmer capacitor, and this effect is quite noticeable during tuning.

11.6 Phase Noise

In addition to long-term frequency drifts due to temperature changes, oscillators have random phase shifts due to fluctuations in the oscillator current (Figure 11.13a). This is called *phase noise*. Phase noise causes power to spread away from the carrier frequency to nearby frequencies. Phase noise is a problem because receivers treat it like an ordinary signal, and we hear increased noise at the receiver output. Phase noise is also a problem in circuits such as multimeters that convert analog signals to digital ones, because it causes *jitter* in the timing circuits.

We can get a feeling for the effect of current fluctuations by considering an LC resonator with a charge q injected (Figure 11.13b). The injection phase is

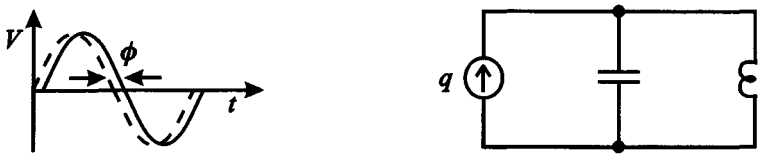


Figure 11.13. (a) Phase noise in an oscillator. The dashed line indicates a sine wave at the carrier frequency, while the solid line shows the output of an oscillator with a phase shift ϕ. (b) Model for phase noise with a charge q injected into an LC resonator.

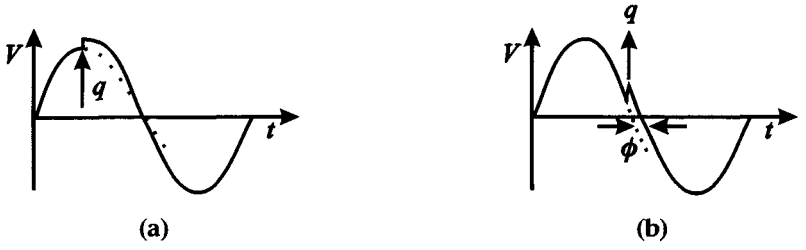


Figure 11.14. (a) Charge injection at the voltage peak (a) and at the zero crossing (b). Charge injection at the peak causes no phase shift, whereas charge injection at the zero crossing causes a large phase shift.

crucial. The charge goes directly into the capacitor, because the current in an inductor cannot change suddenly. This means that the voltage on the capacitor jumps, while the inductor current remains the same. If the charge comes at the peak of a cycle, where the capacitor voltage is maximum and the inductor current is zero, there is no change in the oscillator phase, only a change in amplitude (Figure 11.14a). The amplitude change will be smoothed out by the gain-limiting action of the oscillator, and it is not of much consequence. However, if the charge is injected at the zero crossing where the capacitor voltage is zero and the inductor current is large, the charge causes a large change in phase with only a small change in amplitude (Figure 11.14b).

The fluctuations in transistor currents are much larger when the transistors are active than when they are off. For this reason, it is important that the transistor be active near the peak voltage, rather than near the zero crossing, where the fluctuations would cause phase noise. In the Clapp oscillator, the transistor is active at the peak and off during the zero crossing, and this gives it low phase noise.

FURTHER READING

This chapter owes much to *The Design of CMOS Radio-Frequency Integrated Circuits*, by Thomas Lee, published by Cambridge University Press. The research by Hajimiri and Lee on phase noise has rendered previous writing on oscillators obsolete. Many practical designs and construction details for VFOs are given in *The ARRL Handbook*, published by the American Radio Relay League. Synthesized oscillators are thoroughly

covered in *Communications Receivers, Principles and Design,* by Ulrich Rhode and T.T.N. Bucher, and published by McGraw-Hill.

PROBLEM 26 - VFO

The VFO shown in Figure 11.15 is more complicated than the previous circuits we have built. It is a good idea to check all the connections carefully. Oscillator circuits can be frustrating, because one bad connection can prevent the oscillation from starting, and it is difficult to find the problem because there is no signal to trace.

We will consider each component in turn. C52 and C53 form the capacitor divider network. L9 and C51 form the series resonator. D8 is a *varactor* diode. It acts as a variable capacitor, controlled by the reverse bias voltage. The voltage determines the capacitance by controlling the thickness of the depletion layer. Our diode is the MVAM108. These diodes are intended for tuning AM radios, and that is where the "AM" in the type number comes from. "M" is for Motorola, "V" is for varactor, and "8" is for 8 V, the top voltage at which this diode should be used. The MVAM108 gives a wide range of capacitance from 600 pF at low voltages to 30 pF at 8 V. In the circuit, we control the bias on the varactor diode with a potential divider network formed by R17 and R20. R17 is a large potentiometer that sets the bias on the varactor. This is our tuning knob for the radio. R19 is a large series resistor that keeps the divider network from loading the resonator, and C49 prevents L9 from shorting out the divider.

C50 is an air-variable capacitor in parallel with L9. The capacitance is a maximum, about 25 pF, when the leaves are fully meshed, and a minimum, about 2 pF, when the leaves are unmeshed. We use C50 to set the range of frequencies that can be covered by the VFO. RFC2 is a choke that gives a DC ground connection to the source. C54 is an RF bypass capacitor that keeps the RF impedance between the drain and ground low. D9 is the detector diode that controls the gain of the JFET. R21 sets the initial gate bias

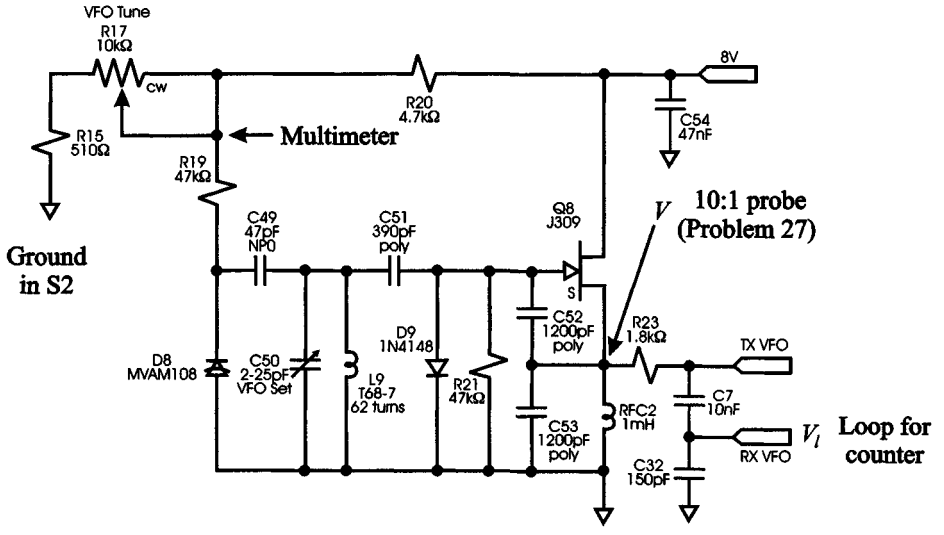


Figure 11.15. The VFO in the NorCal 40A.

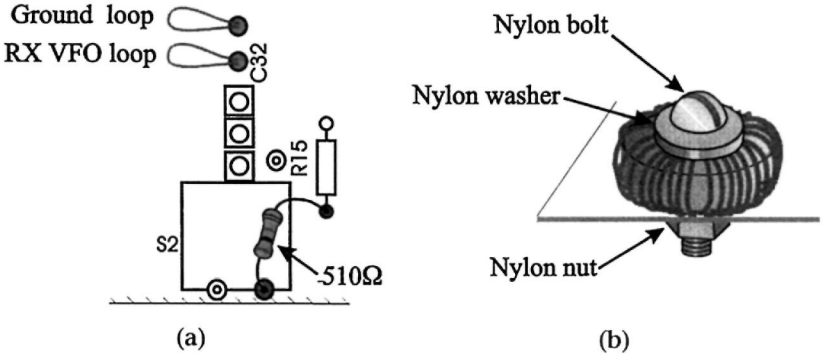


Figure 11.16. Special solder connections for the VFO (a), and mounting L9 (b).

at zero volts to ensure that the oscillation starts. R23 is the load. R23 and C32 act as a low-pass filter that sets the input voltage levels for the Transmit Mixer and the RF Mixer. C7 provides a DC block between the mixer inputs.

To start, install all of the components in Figure 11.15. Be careful not to overheat the polystyrene capacitors C51, C52, and C53 when you are soldering them in. If the plastic melts, they short out. After you have installed the R17 pot, take a pair of pliers and twist off the locking tab to the left of the shaft. This tab is meant to fit in a slot in the front panel, and we will not need it. If you do not take it off, it will interfere with the front panel. Also make sure that the nut and washer stay on the pot. You will need them later. There are some special connections that are shown in Figure 11.16a. The 510-Ω resistor should be soldered between the R15 hole and one of the ground holes in S2 at the edge of the board. There are two additional wire loops to solder in to make it easy to hook on probes to check the output of the VFO. Stick both ends of a loop in the same hole and solder them.

The L9 inductor uses a 68-7 core. The number "68" indicates the size of the core (0.68" diameter), and "7" is the number of the iron-powder mix. #7 cores are painted white. In Problem 9 we used the red 37-2 cores for the Transmit Filter. #7 cores are more stable than #2 cores. See Appendix D for more information. For the coil, you should start with 1.5 m of #28 wire. Wind 62 turns tightly and neatly around the core without overlapping the wires. The turns should be spread as evenly as possible. Check your coil carefully. If the turns bunch or the count is wrong, you may have to add or subtract a turn later. Solder the coil to the board. L9 is also secured to the board by a nylon bolt, washer, and nut to keep the core from moving (Figure 11.16b). It also helps pin down the turns of the winding. The stepped side of the washer should face the core to help it fit in neatly.

Now we are ready to test the oscillator. With a screwdriver, set the air-variable capacitor (C50) to half-mesh. Plug in the power supply, and turn on the power. Attach a 10:1 probe to the probe loops (RX VFO and the ground loop in Figure 11.16a). The oscilloscope should be set for an internal trigger. Verify that you see a sine wave.

A. Attach a multimeter probe to measure the DC voltage of the wiper of the R17 pot. This is the multimeter connection shown in Figure 11.15. Record the wiper voltage when R17 is fully counterclockwise and when it is fully clockwise.

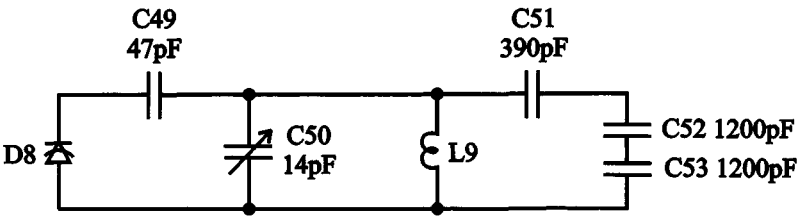


Figure 11.17. Simplified circuit diagram for calculating the resonant frequency, showing L9 and the important capacitances.

B. Now we will try to calculate these numbers. From Figure 11.15, what would you expect the multimeter voltage to be for the counterclockwise setting? For the clockwise setting?

C. Study the data sheets in Appendix D to find the capacitance of the MVAM108 for these voltages. You may need to extrapolate a bit.

D. Replace the scope probe with counter leads. What is the frequency when R17 is counterclockwise? How much does the frequency increase when we rotate R17 fully clockwise?

E. Now we are ready to calculate the oscillation frequency. Our experience has been that the inductance constant for the 68-7 core varies considerably. A reasonable value to use is $A_l = 5.0$ nH/turn^2. Calculate the inductance for L9 with 62 turns. I have drawn a simplified circuit diagram for the important reactive elements in Figure 11.17. We have neglected the transistor Q8, the diode D9, the choke RFC2, and the load circuits. You can take C50 to be the average of its fully meshed and unmeshed values, 14 pF. Calculate the resonant frequency for the counterclockwise setting. Now calculate how much the frequency should increase for the clockwise setting.

PROBLEM 27 - GAIN LIMITING

A. Measure the peak-to-peak source voltage V. You should connect the 10:1 probe at the source end of R23 for this (Figure 11.15).

B. Now use Figure 11.9 to predict the output voltage V that satisfies the large-signal oscillation condition. Your prediction may be high because we have not considered circuit losses.

C. In deriving the oscillation condition for our VFO, we neglected the inductor resistance and the drain-source resistance of the JFET r_d. How does the oscillation condition change if we add these effects? If L9 has a Q of 250, and the JFET output resistance is $r_d = 5$ kΩ, what is the new prediction for V?

D. The voltage is smaller at the RX VFO loop. Measure the loop voltage V_l with the 10:1 probe. You should remove the counter probe for this measurement so that it does not load the circuit. Find the loss ratio $|V/V_l|$. For comparison, calculate the ratio that you would expect.

E. Now measure the temperature dependence of the oscillator. Reattach the counter probe to the RX VFO loop so that you can measure the frequency. Rest the bulb of a thermometer on the screw hole in the circuit board near R6. Heat the board with a hair drier until the temperature reaches 50°C. This is best done with the board in a plastic box with holes that direct the flow of air. See Appendix A for more information. Switch off the hair drier. Record the temperature and the frequency as the temperature drops. From your measurements, find the frequency sensitivity in Hz/°C. Find the temperature coefficient in ppm/°C. How large a temperature change would be necessary to cause the frequency to shift 100 Hz?

F. There is an advantage in having a high VFO frequency, because this makes it easy for filters to reject the image. However, there is a big disadvantage: less stable oscillators. Assume we reduce the capacitance and inductance by a factor of six to increase the VFO frequency by the same factor. This would leave us with the same IF frequency as before. The radio would work with no modification, and the image of the VFO would be rejected more easily. To see the difficulty with this approach, calculate the temperature change that would be needed to cause the frequency to drift 100 Hz, assuming the same temperature coefficient as before.

G. Now calculate the temperature coefficient that you expect, assuming that the polystyrene capacitors have a temperature coefficient of −150 ppm/°C and the 68-7 core has a temperature coefficient of +50 ppm/°C. You may neglect the effect of the other components.

H. Calculate the change in the oscillation frequency that you would expect from taking a turn off the inductor. Now set R17 fully counterclockwise, and adjust the air-variable capacitor (C50) until the oscillation frequency is 2,085 kHz. This sets the lower end of the tuning range for the radio. If you cannot reach this frequency, you will need to change the number of turns.

The next step is to install the Receiver-Incremental-Tuning (RIT) circuit. This is our first chance to use one of the eight-pin integrated-circuit (IC) packages. You will also hear these called DIP (for "dual-in-line package," because the pins come in two lines). In digital circuits, it is common to mount the ICs in sockets, so that they can be easily removed if they burn out. In radio circuits, however, people usually solder in the ICs. This reduces problems of noise pickup and helps prevent unwanted oscillations. The problem with soldering an IC is that it is difficult to remove, because you have to get all the solder off each lead before it will budge. Check that you have the IC oriented correctly before you solder! Manufacturers make a notch or a dimple at one end, and there is a matching notch in the board outline. It is important to be able to identify each pin by number. The pins are numbered in a counterclockwise direction from the notch (Figure 11.18a). You should realize that the numbering is only counterclockwise if you look from the top of the package. From the bottom side, it is clockwise. This can be confusing, particularly when the IC is mounted on the board.

The RIT allows us to offset the receive frequency from the transmit frequency. Some operators may have transmitters and receivers that are not aligned, or their transmitters

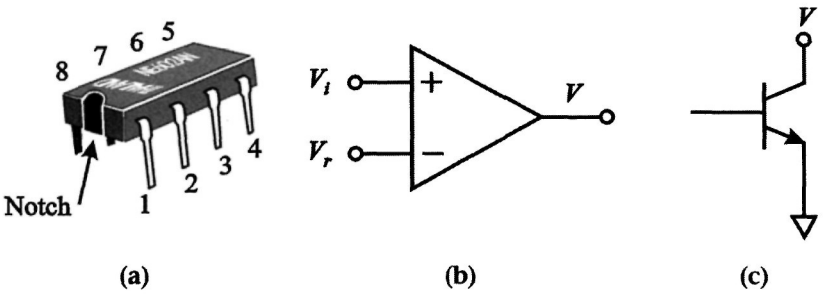


Figure 11.18. Identifying the pins on an eight-pin DIP package (a). Schematic symbol for a comparator (b). Open-collector circuit for one of the LM393N comparators (c).

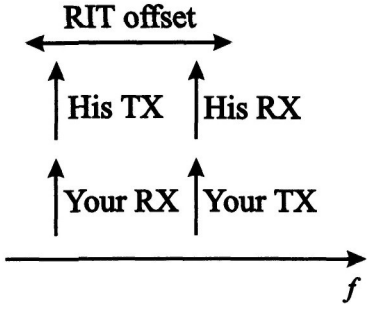


Figure 11.19. Using the RIT to adjust your receive frequency (RX) when the other operator's receive and transmit (TX) frequencies are not aligned.

may drift from heating, while their receiver does not. The RIT shifts the receive frequency without changing the transmit frequency. For example, assume that the other operator's transmit frequency is lower than his receive frequency. This means that you need an RIT offset to align your receiver with his transmitter (Figure 11.19). In our measurements, the RIT is useful for fine adjustments of the receiver frequency.

The RIT circuit uses an IC with a pair of comparators, the LM393N by National Semiconductor. The letters "LM" identify an IC from National Semiconductor, and "N" indicates a DIP package. A *comparator* is a differential amplifier with a very high voltage gain, typically about 200,000. Figure 11.18b shows the schematic symbol for a comparator. The triangle is the usual symbol for an amplifier. The differential inputs are labeled + and − so that you know which input is subtracted. Typically, one of the inputs is a voltage that changes, and we label it as V_i. The other is a fixed voltage that we call V_r, with the r standing for "reference." You can understand what the comparator does if you consider the output circuit for the comparator, which is just an npn transistor with its collector open-circuited (Figure 11.18c). People call this an *open-collector* output. We have two possibilities. If V_i is even slightly less than V_r, the gain of the comparator is so large that we will have a large base current in the output transistor. The input need only be a few microvolts below the reference voltage to completely turn the transistor on. The output transistor will present a low impedance to ground for an outside circuit. However, if the input voltage V_i is even slightly greater than V_r, the output transistor will turn off. We can reverse this if we apply V_i to the − input and V_r to the + input.

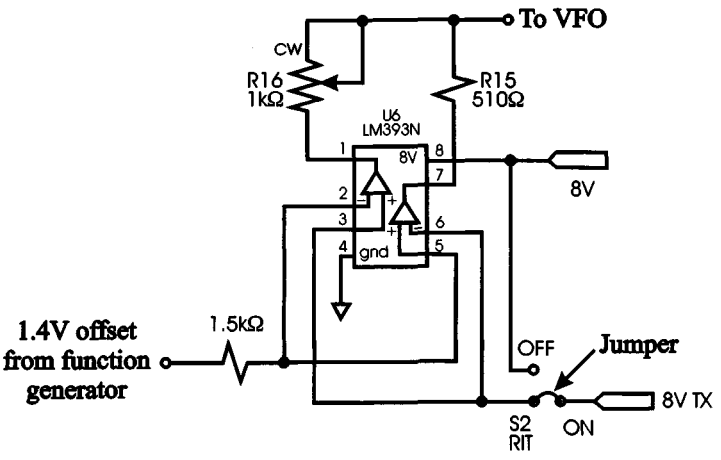


Figure 11.20. The RIT circuit. The original NorCal 40A circuit has a switch S2 to turn the RIT on and off. In our measurements we will not use the switch, but we will add a jumper so that the RIT is always on.

Now we can understand how the RIT circuit works (Figure 11.20). If the transmitter is on, 8V TX will be at 8V. This is greater than the reference voltage, 1.4 V, and it means that the left comparator will be off, and the right comparator will be on. R16 is disconnected, and R15 is effectively connected to ground, and the VFO will work in the same way it did in the last laboratory exercise.

However, for receiving, 8V TX will be below the 1.4-V reference. This disconnects R15, and shorts R16 to ground in its place. R16 is a 1-kΩ pot. Its resistance ranges from near zero to twice as large as R15. The pot setting adjusts the varactor voltage just the way the VFO Tune pot does. However, since the RIT pot varies over only 1 kΩ rather than the 10 kΩ that the VFO Tune pot covers, we get a finer frequency control. We will use the RIT for precise frequency adjustment of the receiver.

Now we are ready to build the RIT circuit. The first thing that you should do is to take the 510-Ω resistor lead that you connected to ground last time and move it to the empty R15 hole. Next pop the comparator IC into the U6 holes, checking the orientation carefully. Solder each of the pins for the comparator IC. Follow with the pot R16. Break off the locking tab to the left of the shaft with a pair of pliers, so that the tabs do not get in the way when we add the front cover.

There are several special connections (Figure 11.21). In the S2 outline, add a ground jumper wire across the two holes at the edge of the board. This is just another ground connection for probes. In addition, add a short jumper to bypass S2 in the two holes that are shown in the figure. Then solder one end of a 1.5-kΩ resistor to hole 2 of U2. This is our 1.4-V reference connection, and for this measurement it can be provided by an offset voltage from a function generator.

1. Now plug in the power supply and turn it on. The counter should be connected to the RX VFO loop. Also insert a shorting plug into the Key jack to turn on 8V TX. Use the big VFO Tune pot R17 to set the frequency close to 2,100 kHz. Record this

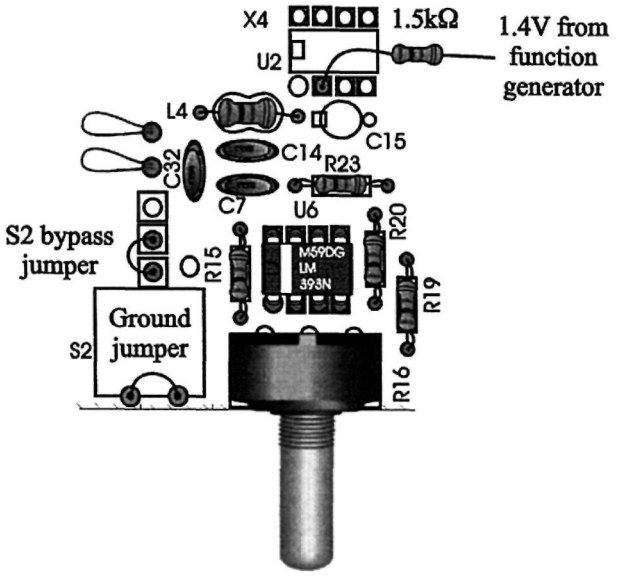


Figure 11.21. Jumpers and connections for the RIT circuit.

frequency. While the transmitter is on, the RIT should not work. You should verify that twiddling the RIT pot does not change the frequency appreciably. Now remove the shorting plug from the Key jack. This should turn off 8V TX and allow the RIT to work as a fine frequency control. Full counterclockwise rotation should give the minimum frequency, and full clockwise rotation should give the maximum. Record the RIT tuning range. Remove the 1.5-kΩ resistor from U2.