# CNTFET-Based Design of Ternary Multiplier using Only Multiplexers

Ramzi A. Jaber*, Ali M. Haidar
*Depart. of Electrical & Computer Engineering*
*Beirut Arab University*
Debieh, Lebanon
r.jaber@ieee.org*; ari@bau.edu.lb

Abdallah Kassem
*Depart. of Electrical & Computer Engineering*
*Notre Dame University*
Louaize, Lebanon
akassem@ndu.edu.lb

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***Abstract*—Multiple-valued logic (MVL) circuit has many-valued logic in each digit to lower interconnections and energy consumption over a binary logic circuit. Therefore, this paper proposes a ternary multiplier (TMUL) that reduce energy consumption in the context of low-power embedded circuits. The CNTFET-based TMUL circuit use only cascading proposed ternary multiplexer to reduce the transistors count and improve performance efficiency. Extensive simulations along with several benchmark designs using HSPICE, prove the merits of the proposed TMUL by reducing energy consumption, improving the noise tolerance, and robustness to process variations (TOX, Channel length, CNT Count, and CNT Diameter).**

***Index Terms*—Carbon Nano-Tube Field Effect Transistors (CNTFET), Multiple-Valued Logic (MVL), Multiplexer (MUX), Process Variations, Ternary Logic Circuits.**

## I. Introduction

MVL circuits reduce the interconnections and energy consumption unlike binary circuits since each digit can hold more than two states [1].

Among all different base systems, ternary logic has a higher performance system in terms of circuit complexity and cost [2]. There are two methods to implement the ternary system: unbalanced (0, Vdd/2, Vdd) equivalent to (0, 1, 2), and balanced (-Vdd, 0, Vdd) equivalent to (-1, 0, 1).

Therefore, the researchers are interested in MVL and implemented it in algorithm [3], healthcare applications [4], and ternary circuit designs [5], [6].

CNTFETs have a higher performance among all different transistor technologies [7].

The authors of [8]–[10] designed TMULs using the conventional design by utilizing the basic logic gates and Ternary Decoder (TDecoder).
In [8], the authors presented a TMUL with 100 CNTFETs using TDecoder (16 CNTFETs), binary logic gates, and Ternary Encoder. While in [9], the authors designed a TMUL with 76 CNTFETs using TDecoder (10 CNTFETs), NAND, Ternary NAND, and Standard Ternary Inverter (STI). Whereas in our past paper [10], we proposed a TMUL with 61 CNTFETs using TDecoder (9 CNTFETs), two power supplies (Vdd, Vdd/2) and applying De Morgan's Law.

However, in [11], the authors represented a ternary multiplexer (TMUX) with 28 CNTFETs and a TMUL with 112 CNTFETs using cascading TMUXs while in [12], the authors presented the TMUX with 18 CNTFETs.

**Contributions:**
The designs mentioned above suffer from many transistors count, high energy consumption, low robustness to process variations, or low noise tolerance because they use Ternary Decoders and basic logic gates that lead to high transistors count (compared to [8]–[10]).

Thus, this paper proposes efficient circuit implementation of TMUL with 60 CNTFETs using previous proposed "decoderless" TMUX (15 CNTFETs) [13].

## II. CNTFET Transistor

This paper uses the Stanford CNTFET model, which can be found in [14]. However, it is worth to mention that the CNTFET threshold voltage is depend on the CNT diameter and is calculated by the following equation (1):

$$V_{\text{th}} = \frac{\sqrt{3}}{3}\frac{d \cdot V\pi}{e \cdot Dcnt} \tag{1}$$

Where $d$, the distance of carbon-carbon atom, is equal to 2.49 Å; $V\pi$, the carbon bond energy, is equal to 3.033; $e$ is the electron charge unit, and $Dcnt$ is the CNT diameter.

The relationship between the diameter and threshold voltage for (D1=1.487 nm, and D2=0.783 nm), and the operation of the CNTFET transistor is described in Table I.

TABLE I: CNTFET Operation with D1=1.487 nm, D2=0.783 nm

| Type | Diameter | Threshold voltage | Voltage Gate 0V | 0.45V | 0.9V |
|---|---|---|---|---|---|
| P-CNTFET | D1 | - 0.289 V | ON | ON | OFF |
| | D2 | - 0.559 V | ON | OFF | OFF |
| N-CNTFET | D1 | 0.289 V | OFF | ON | ON |
| | D2 | 0.559 V | OFF | OFF | ON |

## III. Ternary Multiplexer

Block diagram of (3:1) Ternary Multiplexer (TMUX) is represented in Fig.1, which has three inputs ($I_0$, $I_1$, $I_2$), one selection ($S$), and one output ($Z$) that depends on ($S$) as described in Eq. (2).

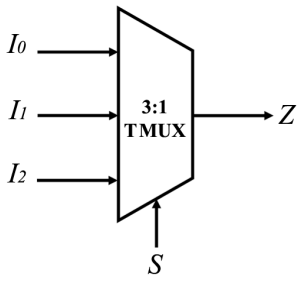


Fig. 1: The model of (3:1) TMUX

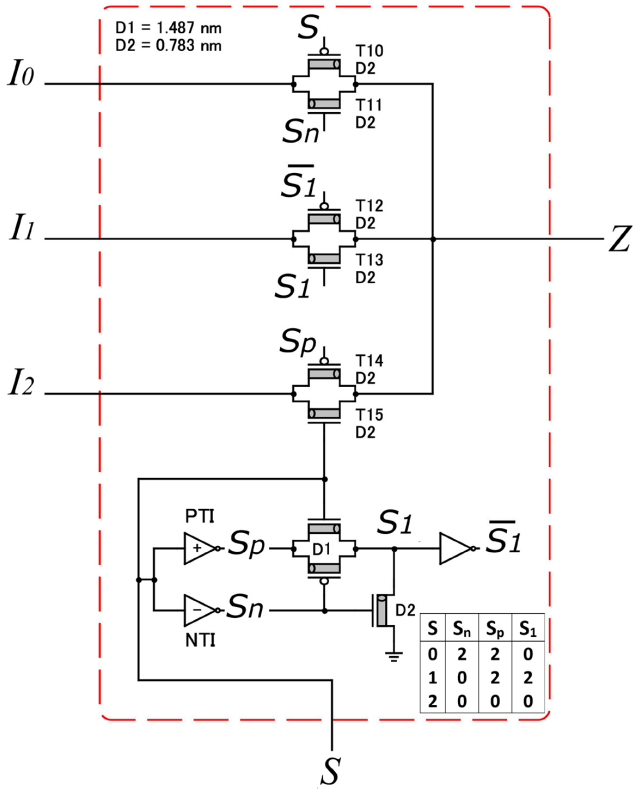


Fig. 2: Previous proposed TMUX with 15 CNTFETs [13].

$$Z = \begin{cases} I_0, & if \quad S = 0 \\ I_1, & if \quad S = 1 \\ I_2, & if \quad S = 2 \end{cases} \tag{2}$$

Figure 2 shows the previous proposed "decoder-less" TMUX with 15 CNTFETs [13] using transmission gates and three unary operators (one-input and one-output logic gates): PTI (Positive Ternary Inverter, $S_p$), NTI (Negative Ternary Inverter, $S_n$), and $S_1$.

## IV. Proposed Ternary Multiplier

The TMUL multiplies two ternary inputs ($A$, $B$) and produces two ternary outputs ( $Product$, $Carry$), as shown in Table II.

Table II can derive the equations of the Product and the Carry to lead two designs:

1) Conventional design, like in [8]–[10], uses Equation (3).
2) Cascading TMUXs design, like in [11] and adopted in this paper, uses Equation (4).

TABLE II: Truth table of TMUL

Product

| A/B | 0 ($B_0$) | 1 ($B_1$) | 2 ($B_2$) |
|---|---|---|---|
| 0 ($A_0$) | 0 | 0 | 0 |
| 1 ($A_1$) | 0 | 1 | 2 |
| 2 ($A_2$) | 0 | 2 | 1 |

Carry

| A/B | 0 ($B_0$) | 1 ($B_1$) | 2 ($B_2$) |
|---|---|---|---|
| 0 ($A_0$) | 0 | 0 | 0 |
| 1 ($A_1$) | 0 | 0 | 0 |
| 2 ($A_2$) | 0 | 0 | 1 |

$$\begin{aligned} Product &= 2 \bullet (A_1B_2 + A_2B_1) \\ &+1 \bullet (A_1B_1 + A_2B_2) \\ Carry &= 1 \bullet A_2B_2 \end{aligned} \tag{3}$$

$$\begin{aligned} Product &= 0.B_0 + A.B_1 + \\ &(0.A_0 + 2.A_1 + 1.A_2).B_2 \\ Carry &= 0.B_0 + 0.B_1 + \\ &(0.A_0 + 0.A_1 + 1.A_2).B_2 \end{aligned} \tag{4}$$

Where $A_k$ and $B_k$ are the TDecoder outputs from inputs $A$ and $B$, respectively where $k \in \{0,1,2\}$.

Figure 3 shows the proposed TMUL using cascading TMUX with (4*15) 60 CNTFETs.

The advantages of the proposed TMUL are: (1) Not using TDecoder and basic logic gates like [8]–[10], (2) Using our previous proposed TMUX [13]. These positive points can decrease the number of used transistors and PDP. Also, improving the robustness to process variations and noise tolerance.

## V. Experimantal Results

The proposed TMUL is compared to CNTFET-Based TMULs in [8], [10], [11] and extensively simulated using the HSPICE for temperature variation (from 0°C to 70°C ), power supply variation (from 0.8 V to 1 V), frequency variation (from 0.5 GHz to 2 GHz), Noise effect, and process variations (TOX, Channel length, CNT Count, and CNT Diameter).

Table III shows the comparison of all investigated circuits for TMUL in terms of transistors count, average power ($\mu$W), maximum delay (ps), and PDP (x$10^{-18}$ J) with power supply at 0.9 V, frequency at 1 GHz, and temperature at 27°C.

The proposed TMUL has a significant reduction in transistors count and PDP.

Around 40%, 1.64%, and 46.43% compared to transistors

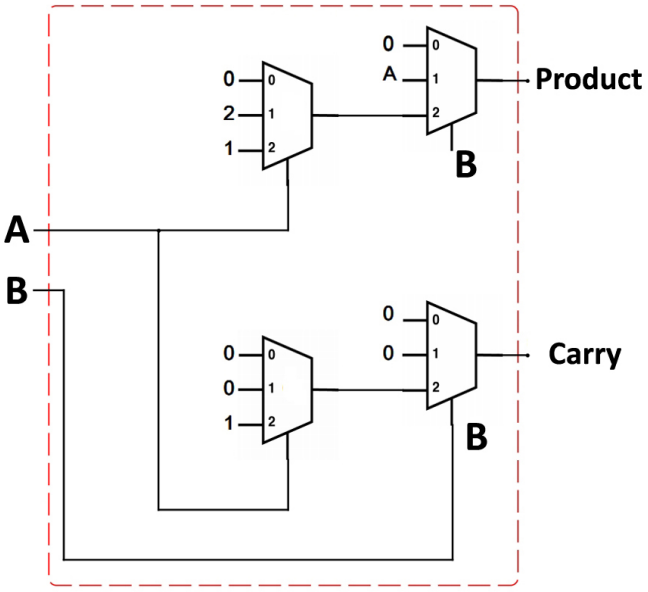


Fig. 3: The Proposed TMUL with 60 CNTFETs.

TABLE III: TMULs Comparison

| TMUL | Transistors count | Power $\mu$W | Delay ps | PDP x$10^{-18}$ J |
|---|---|---|---|---|
| In [8] | 100 | 1.88 | 46.32 | 87.08 |
| In [10] | 61 | 0.42 | 54.82 | 23.02 |
| In [11] | 112 | 1.93 | 18.21 | 35.15 |
| **Proposed** | 60 | 0.17 | 9.65 | 1.64 |

count in [8], [10] and [11], respectively.
Around 98.11%, 92.87%, and 95.33% compared to PDP in [8], [10] and [11], respectively.

Fig.4 displays the PDP comparison to the models in [8], [10] and [11].
Fig.4(a) shows power supply (from 0.8 V to 1 V) with a frequency at 1GHz and temperature at 27°C.
Fig.4(b) shows temperature (from 0°C to 70°C) with a frequency at 1GHz and power supply at 0.9 V.
Fig.4(c) shows frequency (from 0.5 GHz to 2 GHz) with a power supply at 0.9 V and temperature at 27°C.

As shown in Fig. 4, the proposed TMUL has the lowest PDP among all the investigate circuits for power supply variation, temperature variation, and frequency variation.

### *A. Process Variations & Noise Effect*

Figure 5 shows the Stanford CNTFET model as described in [14].

Process variation is the generally occurring change in the attributes of transistors (oxide thickness, length, ...) when fabrication integrated circuits. the variation has a high impact on the robustness and performance of transistors and circuits.

Therefore, all TMUL circuits are tested for major process variations: TOX, Channel length, CNT Count, and CNT Diameter using Monte Carlo analysis [16], which is based on the statistical Gaussian distributions with ±15%, ±10%, and ±5% variations at the ±3 sigma ($\sigma$) level with 1000 simulations run.

Figure 6 shows the PDP variation of all TMUL circuits for major process variations, which demonstrates that the proposed TMUL has the lowest sensitivity to process variations and highest robustness among all the investigated circuits because the PDP variation is the smallest.

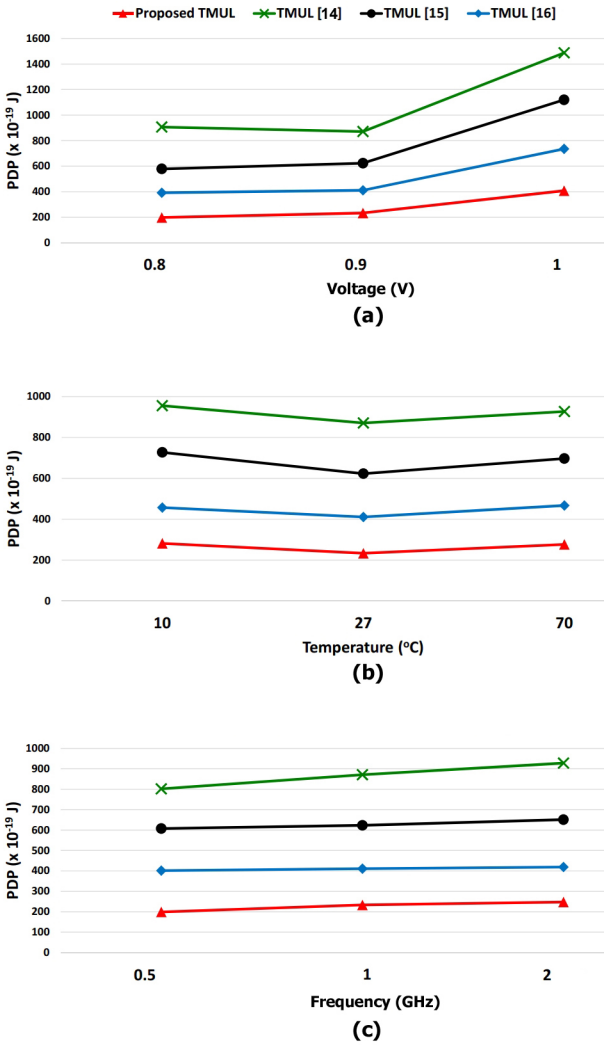


Fig. 4: PDP variation of All TMULs: (a) For voltage variation, (b) for temperature variation, and (c) for frequency variation.

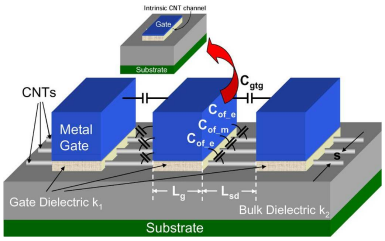


Fig. 5: Stanford CNTFET Model.

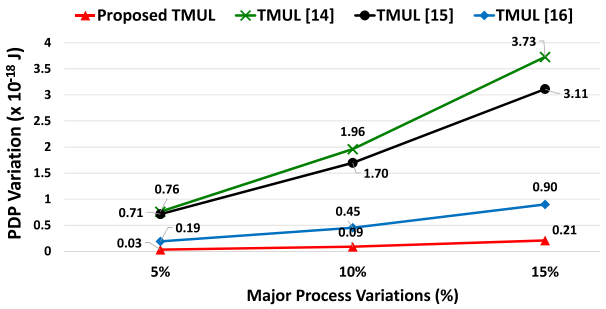


Fig. 6: Major Process Variations: TOX, Channel length, CNT Count, and CNT Diameter.

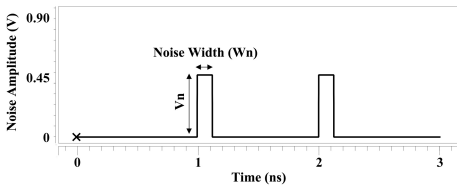


Fig. 7: Noise Signal.

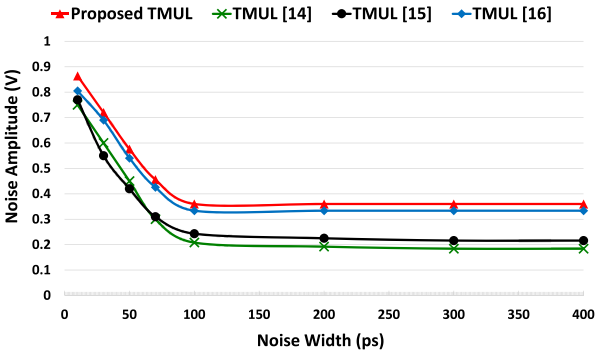


Fig. 8: Noise Immunity Curve (NIC).

Figure 7 shows the noise signal, which is injected into inputs of all TMULs. The noise signal has a pulse amplitude ($V_n$) and a pulse width ($W_n$).

Each point on the Noise Immunity Curve (NIC) is a pair of ($W_n$, $V_n$). The circuit will provide an output error above that point.

Thus, every circuit has a higher NIC shows a more noise-tolerant circuit [17].

The proposed TMUL shows the highest noise immunity among others, as shown in Fig. 8.

## VI. Conclusion

This paper proposed a Ternary Multiplier using a ternary multiplexer based on 32 nm channel CNTFET, which intends to enhance performance and energy efficiency.

The comparison of the proposed TMUL to other designs showed significant performance improvement for several simulation metrics using HSPICE simulator for temperature variation, voltage variation, frequency variation, major process variations, and noise effect.

The results confirmed that the proposed TMUL had higher robustness and noise tolerance among other designs.

Thus, the proposed TMUL can be applied in embedded systems to preserve battery consumption.

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